Lehrstuhl für Meß- und Regelungstechnik
im Maschinenbau und in der Verfahrenstechnik
Technische Hochschule Karlsruhe

EAI®

580/680

SCIENTIFIC COMPUTING SYSTEM

Maintenance Series

26.268
DIGITAL VOLTMETER

EAI®

580/680

SCIENTIFIC COMPUTING SYSTEM

Maintenance Series

26.268
DIGITAL VOLTMETER

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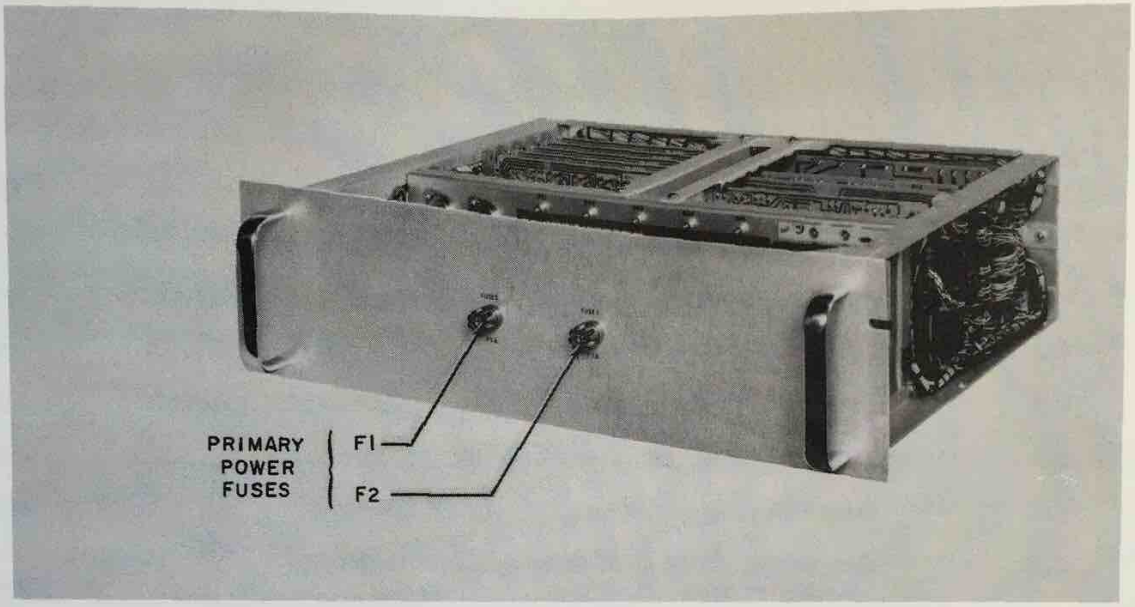
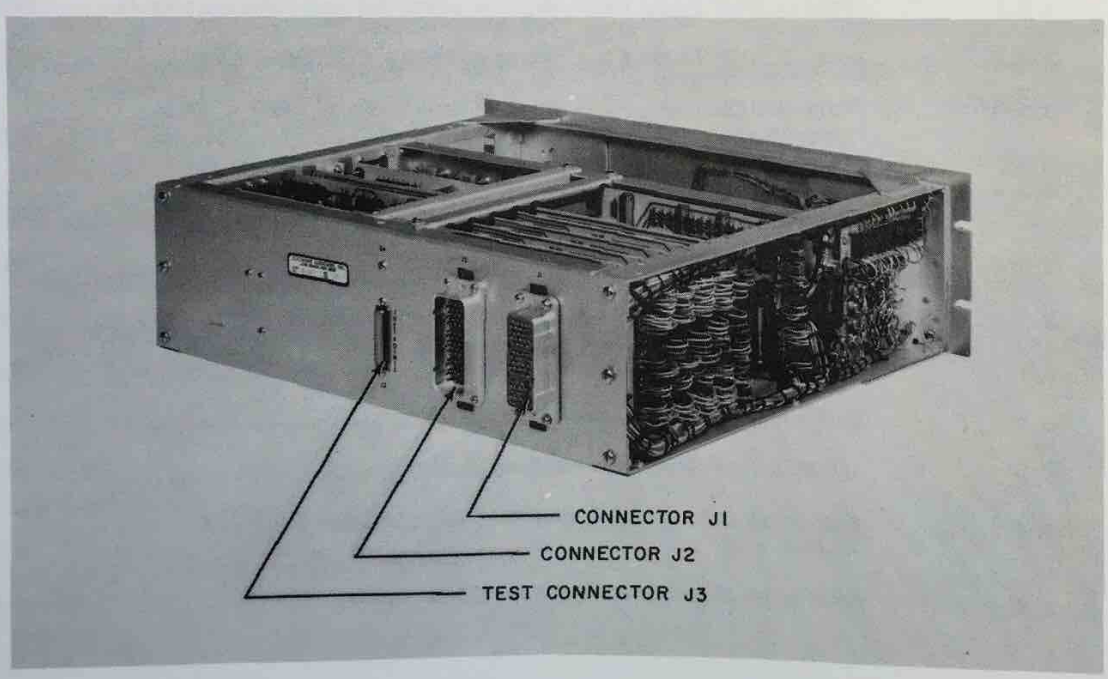


(a) Three-Quarter Front View



(b) Three-Quarter Rear View

Figure 1.1. Digital Voltmeter, Model 26.268

CHAPTER 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

The 26.268 Digital Voltmeter (DVM) shown in Figure 1.1, is a complete analog-to-digital conversion unit, containing a power supply, analog input amplifiers, and all necessary logic circuits. The unit is designed and manufactured by the Instrument Division of Electronic Associates, Inc. (EAI), specifically for installation in the EAI 680 Scientific Computing System. A separate display unit (Model 554.048) is mounted on the computer control panel and indicates digitally the value and polarity of any analog input voltage within its range.

The DVM range is fixed at ±10 volts and has a 20% overrange capability. The display provides a five digit readout, polarity and decimal point symbols. The display is scaled in computer units (in the 680, one computer unit equals 10 volts), so the maximum reading with overrange is ±1.1999 computer units, equal to ±11.999 volts. An input unloading network provides an extremely high full time input impedance.

The DVM uses the programmed-comparison (successive-approximation) conversion principle that combines accuracy and high speed. The unknown input voltage is connected to a pair of cascaded operational amplifiers that provide an unloading circuit, as well as providing both polarities of the unknown voltage to the digitizing circuits. The logic circuits in the DVM select the necessary polarity for conversion and display the corresponding polarity symbol on the readout unit. The DVM then compares the unknown with a precise reference potential of the opposite polarity, added in binary-coded decimal increments, until the algebraic sum of the unknown and the reference is equal to zero. The DVM registers then contain a binary-coded decimal (BCD) representation of the unknown input. Decoding circuits within the DVM provide an output to the display unit that is the decimal equivalent of the stored BCD data.

The input sampling rate is determined by the ac line frequency, so that conversions occur 50 or 60 times each second. The conversion time (without a polarity change) is fixed at approximately 2 milliseconds, and the value is displayed during the time between convert commands.

Conversion Delay Network 12.1654 delays the convert command to permit the DVM to phase lock with ripple voltage in the 580/680 Computer. Variable resistor R3, located on the 12.1654 circuit board, controls the amount of delay.

1.2 PHYSICAL DESCRIPTION

The DVM chassis houses the power supply and the necessary analog and logic circuits for the digital voltmeter. Table 1.1 lists the physical characteristics of the 26.268 Chassis.

Table 1.1. 26.268 Chassis Physical Description

Dimension	Value
Height	5-1/4 Inches
Width (With Panel)	19 Inches
Depth	16 Inches
Weight	20 Pounds

Most of the DVM components (except for some power supply and analog input components) are mounted on plug-in etched circuit cards. These cards are listed in Table 1.2, and shown in Figure 1.2. The components that are not mounted on plug-in cards are shown in Figure 1.3.

Table 1.2. 26.268 DVM Plug-In Components (See Figure 1.2)

Component	Model Number	Quantity	Connector Position
Dual DC Amplifier	6.463-5	1	(AR2)
Reference Amplifier	6.736-1	1	(AR1)
Miscellaneous Network Card	12.937-5	1	(NW3)
Summing Resistor Network Card	26.116	1	(NW2)
Comparator and Diode Gate Card	26.242	1	(A8)
BCD Counter	38.032	3	(A1-A3)
BCD Counter	38.032-1	1	(A4)
Power Supply Regulator	43.141	1	(VR1)
Programmer	44.302-1	1	(A5)

The DVM is provided with three connectors at the rear (towards the front of the computer) that provide power and signal inputs to the unit, and outputs to the display indicators. These connectors are listed in Table 1.3. Tables 1.4 and 1.5 list the pin connections for J1 and J2, respectively. Pin connections for J3 are provided in Table 4.1 in Chapter 4.

Table 1.3. Connectors and Mating Plugs (See Figure 1.4)

DVM Connector	Mating Computer Connector	Function
J1	DV-P1	Signal Input-Decimal Output to Display
J2	DV-P2	Power Input-BCD Output
J3	None	Test Connector

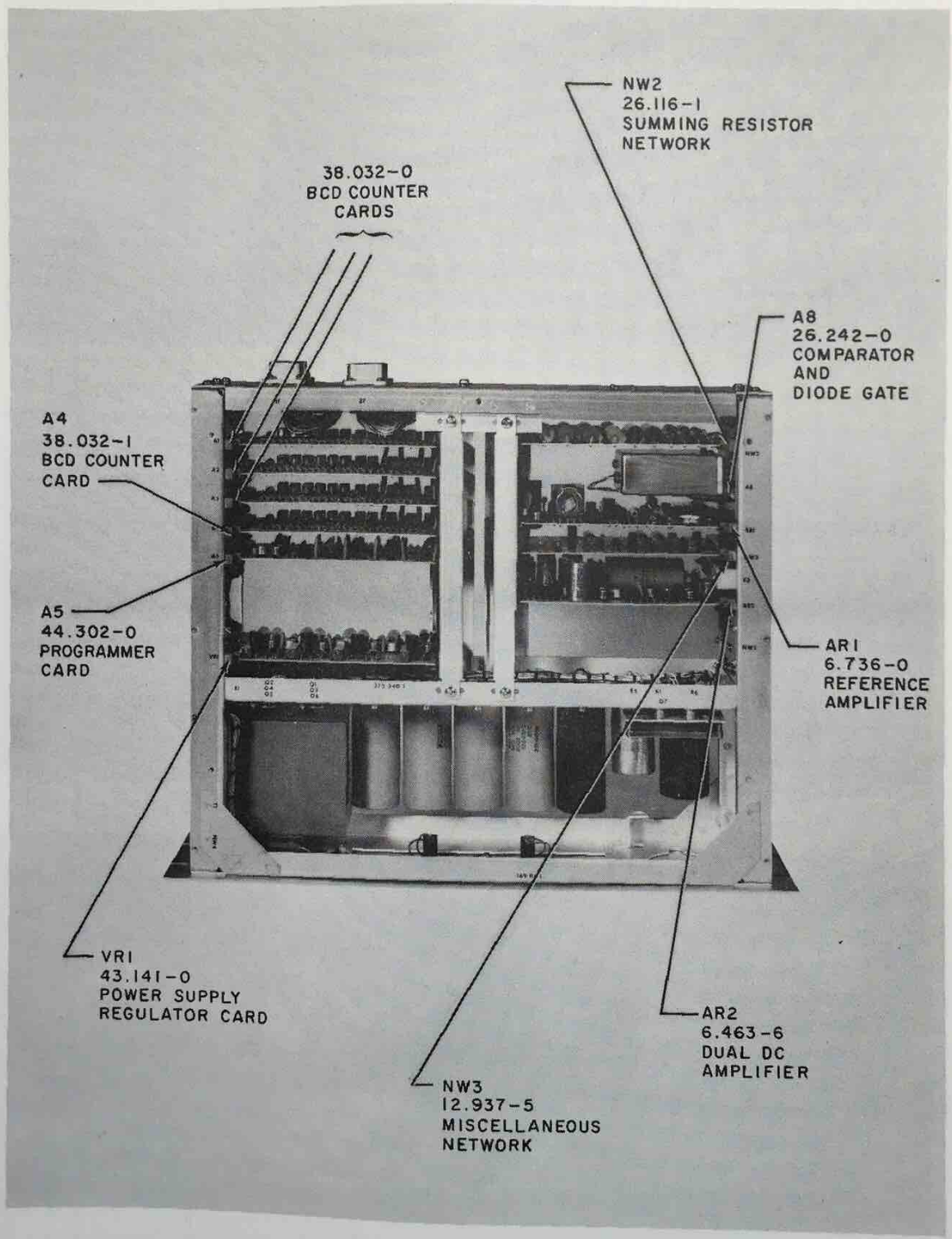
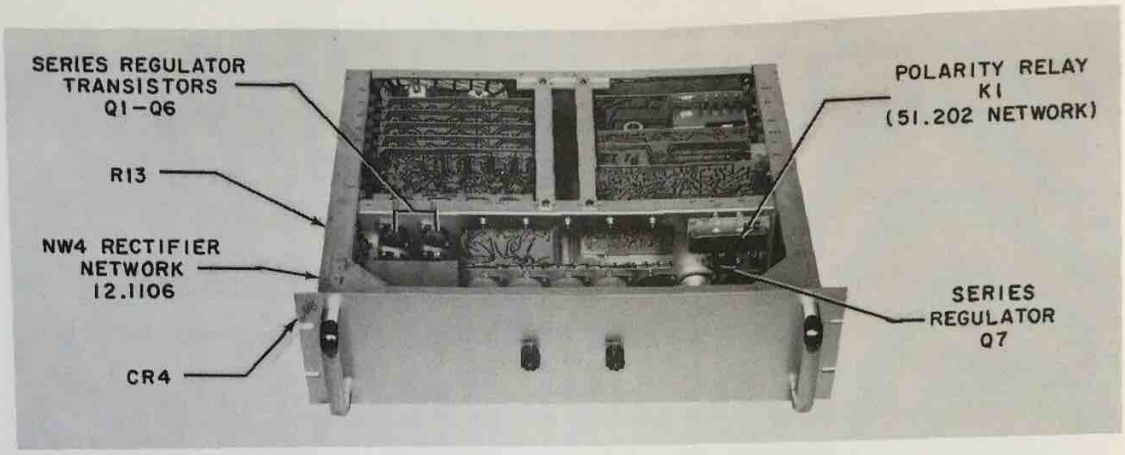
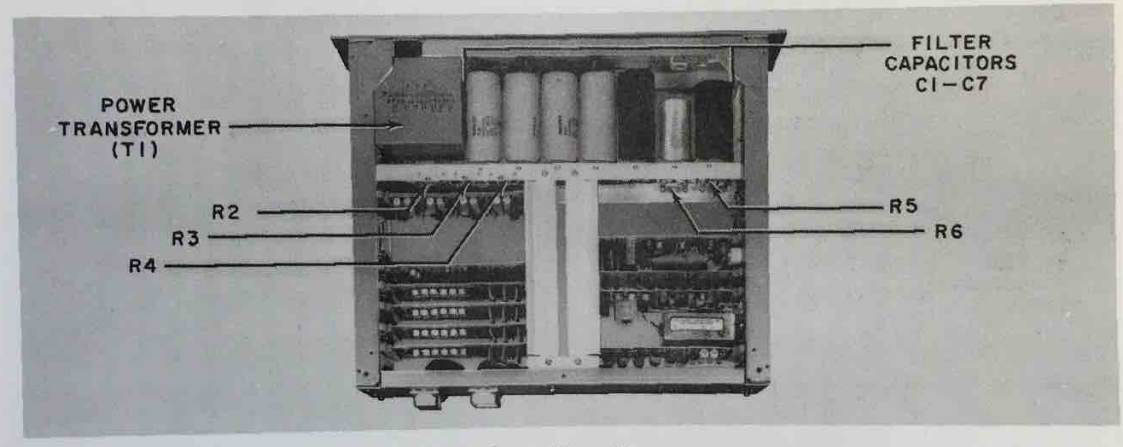


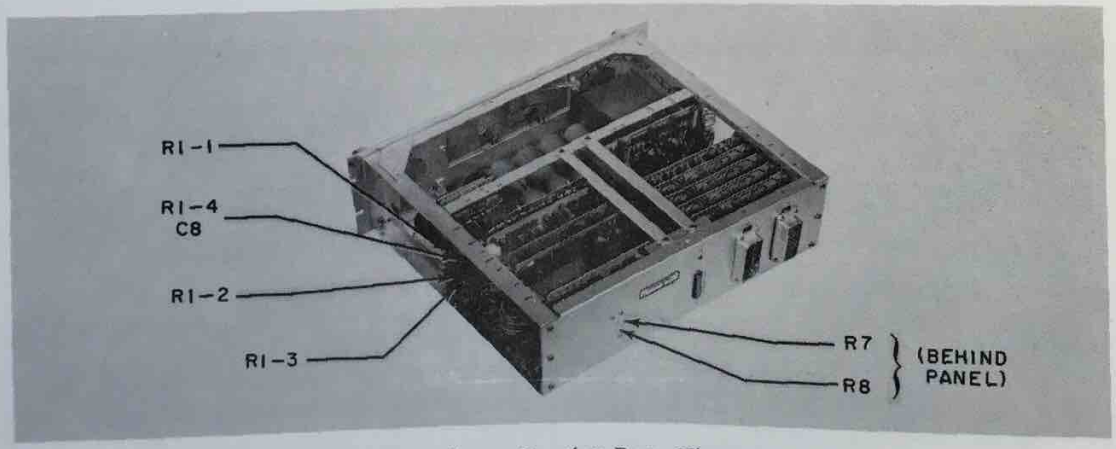
Figure 1.2. Model 26.268 DVM, Top View Showing Plug-In Cards



(a) Front View



(b) Bottom View



(c) Three-Quarter Rear View

Figure 1.3. 26.268 DVM Showing Fixed Components

Table 1.4. Connector J1 Terminals

Pin	Function	Electrical Characteristics
1-A	Decimal 1 (Units)	-0.8 volt* indicates presence of digit or symbol (can supply up to 5 ma of current). -7 volts indicates absence of digit or symbol (can supply up to 1 ma of current). See Drawing D026 268 0S, Sheet 3.
1-B	2	
1-C	3	
1-D	4	
1-E	5	
1-F	6	
1-G	7	
1-H	8	
1-J	9	
1-K	0	
1-L	Decimal 1 (Tens)	
1-M	2	
1-N	3	
1-P	4	
1-R	5	
1-S	6	
1-T	7	
1-U	8	
1-V	9	
1-W	0	
1-X	Decimal 1 (Hundreds)	
1-Y	2	
2-A	3	
2-B	4	
2-C	5	
2-D	6	
2-E	7	
2-F	8	
2-G	9	
2-H	0	
2-J	Decimal 1 (Thousands)	
2-K	2	
2-L	3	
2-M	4	
2-N	5	

**From saturated transistor in series with 4.7 ohm resistor.*

Table 1.4. Connector J1 Terminals (Continued)

Pin	Function	Electrical Characteristics
2-P	6	
2-R	7	
2-S	8	
2-T	9	
2-U	0	
2-V	Decimal 1 (Ten-Thousands)	
2-W	0	
2-X	+ Indicator	
2-Y	- Indicator	
3-A	Decimal Point Indicator Ground	-8 Volt Ground
3-B	Readout Display Ground	-8 Volt Ground
3-C	Readout Display Power	-8 Volts
3-D	Zero Adjust	Emitters of differential comparator amplifier to zero adjust pot.
3-E	Zero Adjust	
3-F	Zero Adjust Pot Wiper	+40 volts through a 56K resistor.
3-G	Signal Ground	Zero current ground reference.
3-H	$\frac{D}{10}$ Readout Feedback Resistor	Connection between pins 3-H and 3-K changes gain of first unloading amplifier from 1.25 to 0.125.
3-J	Signal Input	Analog signal from 0 to ±11.999 volts.
3-K	Unloading Amplifier 1 Summing Junction	See connections for pin 3-H above.

Table 1.5. Connector J2 Terminals

Pin	Function	Electrical Characteristics
1-A	Units BCD 1	Output normally taken from the NOT output terminations. -12 volts (from a source impedance of 2K) from the NOT terminals indicates the presence of a bit (can supply up to 0.5 ma of current); +2 volts (from a saturated transistor source) indicates the absence of a bit (can supply up to 5.0 ma of current). Complementary signals are available at the TRUE output terminals.
1-B	$\overline{1}$	
1-C	2	
1-D	$\overline{2}$	
1-E	4	
1-F	$\overline{4}$	
1-G	8	
1-H	$\overline{8}$	
1-J	Tens BCD 1	
1-K	$\overline{1}$	

Table 1.5. Connector J2 Terminals (Continued)

Pin	Function	Electrical Characteristics
1-L	2	
1-M	$\overline{2}$	
1-N	4	
1-P	$\overline{4}$	
1-R	8	
1-S	$\overline{8}$	
1-T	Hundreds BCD 1	
1-U	$\overline{1}$	
1-V	2	
1-W	$\overline{2}$	
1-X	4	
1-Y	$\overline{4}$	
2-A	8	
2-B	$\overline{8}$	
2-C	Thousands BCD* 1	*NOTE
2-D	$\overline{1}$	The thousands $\overline{2}$ and $\overline{8}$ bits at pins 2-F and 2-K, respectively, erroneously indicate a thousands ten for a 10,000 or 11,000 count. The thousands $\overline{2}_1$ and $\overline{8}_1$ bits at pins 2-M and 2-N, respectively, indicate the correct BCD code.
2-E	2	
2-F	$\overline{2}$	
2-G	4	
2-H	$\overline{4}$	
2-J	8	
2-K	$\overline{8}$	
2-L	Ten-Thousands BCD 1	
2-P	$\overline{1}$	
2-M	Thousands BCD* $\overline{2}_1$	
2-N	$\overline{8}_1$	
2-R	Conversion Complete Signal Complement	Complement of signal at pin 2-S.
2-S	Conversion Complete Signal	-12 to +2 volt leading edge of pulse indicates start of conversion; +2 to -12 volt trailing edge indicates end of conversion.
2-U	Zero Set Signal	+2 volt level with -12 volt pulse (100 microseconds minimum duration at beginning of conversion cycle).
2-V	+Sign Flip-Flop	+2 volts when input unknown is positive; -12 volts when input unknown is negative.
2-W	-Sign Flip-Flop	Complement of signal on pin 2-V.

Table 1.5. Connector J2 Terminals (Continued)

Pin	Function	Electrical Characteristics
2-X	HOLD Signal Input	External hold of conversion cycle; display remains constant until command is removed. Input should be a -12 to -25 volt level (normally, -15 volts), from a source capable of delivering 1 ma of current. See Chapter 2, Paragraph 2.3.
2-Y	-15 Volt Supply*	
3-A	+2 Volt Supply*	
3-B	External Trigger (Convert Command)	10-12 volt positive-going pulse with a rise time $\leq$5 microseconds, and a duration of at least 20 microseconds. See Chapter 2, Paragraph 2.3.
3-C	H-F Clock	8-10 kc "Master" clock, -11 to 0 volt pulses of 10 microseconds duration, rise time <1.5 microseconds.
3-D	Internal HIGH Clock	50/60 cps line frequency clock (normal Convert Command), -11 to 0 volt pulses, <1.5 microseconds rise time, 8 milliseconds in duration at 60 cps.
3-E	H.Q. (High-Quality) Ground	Zero current ground reference.
3-H	H.Q. Ground	Same as above.
3-J	+10 Volt Reference Input	Computer reference to DVM reference amplifier.
3-K	+15 Volt Supply*	
3-L	Internal LOW Clock	1-3 cps, -12 to 0 volt pulses, 10 microseconds in duration with a rise time of less than 1.5 microseconds. See Chapter 2, Paragraph 2.3.
3-P	±Ground	Common ground for all DVM power supplies.
3-U 3-W 3-X 3-Y	117 VAC Common 117 VAC Hot 117 VAC Hot 117 VAC Common	Primary power input terminals. For operation from 117 vac, 50/60 cps, pins 3-W and 3-X should be connected to 117 vac HOT input and pins 3-U and 3-Y should be connected to 117 vac COMMON input. For operation from 230 vac, 50/60 cps, pins 3-W should be connected to 230 vac HOT input, pins 3-U and 3-X should be jumpered together, and pin 3-Y should be connected to 230 vac COMMON. See Schematic D026 268 0S, Sheet 4.
3-V	Chassis Ground	

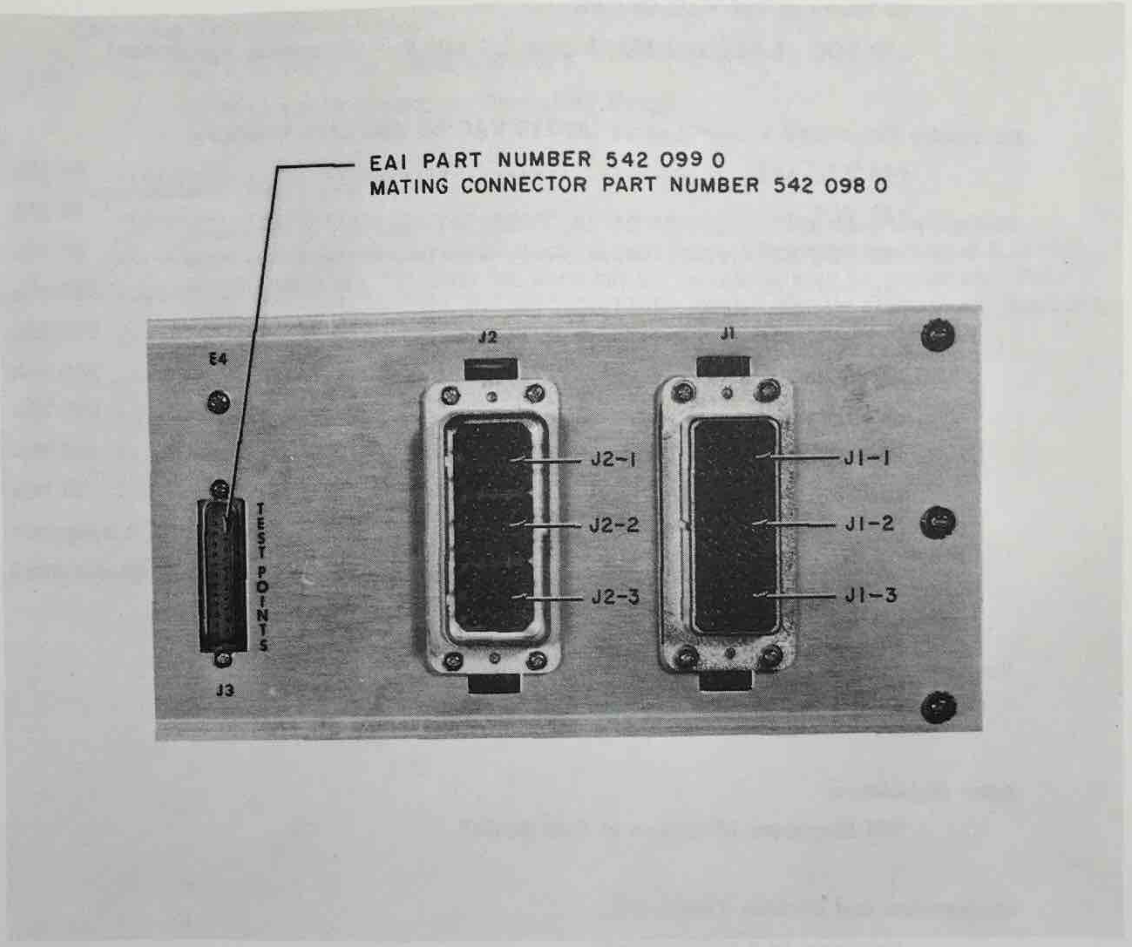
1.3 TECHNICAL DATA AND SPECIFICATIONS

Power Requirements

105 to 125 VAC at 50/60 CPS, provisions for 210-250 VAC operation.

83 VA at 117 VAC 60 CPS

**See Paragraph 1.3 for voltage tolerances.*



Connector Designation	Connector Shell	Connector Blocks		Pins		Sockets	
	Part Number	Qty.	Part Number	Qty.	Part Number	Qty.	Part Number
J1	198 952 0	3	542 1244 0	—	———	54	674 145 0
J1 Mating Connector*	198 953 0	3	542 1243 0	54	674 144 0	—	———
J2	198 953 0	3	542 1243 0	58	674 144 0	—	———
J2 Mating Connector*	198 952 0	3	542 1244 0	—	———	58	674 145 0

**Note: A cover shell (EAI Part No. 198 925 0) may be used with the mating connector for J1 or J2.*

Figure 1.4. DVM Rear View Showing Connectors

69 Watts at 117 VAC 60 CPS

+10 VDC ±0.01% at 1 MA; Ripple $\leq$ 1 MV P-P (Computer Reference)

Internally Generated Power Levels (At 115 VAC 60 CPS Line Voltages)

+40 VDC ±1%	20 MA
+20 VDC ±1%	35 MA
-20 VDC ±1%	80 MA
+15 VDC ±5%	20 MA
-15 VDC ±5%	300 MA
-7.5 VDC ±7%	920 MA
±2 VDC ±10%	650 MA
-8 VDC Unregulated	480 MA
-21 VDC Unregulated	25 MA
6.3 VAC	1.8 Amperes
-100 VDC ±0.005% (With Respect to Computer Reference)	20 MA (Reference)

Range

0-10 Volts +20% Overrange (00.000 to 11.999 Volts)

Input Impedance

500 Megohms Minimum at Full Scale*

Conversion and Display Time

Converts in 2 Milliseconds

Displays for 14.7 Milliseconds (60 CPS Line Frequency)

Displays for 18 Milliseconds (50 CPS Line Frequency)

NOTE

The unknown input voltage is sampled continuously at a rate of 50 or 60 samples per second, depending on ac line frequency.

Accuracy

±0.01% of full scale** +1 digit with respect to the DVM -100 volt reference and +10 volt computer reference.

**Maximum input current does not exceed 20 nanoamperes at any input voltage within the range.*

***Full scale is defined as 10.000 volts.*

Operating Temperature Range

50°F to 100°F at Rated Accuracy

40°F to 120°F Maximum Operating Range

Temperature Coefficient

A change in reading of 0.0005% per °F typical. (This does not include the zero set temperature coefficient; a maximum change in reading of 0.0008% of full scale per °F from the zero set temperature may be expected. This change in reading from the zero set temperature may be eliminated, however, by readjusting the ZERO control.)

CHAPTER

2

CHAPTER 2

INSTALLATION AND OPERATION

2.1 INSTALLATION

The DVM and the display unit are installed in the computer before shipment. The DVM is completely adjusted and calibrated prior to shipment, and should be ready for use when received. The DVM should be checked as a part of the general visual inspection when the computer is received, to assure that all connectors are in place and that none of the etched circuit cards have been jarred loose.

2.1.1 Preliminary Checks

When visual observations confirm that all etched-circuit cards and the connectors in J1 and J2 are properly installed, a check of the electrical operation may be performed.

1. Check that all required power levels are present; initially, this may be performed with any 10% accuracy voltmeter. The voltages are present at J3 on the rear of the DVM chassis. Refer to Table 4.1 in Chapter 4 to locate the appropriate pins.

2. Adjust the DVM ZERO control on the computer to provide a readout of ±0.0000 with the DVM patching terminal connected to ground. If the polarity relay begins to chatter, turn the zero control slightly clockwise until the polarity symbol remains constant and the indicators retain the all zero display.

3. Connect a 0 to 10 volt variable input (either polarity) to the DVM (a potentiometer and inverter of the computer can be used). Slowly vary the input level from 0 to 10 volts, and note that the DVM counting sequence is functioning properly.

4. Apply a positive and then negative input (less than 11.999 volts in each case) to the DVM input, noting that the proper polarity sign is displayed.

5. If the DVM does not appear to be functioning properly, refer to Chapter 4 and correct the difficulty.

2.2 NORMAL OPERATION

The DVM operates in conjunction with the computer readout system to display voltages at selected points. It is necessary only to address a component with the signal selector system in order to digitally display the value of an analog level. The operation of the signal selector system is described in the 680 Computer Maintenance Manual.

2.3 SPECIAL OPERATION

The DVM, as installed in the computer, is designed to be free-running; that is, readings are taken continuously at a rate (50/60 cps) determined by the frequency of the ac power input. Special applications (such as the addition of a printer or other recording device) may require interlocking the operation of the DVM with other equipment. Built-in features of the DVM permit simple external modifications to slave the operation of the meter to an external device. The 50/60 cps trigger is jumpered from pin 3-D to pin 3-B of connector DV-P2. To supply an external trigger, this jumper must be removed, and an external trigger may be applied to pin 3-B of DV-P2. This trigger (or convert command) should have an amplitude of 10 volts, (positive going), with a rise time of less than 5 microseconds. The DVM registers will contain the digital equivalent of the unknown input approximately 2 milliseconds after the input trigger (without a polarity change), or after approximately 37 milliseconds if a polarity change is required.

A low-frequency triggering technique may also be used. The DVM contains a low-frequency oscillator (1-3 cps) that may be used if a lower triggering rate is required. The output of this oscillator appears on pin 3-L of DV-P2. To use this oscillator as a trigger source, the jumper between pins 3-D and 3-B must be removed, and a jumper installed between pins 3-L and 3-B of DV-P2.

A third triggering technique uses the high-frequency oscillator (8-10 kc) as a trigger source. If trigger rates above 100 cps are employed, the DVM display will be difficult or impossible to read, since the ratio of display time to conversion time decreases. If the high-frequency oscillator is to be used as a trigger source, the jumper between pins 3-D and 3-B of DV-P2 is removed, and replaced between pins 3-C and 3-B of DV-P2. The DVM now converts continuously at a rate of approximately 500 conversions per second. Under these conditions, the display unit cannot provide any meaningful information. However, if a -15 volt Hold signal is applied to pin 2-X of DV-P2, the continuous conversions are interrupted for the duration of the signal and the

display may be observed. The DVM registers will contain the correct data approximately 2 milliseconds after the application of the Hold signal if no polarity change was in progress, and 37 milliseconds after the Hold signal if a polarity change was in progress (i.e., if the input signal polarity changes immediately prior to, or coincident with, the Hold command). Other signals present at DV-P2 may be used as required by an interlocked read-print system. The Conversion Complete signal (+2 volts when conversion is completed) is available at DV-P2, pin 2-R. Its complement ($\overline{\text{conversion complete}}$) is present at pin 2-S of DV-P2, and has a value of -12 volts when conversion is completed.

Whenever modifications to the basic DVM system are contemplated, it is suggested that the user contact the nearest EAI Service Engineering office for assistance. Experienced field representatives may be able to offer cost-saving techniques and help to avoid potentially troublesome system approaches. A list of the EAI Field Sales and Service Engineering offices is provided at the front of this manual.

CHAPTER

3

CHAPTER 3

THEORY OF OPERATION

3.1 INTRODUCTION

This chapter describes the theory of operation of the DVM in terms of a block diagram and a functional diagram analysis. The descriptions are supplemented by block diagrams, simplified schematics, a timing diagram, functional diagrams, logic diagrams, and a power distribution diagram. Transistor theory and standard circuits incorporating these devices are not described in detail since much written material is available on these subjects.

The DVM utilizes the programmed-comparison type of meter circuit where the current produced by the unknown (or input) voltage is compared to a known current which is the BCD equivalent of the analog unknown; decoding the BCD count to the common decimal equivalent provides a decimal display of the unknown magnitude. Polarity detection circuits provide a display of the polarity sign.

3.2 BLOCK DIAGRAM DESCRIPTION

Figure 3.1 is a block diagram illustrating the operation of the DVM. The unknown input is applied to the unloading amplifiers which provide the high input impedance of the meter as well as the scaling of the unknown input. This unloading input system consists of two cascaded operational amplifiers. The first amplifier determines the scale factor given the unknown input. The second amplifier has a fixed gain-of-one. The two amplifiers provide both a positive and a negative polarity scaled-representation (equal in magnitude) of the input unknown. Both polarities of the scaled unknown are applied to the polarity relay K1.

The state of the polarity relay is always set to provide the *positive* scaled representation of the unknown to the comparator summing junction since it is to be compared to a known current generated by a *negative* reference voltage source. The polarity of the unknown input determines which of the two amplifiers will provide the scaled positive signal, and the polarity relay is always switched to select this positive potential.

The proper state of the polarity relay is determined by the programmer. The programmer temporarily removes all the known current from the comparator summing junction thus placing the comparator input entirely under the influence of the scaled unknown input as selected

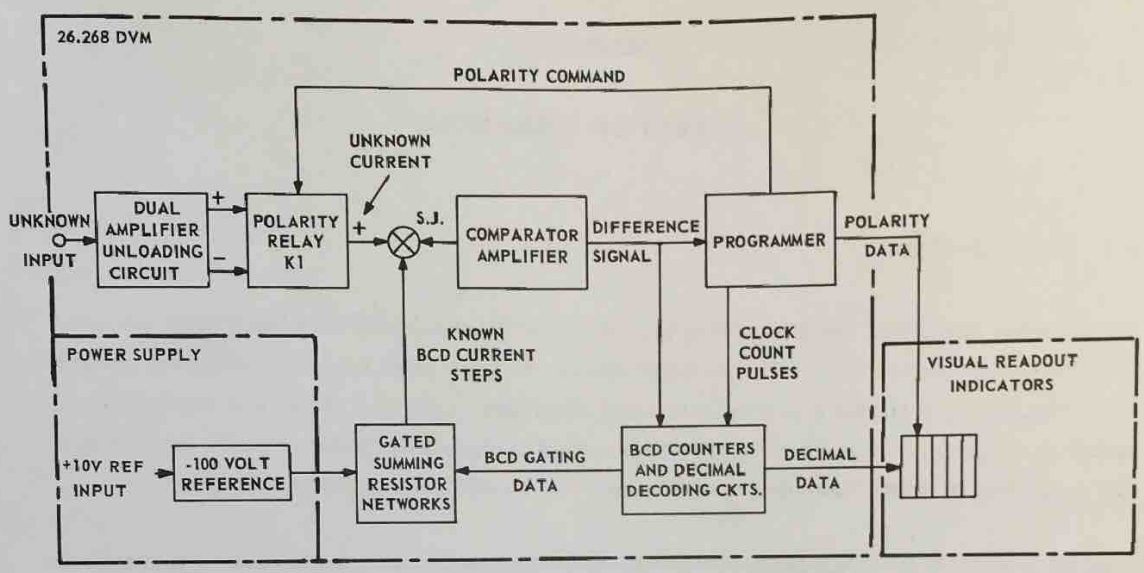


Figure 3.1. DVM, Model 26.268, Block Diagram

from one of the two input amplifiers. The comparator output level indicates to the programmer whether the scaled unknown is positive or negative; if positive, the relay state is retained, if negative the relay is switched to its opposite state. Drive transistors on the programmer provide the output polarity indication for the DVM display. Once the polarity relay is properly set, the programmer starts the comparison sequence by sending count pulses to the BCD counters. There are four cascaded BCD counters, each controlling the gates of a set of weighted resistors. Each resistor set controls current flow from a known negative voltage source in BCD steps. In addition, each of the four resistor sets differs by an order of magnitude from the next lower set.

The BCD counters release the gates of the weighted-resistor sets and apply current from the negative source in known BCD steps. This current is compared to the current from the scaled positive representation of the unknown input. The counters release the current through the most significant bit-weighted resistor of the highest-order resistor set first (8000 bit), then the next most significant resistor gate of that set (4000 bit) and subsequently the 2000 bit and the 1000 bit as the lowest of that set. The next order counter then releases its most significant weighted resistor gate (800 bit), followed by the remaining resistors in that set. The counting sequence thus proceeds through all the resistors in the four sets in the same order.

As each gate is opened the comparator indicates to the BCD counters whether the current from the known or from the unknown is the larger. If the *unknown* current is larger, the opened gate

remains opened (its counter remains on) when the next gate is released. If the *known* current is larger, the gate is closed (its counter turned off) when the succeeding gate is opened. Using this programmed-comparison sequence of operation, the known and unknown currents are brought into agreement in magnitude.

The counters that are still on when agreement is reached and the counting cycle is completed, contain in BCD count the magnitude of the unknown input. This data is decoded into the decimal form to be displayed as the magnitude of the unknown input on the visual readout.

3.3 DVM CIRCUIT DESCRIPTIONS

Functional Schematic Diagram D026 268 0S (Sheets 1, 2, and 3) in Appendix 2 is used as the basis of the DVM circuit description. This diagram is supplemented by detailed schematic diagrams of each etched-circuit card, also in Appendix 2. In addition, a logic flow diagram, a timing diagram, and simplified schematic diagrams are incorporated within the text.

The DVM circuit description is described assuming the DVM is measuring an input voltage of +4.507 volts. In order to enable the reader to more easily follow the digitizing sequence of the DVM, the input unloading amplifier circuits, and the comparator and gated resistor matrix are briefly described first.

3.3.1 Unloading Amplifiers

Figure 3.2 is a simplified schematic of the unloading amplifier circuit of the DVM. The dual amplifier configuration permits the DVM to measure both positive and negative inputs, and also provides the high input impedance of the DVM readout system. The gain of amplifier A is normally 1.25, thus permitting unloading of the input circuit. When a D/10 readout is required, an external connection is completed between pins 3-H and 3-K of J1, changing the gain of amplifier A to 0.125. The gain of amplifier B is unity; therefore, both amplifiers provide scaled outputs of the unknown (equal in magnitude but of opposite polarity) to the K1 polarity relay. The amplifier A output is applied to K1-6, the amplifier B output is applied to K1-5. During the *Zero Set* and *Sign Check* sequence in the DVM operation (described later in the text), the position of the K1 armature is set so the positive scaled representation of the unknown is applied to the comparator summing junction.

An anti-saturation network is provided around amplifier A to prevent saturation of this unit during overload conditions. This decreases the amplifier recovery time when the overload is removed.

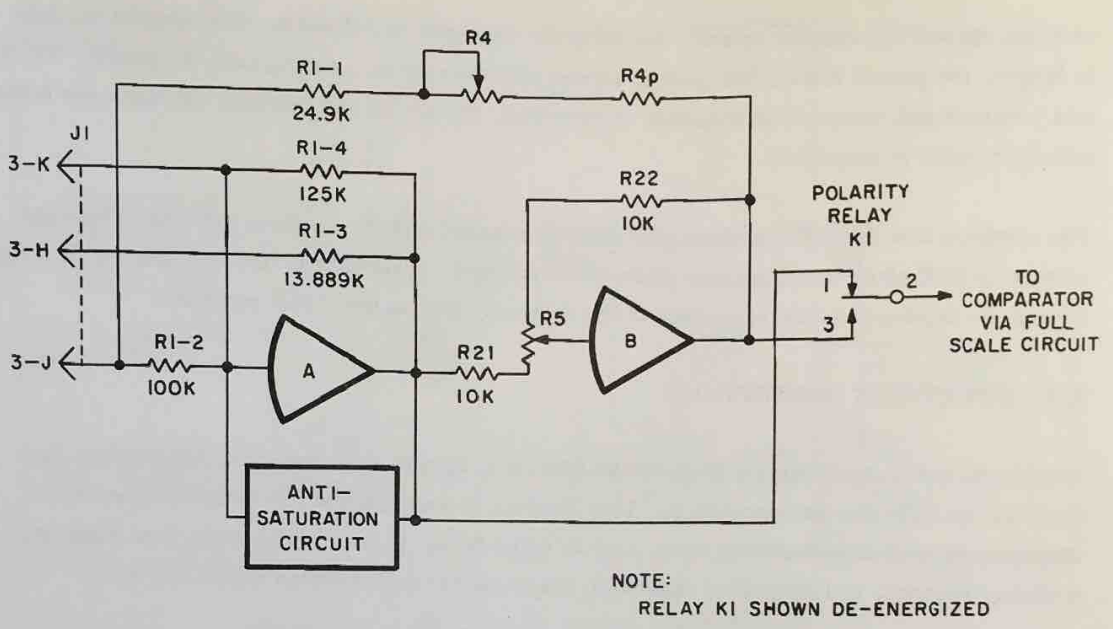


Figure 3.2. Input Unloading Amplifiers, Simplified Schematic

3.3.2 Comparator Amplifier and Gated Resistor Matrix

The comparator amplifier is a high-gain unit sensitive to the polarity of the source of the comparator summing junction current. It consists of a four stage differential amplifier (Q1 through Q4 of the 26.240) and two cascaded output stages, Q5 and Q6. The output stages operate at either saturation (0 volt out) or at cutoff (-14 volts out) in response to the polarity of the summing junction current source; the output of Q5 is the Comp + output and that of Q6 the Comp - output. The two outputs are opposite in phase. The DVM only uses the Comp - output (referred to hereafter as the *comparator output* or *Comp Out).*

The comparator output is negative (-14 volts) when the comparator summing junction current is due to a positive polarity source, and the output is positive (0 volt) when the summing junction current is due to a negative polarity source.

In addition to the output of one of the dual dc amplifiers (via K1), the gated resistor matrix is also connected to the comparator summing point. The gated resistor matrix is provided with a -100 volt reference source. The polarity of the comparator output indicates whether the current due to the unknown at the summing junction is larger (negative comparator output) or if the matrix current is larger (positive comparator output or zero volt level).

The current from the negative reference source is divided into binary-coded decimal steps by the use of matched resistor sets. A typical example is illustrated in Figure 3.3 which shows four resistors, each gated, and each gate controlled by a separate BCD counter. (The BCD counters of the 100's decade are shown in this illustration.) The 125K resistor permits eight times the current flow as that permitted by the 1 megohm resistor and so on in the ratio of 8:4:2:1 as indicated by the parenthetical notations in Figure 3.3. If three more sets of four resistors (each set ratioed to the next by an order of magnitude) are added to this group and controlled by the 1000's, 10's and 1's counter, then the BCD count of each decade of the DVM will determine the precise current flow from the negative source to the comparator summing point.

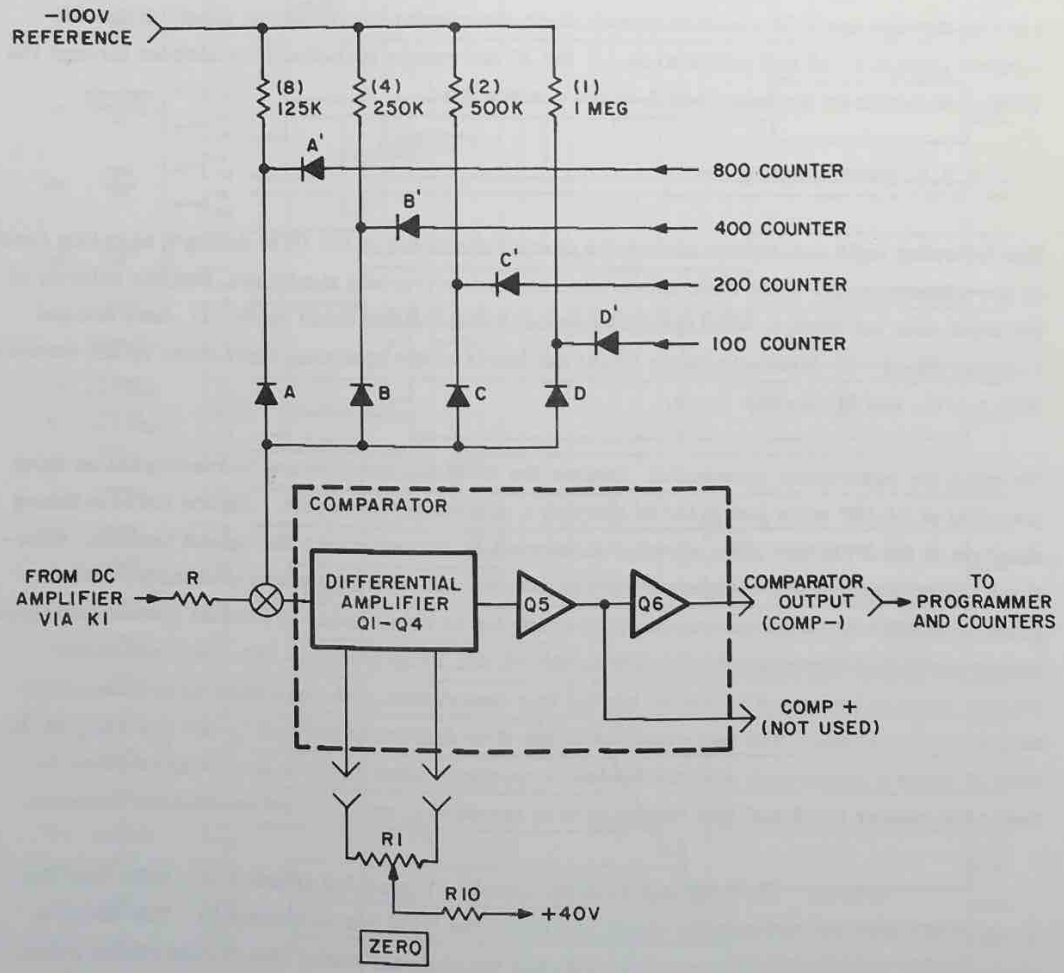


Figure 3.3. Comparator and Typical Gated Resistor Matrix, Simplified Schematic

The current from the -100 volt reference source is compared to that from the positive representation of the unknown input at the comparator summing junction. The larger of the two, by determining the comparator output polarity, permits the DVM to bring the reference current into agreement with the unknown current.

When this state is attained, the count in the BCD counters is the numerical equivalent of the unknown input magnitude in binary-coded decimal form.

The counters control the reference current flow to the comparator summing junction by either forward biasing or reverse biasing the diode gates of the resistor matrix. For example, if the 800 counter applies a +2 volt potential to diode A', then diode A is forward biased and the current through the 125K resistor cannot reach the comparator summing point. If the 800 counter applies a -10 volt potential to A', the A' is reverse biased and the current through the 125K resistor flows through diode A to the comparator.

3.3.3 DVM Sampling Cycle

The following logic description covers the overall operation of the DVM during a sampling cycle of the unknown input. This description assumes, as previously mentioned, that the polarity of the input does not change. The operating cycle is divided into three parts: 1) *Zero Set* and *Polarity Check* 2) *Digitizing Cycle* (these two parts of the operating cycle make up the conversion cycle), and 3) *Display Cycle*.

To make the description meaningful, assume the DVM has sampled and is reading out an input potential of +4.507 volts just prior to starting a new conversion cycle. Figure 3.4 is a timing diagram of the DVM operation showing waveforms at various points throughout the unit. (Portions of the diagram are exaggerated for clarity and all waveshapes are idealized.) The diagram is divided into time increments across the top in relationship to the fast (or *master)* clock pulses generated by oscillator Q11-Q12 on the 44.302 Programmer. The frequency of the master clock is between 8 kc and 10 kc; for this description each time interval is assumed to be 100 microseconds. The one exception is the time increment between t_o and t'_o. The $'_o$ is the time at which a conversion command pulse is received; since there is no synchronization between the master clock and this command it is assumed t_o and t'_o do not necessarily coincide.

3.3.3.1 *Zero Set and Polarity Check.* Figure 3.5 (Part 1) is a logic flow diagram of the zero set and polarity check portion of the DVM conversion cycle. The *hexagon* shaped block indicates interconnections between the diagram parts; like numbers form a continuous path. *Diamond* shaped blocks are *decision* blocks indicating where a choice of two conditions may occur; the decisions made by the DVM are for the most part dependent on the

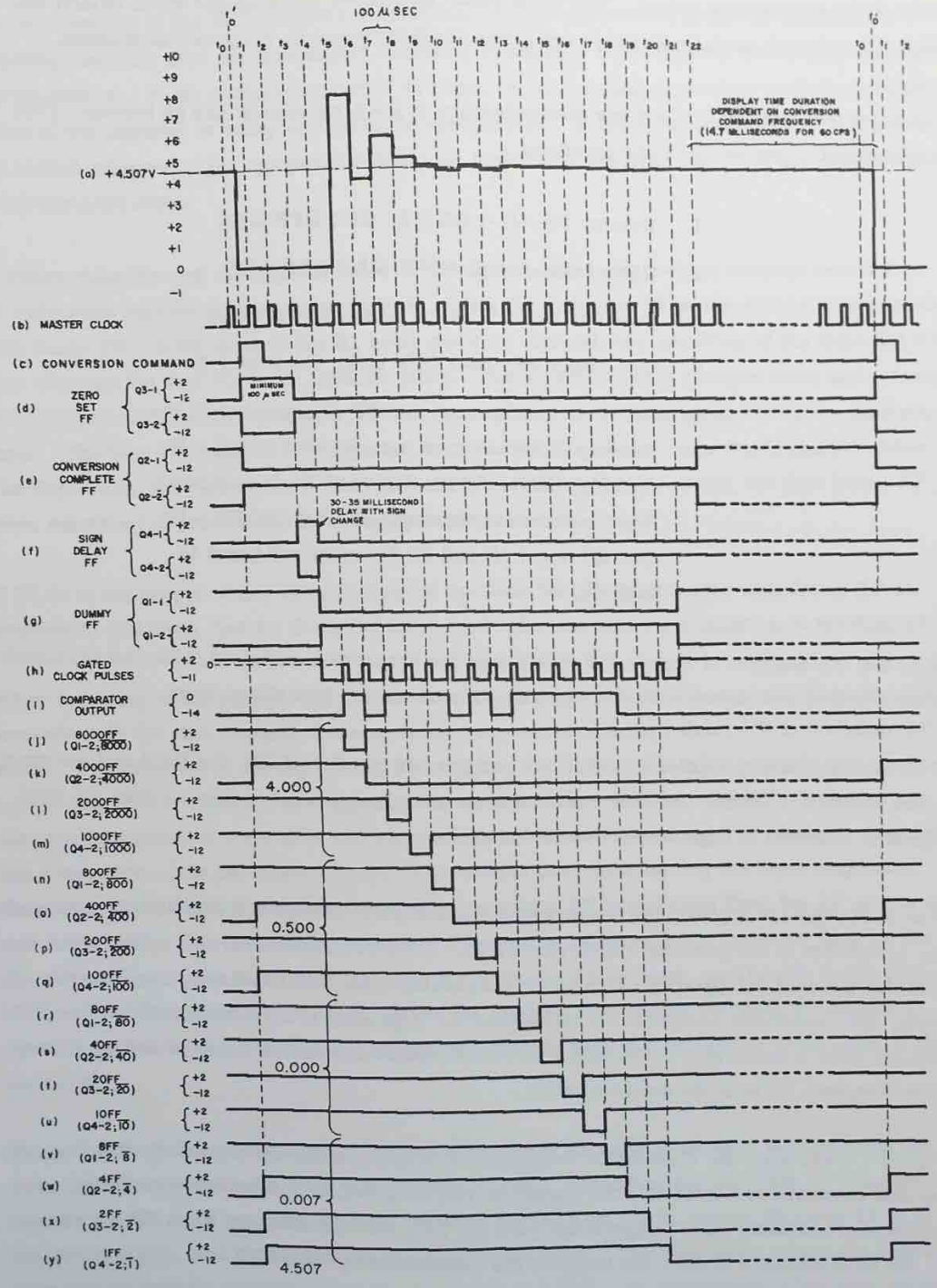


Figure 3.4. DVM Timing Diagram

state of the comparator output. The *rectangular* blocks are *event* blocks which briefly describe the circuit operations; these are generally determined by the previous decision.

The quiescent state of the bistable multivibrators of the programmer are as follows: (The levels listed in parentheses are idealized.)

1. Dummy FF: Q1-1 ON (+2); Q1-2 OFF (-12)
2. Conversion Complete FF: Q2-2 OFF (-12)
3. Zero Set FF: Q3-1 OFF (-12); Q3-2 ON (+2)
4. Sign Delay FF: Q4-1 OFF (-12); Q4-2 ON (+2)
5. Sign FF: The state of this FF is dependent on the polarity of the unknown input; if Q5-1 is ON (+2) the relay driver Q6 conducts and K1 is energized (input unknown is negative), if Q5-1 is OFF (-12) then Q6 is cut off and K1 de-energized (input is positive).

Note that the diagram of Figure 3.5 starts with the conversion command pulse and is immediately followed by a decision block regarding the state of the hold signal input.

If an external hold is applied (a -12 to -25 volt level at pin 2-X of J2), the DVM will not start a new conversion cycle. Another conversion command pulse must be applied after the hold signal is removed to begin a new conversion cycle.

If no hold signal is applied, the conversion command pulse passes to a decision block regarding the completion of the previous conversion cycle. If the previous conversion cycle (which only includes the zero set-polarity check and the digitizing cycle, not the display cycle) is not complete, the Conversion Complete FF will inhibit the triggering of the Zero Set FF*. The DVM will not start a conversion cycle until a new conversion command is received and the Conversion Complete FF is in its quiescent state.

Figure 3.5 assumes the Conversion Complete FF is in the quiescent state at t'_o when the conversion command is received. The answer to this decision, therefore, is yes and the conversion command pulse triggers the Zero Set FF. As indicated, the Zero Set FF resets all the BCD counters to zero and triggers the Conversion Complete FF.

**Provided the conversion command signal does not exceed 12 volts in magnitude.*

The zero setting of the BCD counters removes all reference current from the comparator summing junction; thus the comparator summing junction is controlled by the scaled unknown representation. If the comparator output is negative, it indicates a positive scaled representation of the unknown is being applied to the comparator. If the comparator output is positive, the scaled unknown on the comparator summing junction is negative and relay K1 must be set to the opposite state.

In either case the next clock pulse (after a 100 microsecond delay which assures removal of all reference current from the comparator) resets the Zero Set FF which in turn triggers the Sign Delay FF. If the state of the K1 relay must be changed, the resetting of the Zero Set FF also triggers the Sign FF to its opposite state. The sign relay (K1) changes state and selects the output of the amplifier that will provide the scaled positive representation of the unknown input. The Sign FF, when it is triggered, triggers the Sign Delay monostable multivibrator. The Sign Delay mono provides a 30 to 35 millisecond delay (by preventing the Sign Delay FF from resetting) to provide the K1 relay operating time.

If K1 is in the proper state, the resetting of the Zero Set FF triggers the Sign Delay FF as previously indicated, but the Comp Out level (-14 volts) inhibits the triggering of the Sign FF.

After the delay of the sign circuit (100 microseconds without a sign change and 30 to 35 milliseconds with the sign change), the next clock pulse resets the Sign Delay FF to its quiescent state. The resetting of the Sign Delay FF triggers the Dummy FF to its opposite state. Each conversion cycle is started by triggering the Zero Set FF. The Zero Set FF, however, returns to its quiescent state after 100 microseconds. Should it be triggered again, it would stop the conversion cycle and restart a new cycle without ever determining the input magnitude. To prevent such false starts, the Conversion Complete FF inhibits the Zero Set FF conversion command input. The Conversion Complete FF itself is inhibited from resetting first by the Zero Set FF, then the Sign Delay FF when the Zero Set FF is reset, and finally by the Dummy FF when the Sign Delay FF is reset. Since the Dummy FF remains ON until the digitizing cycle is complete, the Zero Set FF cannot be triggered until the magnitude of the input is determined.

Thus, the Zero Set and Sign Check portion of the DVM conversion cycle is started when the Zero Set FF is triggered setting the counters to zero. Resetting the Zero Set FF triggers the Sign Delay FF which provides a sufficient delay for the Sign FF to trigger (if relay K1 is in the wrong state), and in turn trigger the Sign Delay mono. The Sign mono delays the operating sequence to provide operating time for the sign relay (K1). On completion of the sign check (and relay state change if required), the Sign Delay FF is reset. This triggers the Dummy FF which signals the beginning of the digitizing portion of the conversion cycle.

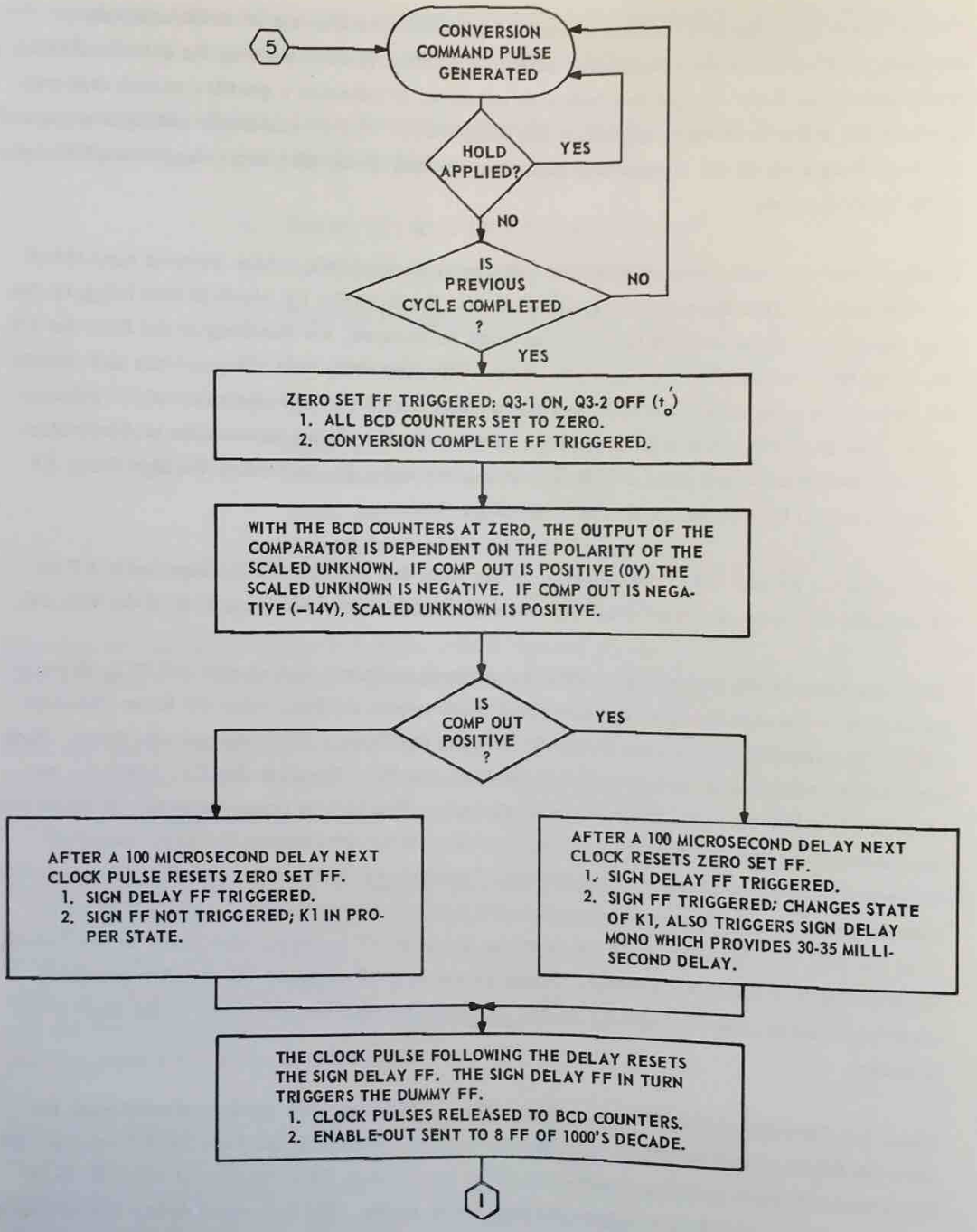


Figure 3.5.1. (Part 1) DVM Logic Flow Diagram (Zero Set and Polarity Check)

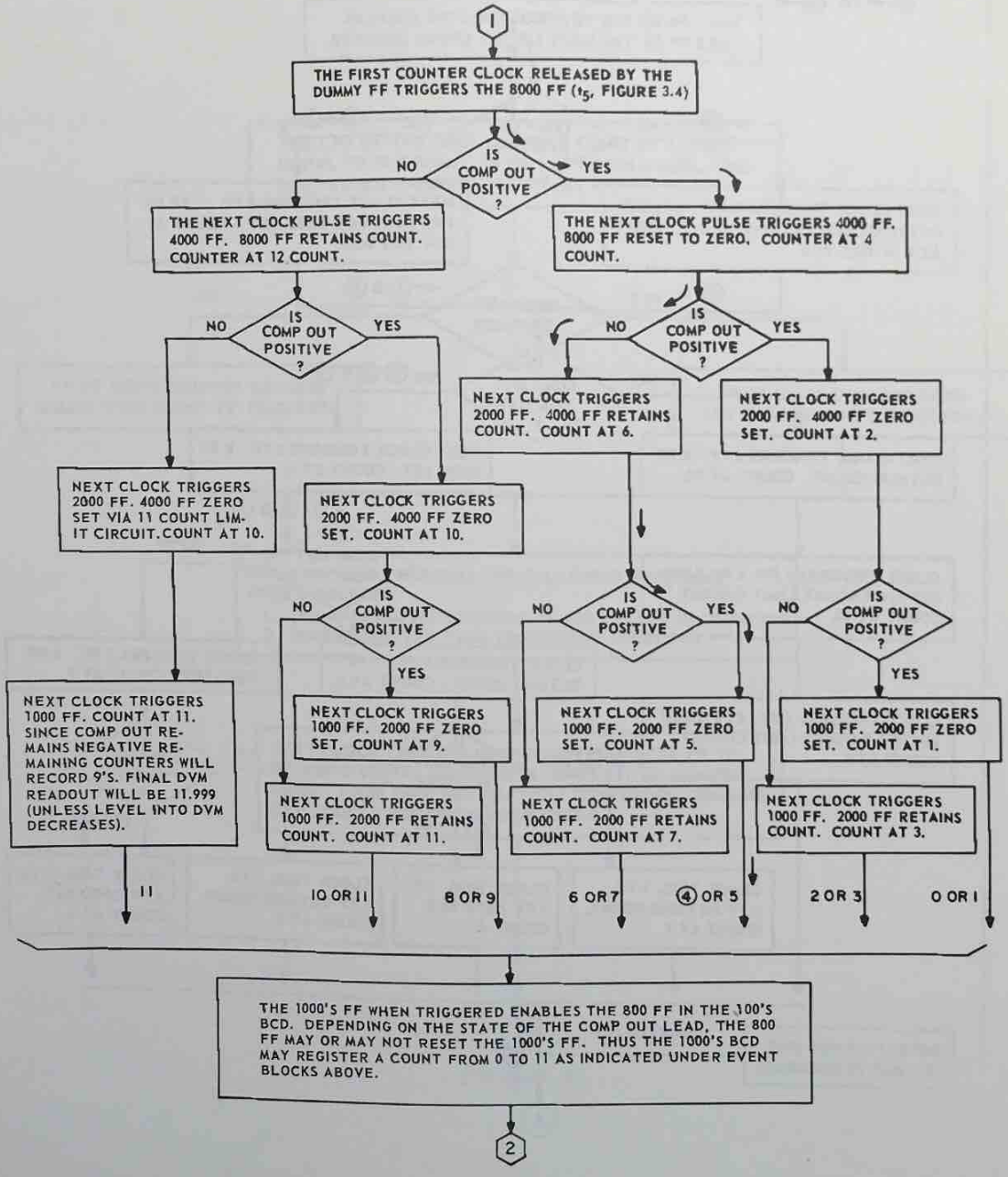


Figure 3.5.2. (Part 2) DVM Logic Flow Diagram (1000's BCD Operation)

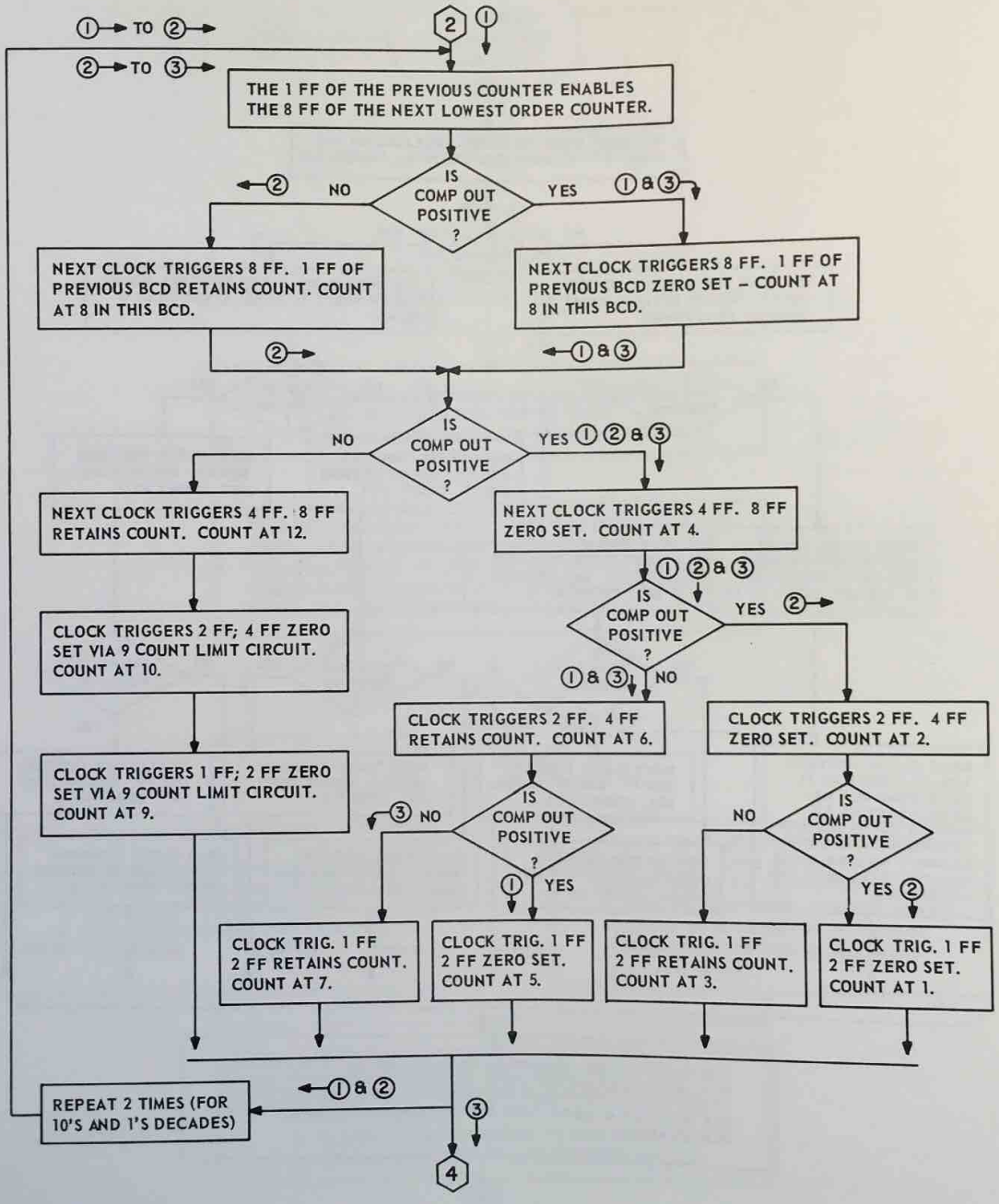


Figure 3.5.3. (Part 3) DVM Logic Flow Diagram (100's, 10's, and 1's BCD Operation)

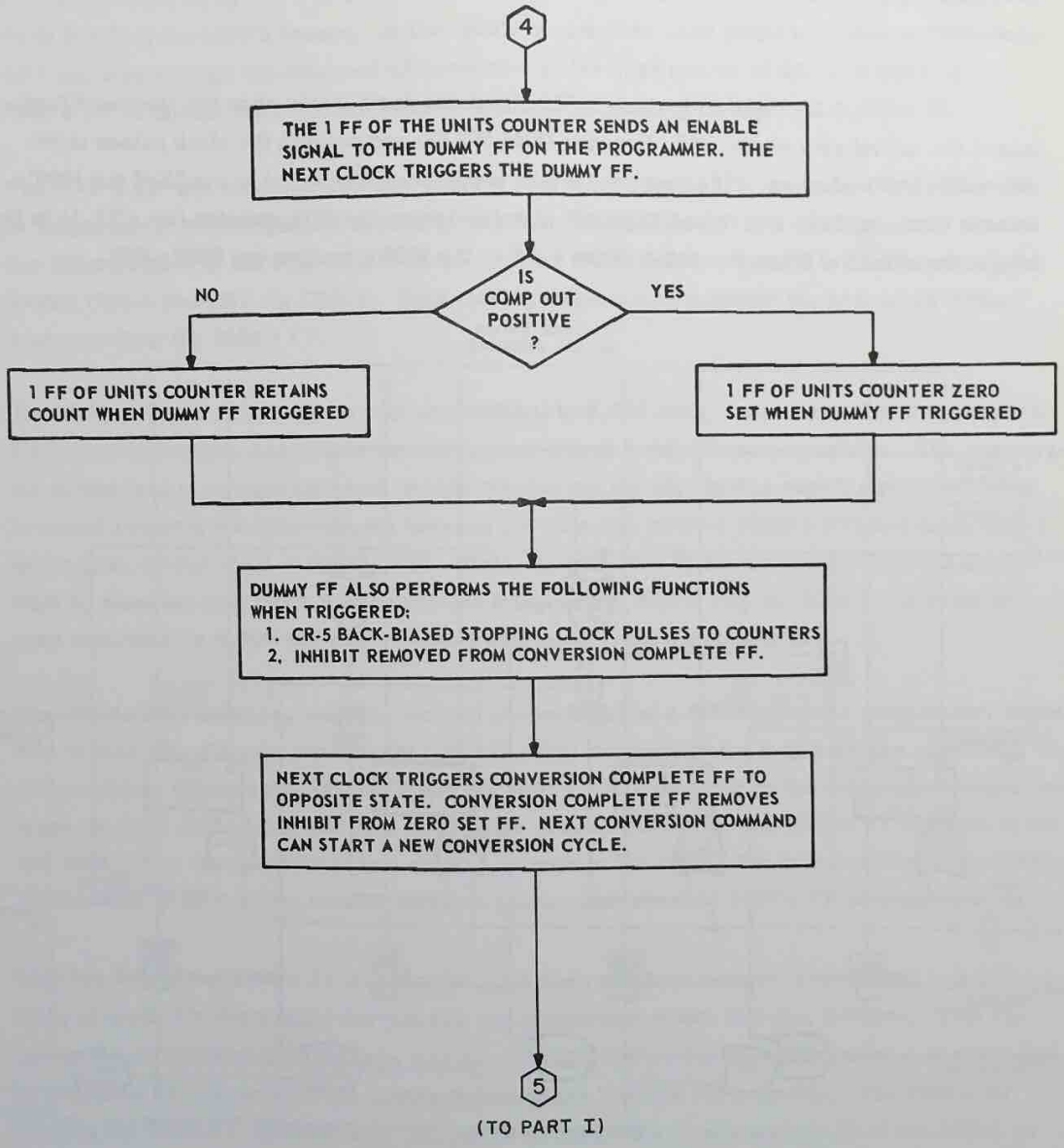


Figure 3.5.4. (Part 4) DVM Logic Flow Diagram (Completion of Conversion Cycle)

The Dummy FF sends an enable signal to the 8 FF in the 1000's decade and also releases count pulses (master clock pulses) to all of the counters. The triggering of the Dummy FF starts the digitizing process of converting the dc analog input magnitude to the binary-coded decimal equivalent.

3.3.3.2 *Digitizing Cycle.* The digitizing cycle starts when the Dummy FF releases the inhibit gate (diode CR1, Drawing D044 302 0S) and permits the clock pulses to be sent to the BCD counters. The Dummy FF also sends an enable signal to pin 22 of the 1000's counter (Drawing D038 032 0S and Figure 3.6) and releases the differentiator (via CR4-1) in the trigger input lead of transistor Q1-2 of the 8 FF in the 1000's counter (or 8000's FF).

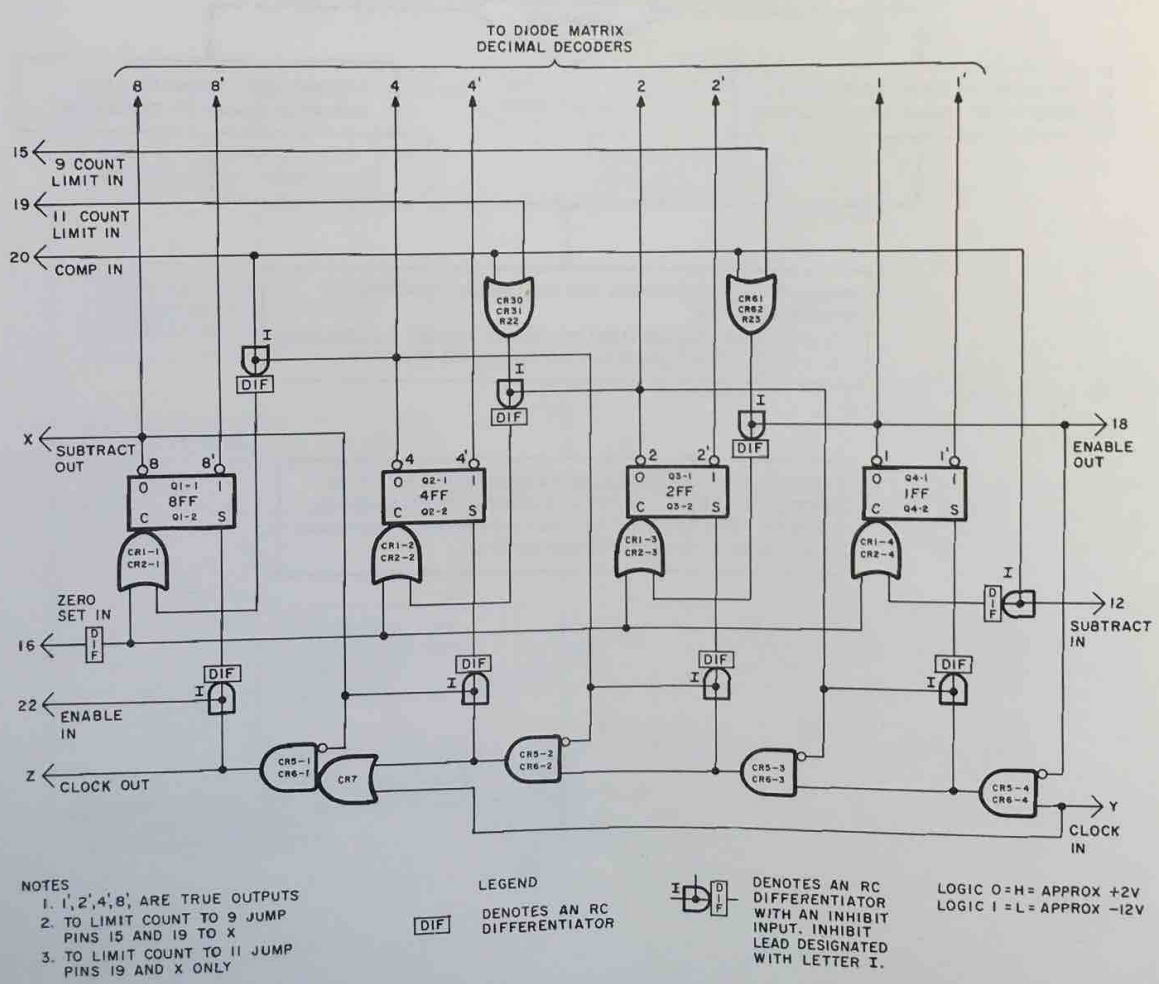


Figure 3.6. Typical BCD Counter Circuit

At time t_5 of Figure 3.4, which assumes no polarity change, the first such clock pulse is sent out of the programmer to pin Y of the 1's BCD (line h). It is shunted through this counter via CR7 and out Pin Z, in Pin Y of the 10's counter, through CR7 and out Z of this counter and so on to Pin Y of the 1000's decade. In the 1000's decade this clock pulse also passes through CR7 and then through the released differentiator in the base circuit of Q1-2, triggering the 8000's FF to the ON state (as indicated by the first event block of Figure 3.5, Part 2).

The 8000's FF will release reference current (Curve a, Figure 3.4) equivalent to 8.000 volts in magnitude to the comparator summing junction. The 8000's FF in triggering also releases the differentiator in the base circuit of Q2-2 of the 4000's counter (via CR4-2) and back biases diodes CR6-1 and CR7 via CR5-1. Back biasing these diodes prevents the next clock pulse from reaching the 8000's FF.

The 8000's FF, in releasing current proportional to 8.000 volts, takes control of the comparator summing junction and causes the comparator output level to become positive. The comparator output lead is brought into each decade counter via pin 20. In this case the positive Comp In signal releases the differentiator between the collector of Q2-1 (4000's FF) and diode CR2-1 in the base circuit of Q1-1 (8000's FF). Thus, as indicated by the arrows on Figure 3.5, Part 2, when the next clock is received and triggers the 4000's FF, the 8000 FF is reset to zero removing its 8.000 volt current-level equivalent from the comparator.

The 4000's FF, however, releases current proportional to 4.000 volts to the comparator. Since this is less than the unknown current (+4.507 volts) the comparator output swings negative. The differentiator between the 2000's FF and the 4000's FF is inhibited by the comparator output and when the 2000 FF is triggered by a clock pulse at t_7 (Figure 3.4), the 4000's FF remains in the ON state. The count continues in a similar manner to the 1000's FF; in this example the 2000's FF is reset to zero so the counter contains a five count when the 1000's FF is triggered.

With the 4000's and 1000's FF's in the ON condition reference current proportional to 5.000 volts is applied to the comparator causing the comparator output to swing positive. This releases the differentiator in the base circuit of Q4-1 (1000's FF); this differentiator is connected to the 800's FF via pin 12 of the 1000's decade to pin X of the 100's decade. The 1000's FF enables the 800's FF differentiator (via pin 18 of the 1000's decade and pin 22 of the 100's) so the 800's FF can trigger. In this example, when the 800's FF triggers, the 1000's FF is zero set.

As indicated on Figure 3.5, Part 2, with the 1000's FF in the ONE state the 1000's decade may contain counts of 1, 3, 5, 7, 9, or 11. Depending on the state of the comparator output,

the 1000's FF may or may not be zero set when the 800's FF triggers. Indicated *under* the last row of event blocks are the possible resultant counts of 1000's BCD counter (from 0 to 11) when the 800's FF triggers. The circled 4 indicates the final count of the 1000's counter for the assumed +4.507 volt input. Figure 3.5, Part 3, illustrates the operation of the 100's, 10's, and 1's counters. The operation of these counters is similar except their count is limited to a maximum of 9. This is accomplished by jumpering pins 15, 19, and X of each individual counter. Thus, if the 8 FF is ON and the 4 FF does not reset it to zero, the 2 FF automatically zero sets the 4 FF via the differentiator enabled by the 8 FF through pin 19. In the same manner, the 1 FF automatically zero sets the 2 FF (if the 8 FF is ON) via the differentiator, enabled through pin 19.

The path indicated by the circled 1 is the sequence of events of the 100's counter with the DVM measuring +4.507 volts. The circled 2 and 3 indicate the sequence of events taking place in the 10's and units counters respectively.

The programmer Dummy FF acts as a counter FF with respect to the 1's decade 1 FF as shown on Figure 3.5, Part 4. The 1's FF enables the Dummy FF; when the Dummy FF triggers, it sends a subtract pulse to the 1 FF which zero sets this FF if the comparator output is positive. In this example where the DVM is measuring +4.507 volts the 1's FF remains in the ONE state.

The Dummy FF indicates the end of the conversion cycle; it back biases diode CR-5 on the programmer preventing any further clock pulses from reaching the counters. It also removes the inhibit signal from the Conversion Complete FF. Thus, the next clock pulse resets the Conversion Complete FF ending the conversion cycle. As indicated on Figure 3.5, Part 4, the resetting of the Conversion Complete FF removes its inhibit signal from the Zero Set FF and returns the event sequence to Figure 3.5, Part 1.

In summary, the digitizing cycle starts with the enabling of the 8000's FF by the Dummy FF. Each counter is triggered in sequence starting with the 8000's FF and on through the 1's FF. As each FF triggers, it releases reference current to the comparator summing junction in proportion to the FF order of magnitude. The reference current is continuously compared to the scaled-unknown current and, by trial and error, the FF counts are either retained or reset to zero until the scaled unknown and reference currents are in agreement. The Dummy FF stops the counting procedure, and the Conversion Complete FF, when triggered, indicates the end of the conversion cycle. The DVM is then ready to re-cycle (t_{22}, Figure 3.4).

3.3.3.3 *The Display Cycle.* The length of the display cycle is dependent on the frequency of the conversion command pulse source. For example, if the 60 cps trigger

is used the display time will be 14.7 milliseconds. The DVM can also be triggered by an external source; in this case the readout is displayed until a new conversion command is received.

The readout display essentially starts at time t_{22} when the Conversion Complete FF triggers and the final count of the BCD counters is determined. Actually, the decoding matrix which controls the light drivers responds to each change in BCD count; however, since each decade is completed in approximately 400 microseconds, the lamp filaments do not have time to respond to each count change. In addition, since the entire conversion cycle is completed in two milliseconds and the minimum display time with the 60 cps trigger is 14.7 milliseconds (18 milliseconds for a 50 cps rate) the readout will appear as a continuous display (assuming a stable input).

Figure 3.7 illustrates the logic circuits of the BCD decades for converting the BCD count to the common decimal equivalent and also shows the display lamp drivers. Drivers Q7 and Q8 and their associated AND gates are only required for the 1000's counter to permit registering an 11 count. For this same reason Q17 and Q18 are OR gated to permit them to indicate the proper digit when the count is 0, 1, 10 or 11. All four BCD cards have this overrange capability and any one may be placed in the 1000's decade position or vice-versa for trouble analysis. (The 1000's card should be returned to its own position, A4, since this unit is used to drive two display lamps at all times. Continuous use in one of the other positions may have adverse effects on the display-lamp life.)

The AND gates of Figure 3.7 consist of diodes which in the forward biased state prevent the corresponding lamp driver from illuminating the associated lamp. As an example of the decoding operation assume the counters of Figure 3.7 have registered a binary 6 count. The collectors of transistors Q1-1 (8 FF), Q2-2 (4 FF) and Q4-1 (1 FF) are negative for a 6 count. These negative potentials are applied to the various diode AND gates of Figure 3.7. Note that the only AND gate with all negative inputs is the gate associated with Q12, the 6 lamp driver.

3.4 POWER SUPPLY CIRCUITS

Drawing D026 268 0S, Sheet 4, in Appendix 2 is the overall schematic diagram of the power supply. Detailed schematics of the 43.141 Regulator (D043 141 0S) and 6.736-1 Reference Amplifier (D006 736 0S) are also provided in Appendix 2.

The -100 volt reference supply consists of the 6.736-1 Reference Amplifier and a stable voltage source provided by the Model 680 Computer (+10 volts reference). The computer reference is

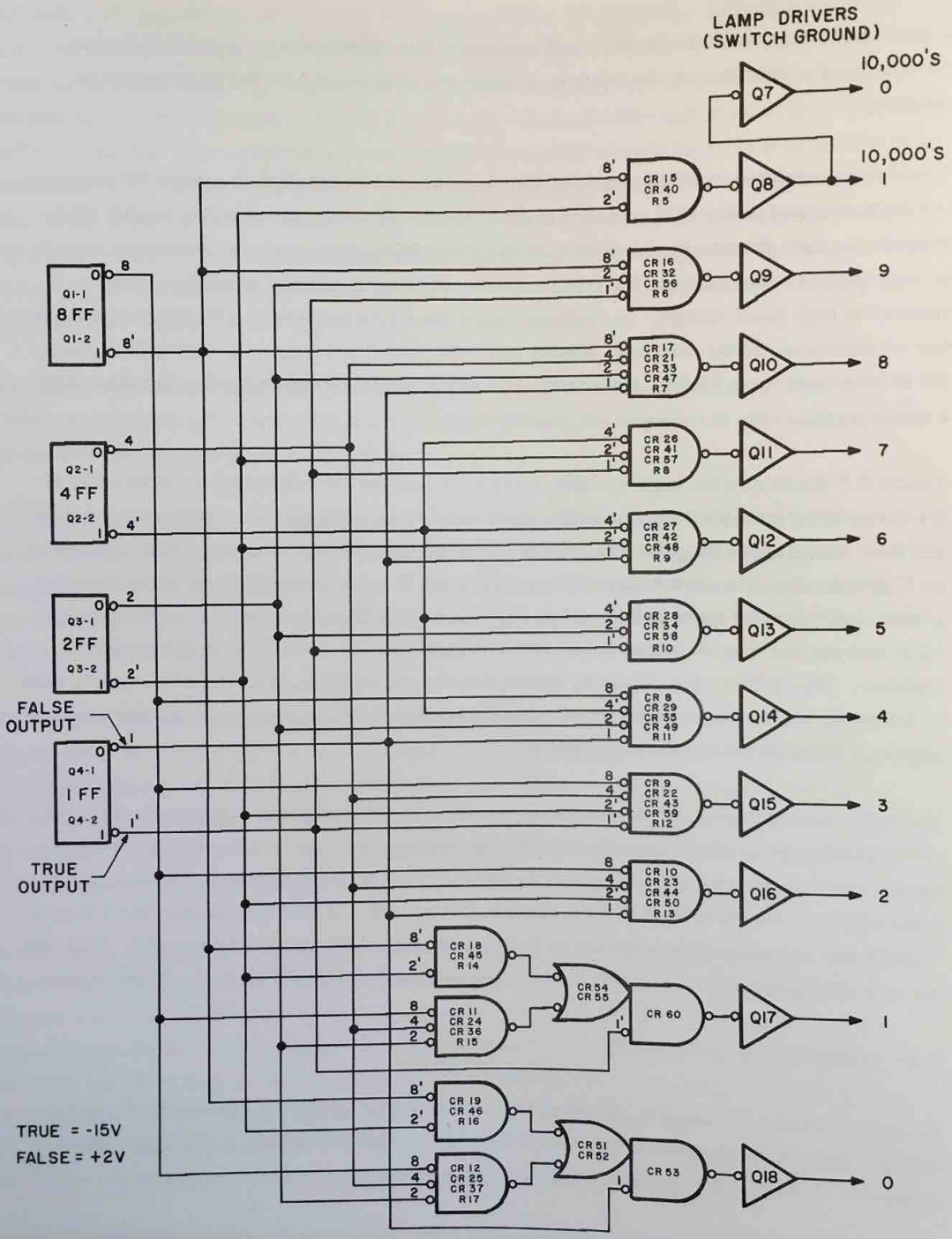


Figure 3.7. Decoding Matrix and Light Drivers, Logic Diagram

applied as an input to a 100 volt amplifier (6.736-1). Any variation in the -100 volt output (referenced to the computer +10 volts) will cause the amplifier to increase or decrease the output level due to negative feedback, thus maintaining an accurate -100 volt reference level. In addition, a variation in the +10 volt computer reference will cause a proportional change in the -100 volt reference. Thus the DVM readout will be relative to the +10 volt computer reference level. A slight increase or decrease in the computer reference level, therefore, will not affect the *relative* overall accuracy of the DVM readout.

The remaining circuits of the power supply are standard full-wave rectified series-regulated units.