Introducing....

PEAC

A low cost, general purpose analogue computer of modern design, intended for the amateur or student.

A useful tool which is capable of solving complicated problems at high speed.

Can be used as a model to simulate mechanical systems and electronic networks.

Extends enormously the scope of the amateur experimenter.

This series of articles will explain in detail the design, construction, and operation of PEAC.

ANALOGUE

MOST of the publicity afforded to computers favours digital equipment. However, digital methods tend to be disproportionately expensive for small installations. On the other hand, although analogue equipment is ideally suited to limited, low-cost applications, it was not until the silicon transistor had become firmly established, and enough practical published information was available, that a start could be made on designing analogue computing equipment to yield a reasonable standard of performance in the lowest possible price range.

A WORTHWHILE PROJECT

No doubt many readers will think that construction of a true computer could involve them in a great deal of time, money, and effort. They might also believe that an average understanding of mathematics would not be sufficient to equip them to operate a computer effectively. However, the amount of time and money spent building PEAC need be no more than is consumed by a home constructed hi fi outfit of normal proportions and performance, and the computer will solve even simple problems a great deal faster than the human mind or slide rule, once it has been programmed to do so.

In fact, a general purpose computer can find application in almost every sphere of technical activity, and is particularly useful in the electronic workshop, to the point of becoming indispensable after a short period of use.

UNIT CONSTRUCTION

PEAC is arranged in the form of units, and is organised in such a way that reasonably advanced computations may commence upon completion of the first unit, UNIT "A". The cost of building UNIT "A", based upon typical retail prices at the time of writing, will not be much above £25, and yet it will solve algebraic polynomial equations, simultaneous linear equations, simple differential equations, and can also be used to simulate the behaviour of many elementary mechanisms and electronic networks.

UNIT "A" is designed primarily to satisfy a minimum user requirement, for experimental and educational work, but it also serves as a convenient starting point for the addition of further units to expand the computer to almost any desired degree of capability and complexity. The additional facilities provided by the add-on UNITS "B", "C", and "D" are described in the specification. See also the block diagram, Fig. 1. 1.

A comprehensive PEAC installation, equipped with a function generator and multiplier, and with full integrating facilities for the fast solution of a range of differential equations, might finally cost around £60: not a lot to pay for an item of workshop equipment which can solve electronic formulae in 10ms, and which may also be employed as a variable waveform generator, 18 input high quality audio mixer, variable characteristic high Q audio filter, large inductance or capacitance simulator, d.c. or a.c. millivoltmeter, and many other things besides.

COMPARISON BETWEEN ANALOGUE AND DIGITAL COMPUTERS

Although popularly regarded as an inaccurate machine of limited usefulness, the analogue computer is to be found in the Polaris missile, spacecraft, aircraft, large scale chemical processes, and many automated production lines, quite apart from basic research work, where flexibility and ease of working are often considered to be more important than extreme accuracy. The analogue computer is, in most cases, very much faster than its digital counterpart, and can offer far more in the way of general facilities for a given outlay.

COMPUTER

By
D. BOLLEN

The time taken to solve a problem on an analogue computer is independent of problem length. All circuits operate in parallel, simultaneously. A typical solution might be arrived at in 20ms, and this solution can then be repeated at the rate, say, of 25 solutions per second. In human terms the solution is virtually immediate and continuous, therefore, any adjustments made to problem parameters (terms of an equation) while the computer is working will be immediately reflected in the solution readout. This rapid response allows the operator to quickly gain an insight into the workings and structure of a problem.

In contrast, digital computers perform many mathematical operations in a pre-determined and comparatively lengthy sequence, which bears little obvious relationship to the structure of the problem, but they do offer the very high degree of accuracy essential for calculations involving money or very precise data.

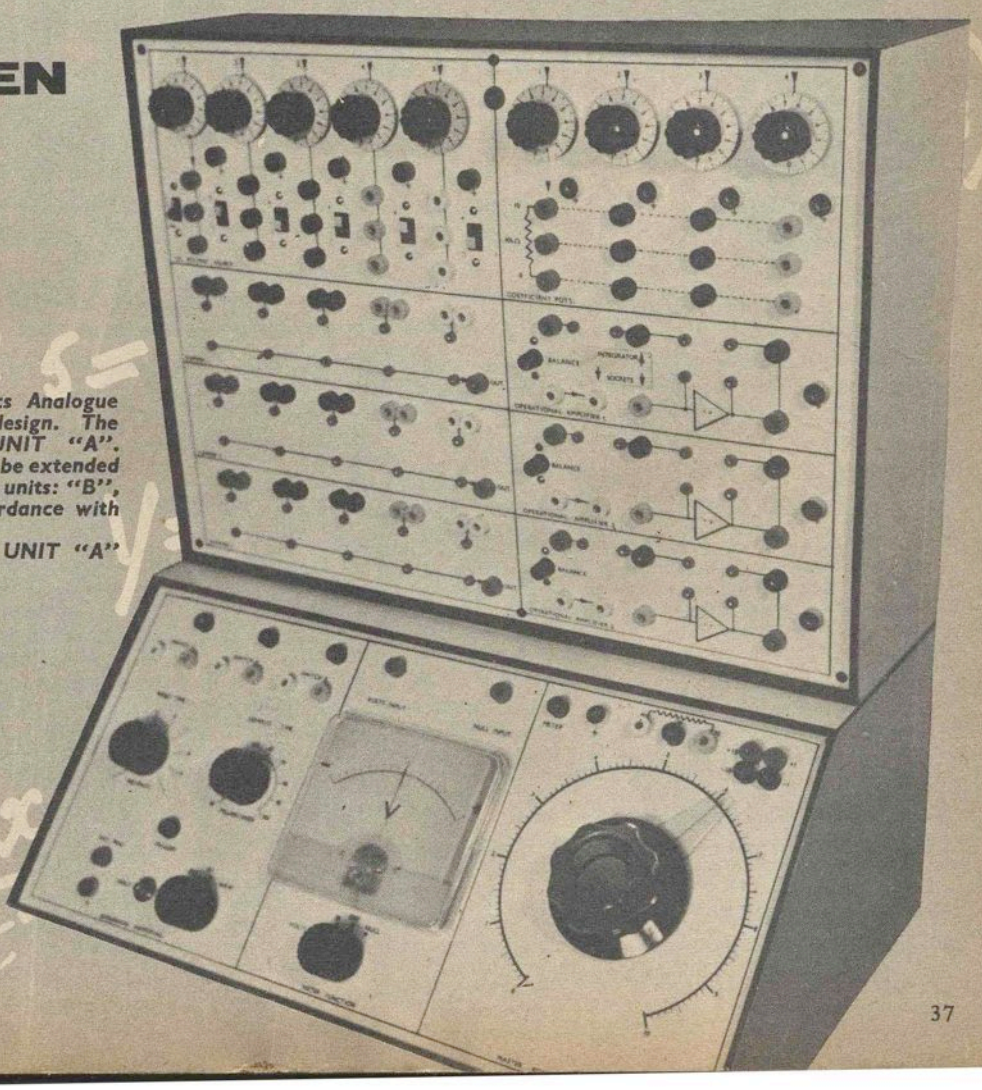
The computer of the future will undoubtedly combine the best of both worlds with analogue and digital equipment in hybrid form.

ANALOGUE METHODS

The statement that an aeroplane is a machine for solving sets of differential equations is not very far removed from the truth. If the aeroplane did not solve its equations correctly it would not be able to fly at all. Almost all relationships or events can be described mathematically, or in turn be represented by an analogy. A model aeroplane in a wind tunnel solves, by analogy, roughly the same equations which govern the behaviour of the real aeroplane, although in much simpler and less expensive fashion.

An analogy of a physical or mathematical process could be achieved by a system of gears, pulleys, and levers; or by the controlled flow of gases or liquids. But in the last couple of decades electronic methods of simulation and equation solving have become almost universal, because of the accuracy, availability, and adaptability of standard electronic components.

The main purpose of the analogue computer is to allow a model to be set up quickly and easily, to simulate the behaviour of a full scale system, and at



The Practical Electronics Analogue Computer is of flexible design. The basic equipment is UNIT "A". Computing facilities may be extended by the addition of further units: "B", "C" and "D", in accordance with user requirements.
This photograph shows UNIT "A" standing on UNIT "B"

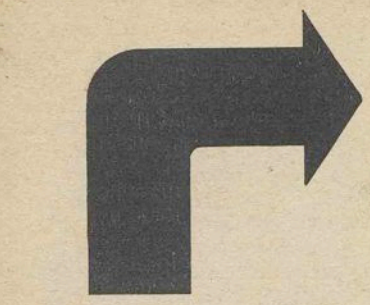
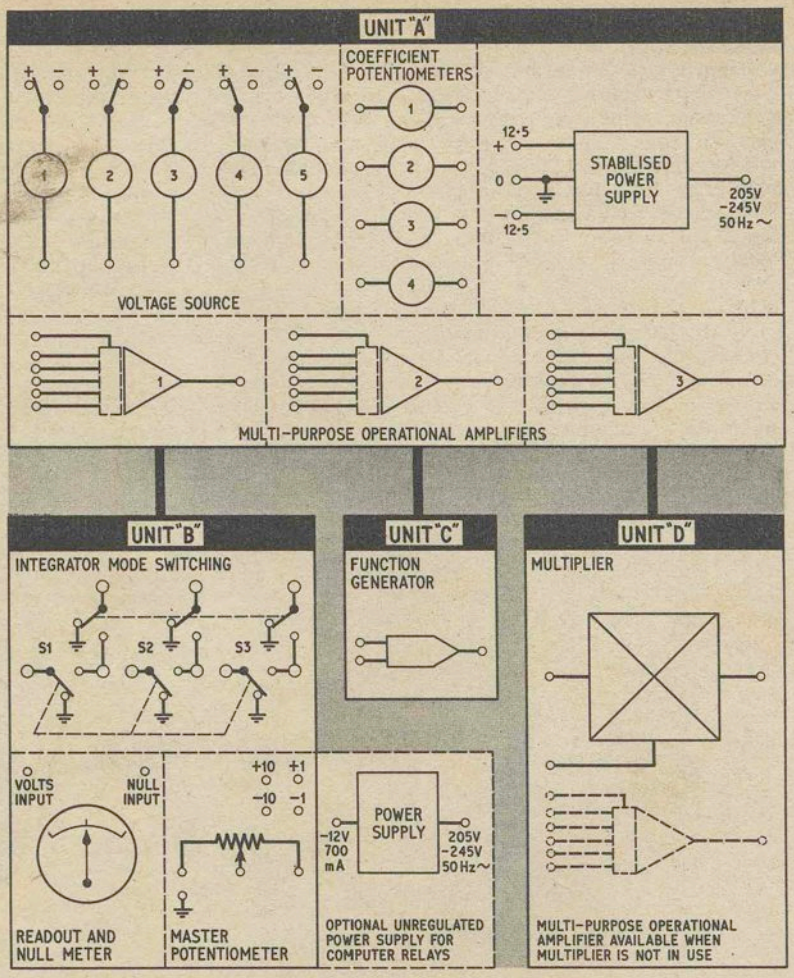


Fig. 1.1 Block diagram of

PEAC

SPECIFICATION



UNIT "A"

POWER SUPPLY

Input 205V—245V 50Hz. Output ±12·5V d.c. Voltage regulation better than 1% for loads of 0—200mA, and 2% for 0—300mA. Total ripple 2mV. Complete short circuit protection.

AMPLIFIERS

Three multi-purpose operational amplifiers, each with five silicon transistors. Open loop voltage gain greater than 5,000. Output ±10V at 5mA. Current demand (average) 40mA. Equivalent input drift under normal room conditions better than ±0·5mV per hour. Unity gain frequency response within 1% for 0—10kHz, and 5% for 0—25kHz. Typical noise and hum at output 3mV.

VOLTAGE SOURCE

Five independent outputs, each continuously variable in three steps giving ±0—0·1V, ±0—1V, and ±0—10V. Dial setting accuracy better than 3% of full scale between dial divisions 1—10. Total current demand 50mA.

COEFFICIENT POTENTIOMETERS

Four 10 kilohm 270° potentiometers. Dial setting accuracy better than 5% of full scale between dial divisions 1—10.

SUMMING NETWORKS

Three five-input summing networks provided with voltage check sockets, and plug-in computing components.

UNIT "B"

MASTER POTENTIOMETER

25 kilohm 300° wirewound; 25 watt. Two voltage measuring ranges ±0—1V and ±0—10V. Scale length 14in. Accuracy better than ±0·5% of full scale.

READOUT METER

Centre zero 100—0—100μA, calibrated 0—0·3V, 0—1V, 0—3V, and 0—10V. Accuracy better than ±2% of full scale.

INTEGRATOR SWITCHES

Provision for three or more integrating amplifiers. Compute times ranging from 10ms—1s. Single shot or repetitive mode with "hold" facility. Current demand around 65mA.

UNIT "C"

FUNCTION GENERATOR

Diode function generator for parabolic and other functions. Typical accuracy 2%. Frequency response to several kHz.

UNIT "D"

MULTIPLIER

Four quadrant multiplication of two or more variable voltage inputs. Also incorporates an operational amplifier which may be used on its own to supplement the amplifiers of UNIT "A". Frequency response generally better than 0—50Hz. Approximate current demand around 75mA.

the same time solve the equation which represents the system. Sometimes the computer will be used just for solving equations or, alternatively, as a working model only, depending on the nature of the problem. The advantage of the electronic computer is that it will do each, or both at the same time, with ease.

The computer is set up, or "programmed", for a particular task by inserting computing components, i.e. resistors and capacitors, into sockets on the front panel. This procedure will be described in full detail in due course.

ANALOGUE COMPUTER CIRCUITS

In the electronic analogue computer, the analogy is created fundamentally by manipulating sets of d.c. voltages. There is nothing to prevent a.c. voltages being used—in fact they often are—except that a.c. measurement techniques are generally less accurate at low levels than d.c. However, when simulating dynamic processes with d.c. voltages, the computer will be handling a voltage which varies with time. In this context it is more appropriate to regard a waveform, even if it is a pure sinewave, as a d.c. voltage varying with time according to a formula which describes the nature of the waveform.

The main computing element is the "operational amplifier". As far as operational amplifiers are concerned, the decibel is much too coarse a unit to use for the measurement of frequency response, so amplitude linearity is usually expressed as a percentage variation over a fairly restricted range of audio frequencies. In some cases, for example, an operational amplifier and its attendant circuits will be expected to respond to inputs from d.c. to 5kHz with an accuracy of a fraction of 1 per cent, and up to 10kHz at no worse than 1 per cent.

COMPUTING ELEMENTS

The majority of problems can be solved by the varied application of only five analogue elements, but the size of the problem to be handled will in turn depend on the quantity of elements available, and hence on the overall size of the computer.

The five computing elements are shown in Fig. 1.2, together with their conventional symbols and generalised functions. The symbols are used as a kind of shorthand when drawing up a computer programme.

The first thing to note about the simplified circuit diagrams of Fig. 1.2 is that the common earth return is often completely ignored. Computer supply voltages are usually positive and negative in relation to an earthed centre tap. Since the input and output terminals of each computing element are arranged to be very close to earth potential in the absence of an input voltage, it is feasible to take the earth rail for granted and regard all circuits as having only two terminals, instead of the usual four.

Although the symbol and function of each of the elements of Fig. 1.2 are common to all analogue computers, the actual circuit design and choice of components will naturally vary from one computer to another. For example, the time-division multiplier of Fig. 1.2e is only one among many possible circuit configurations for achieving multiplication of independent variables. Alternative approaches include the Hall effect, the servo, logarithmic, and quarter square multipliers.

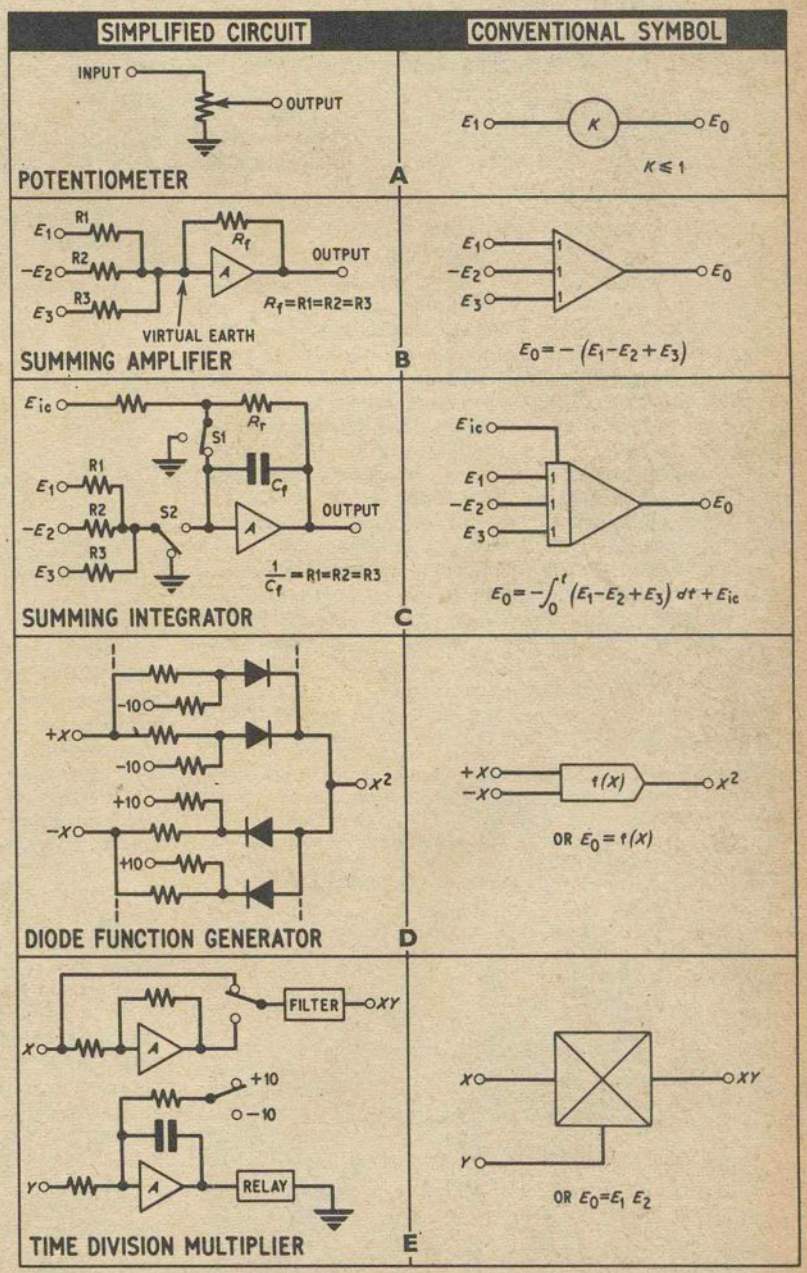


Fig. 1.2 Analogue computing elements

It is proposed to examine computing elements in greater detail when they are dealt with individually at a later stage, but in the meantime a brief survey will suffice.

COMPUTING POTENTIOMETER

The potentiometer of Fig. 1.2a may be used for multiplying a variable voltage (often called a machine variable) by a constant of less than unity.

Example: potentiometer input 1·5 volts. Slider set exactly half way along resistance track, corresponding to a constant of 0·5. Output voltage E_o therefore equals $1{\cdot}5 \times 0{\cdot}5$, or 0·75. As set, the potentiometer will multiply any input voltage by 0·5.

When incorporated in the feedback loop of an operational amplifier, the potentiometer will divide a machine variable by a constant smaller than 1. The fact that potentiometer constants are less than unity is no real disadvantage. It is a simple matter to either increase input voltages by a factor of ten, or increase the gain of an operational amplifier ten times, to bring the potentiometer constant above unity. Like the slide-rule, it is simply a matter of deciding in advance where the decimal point should be.

SUMMING AMPLIFIER

The summing amplifier of Fig. 1·2b uses a high gain operational amplifier with several inputs to achieve addition and subtraction of machine variables. When the operational amplifier has a voltage gain equal to several thousand, input voltages will be accurately summed together, without unwanted interaction. The summing junction SJ is at "virtual earth", a way of saying that SJ will never be more than a few millivolts above or below earth potential, and is also, to all intents and purposes, shunted by a resistance of only a few ohms. Compared with input resistors R1–R3, the SJ shunt resistance is very low indeed, a condition necessary for accurate summing of voltages.

A definite relationship exists between resistors R1–R3, and feedback resistor R_f, and if these resistors are arranged to plug into the amplifier, many problem conditions can be met by "ringing the changes" on preferred values of fixed resistor, including multiplication by a constant as well as addition.

If a voltage E_1 is applied via resistor R_1 (in Fig. 1.2b) ot the summing junction SJ, the output voltage E_o will be $-E_1\frac{R_f}{R_1}$. The operational amplifier is designed to invert an input voltage, hence the minus sign in front of this expression. The ratio between input resistor and R_f holds good for each input.

Example: apply three input voltages $E_1 = 5$, $E_2 = -3{\cdot}5$, and $E_3 = 2$ to the summing junction via $R_1 = 10$ kilohm, $R_2 = 2$ kilohm and $R_3 = 100$ kilohm. Let the feedback resistor $R_f = 10$ kilohm. The relationship between voltages and resistances will be

$$E_o = -\left(E_1\frac{R_f}{R_1} - E_2\frac{R_f}{R_2} + E_3\frac{R_f}{R_3}\right)$$ Substituting values

$$E_o = \left(5\frac{10}{10} - 3{\cdot}5\frac{10}{2} + 2\frac{10}{100}\right) = (5 - 3{\cdot}5 \times 5) + 0{\cdot}2),$$

therefore $E_o = 12{\cdot}3$.

In the above example, the summing amplifier has not only summed negative and positive inputs, but has also multiplied E_2 by 5, and E_3 by a constant of 0·1, merely by selection of appropriate values of input resistor.

SUMMING INTEGRATOR

The summing integrator is used for the detailed investigation of time dependent variables, and for the solution of problems involving calculus.

The integrator of Fig. 1.2c is based on the inverting operational amplifier, with capacitor C_f acting as the feedback component. The output from a single integrator, in response to a steady voltage input, is a linear ramp voltage which increases with time at a rate dependent on choice of input resistor, feedback capacitor, and input voltage. Once again, precise relationships must exist between computing components and voltage, but now time is introduced as an additional analogue variable.

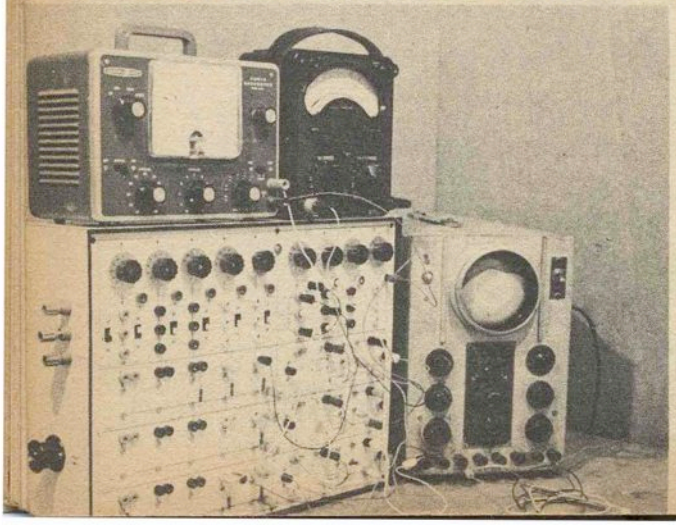
The action of electronic integration is best explained by a working example, and reference should be made to the diagram of Fig. 1.3a.

Example: a fairly sluggish motor car accelerates from rest at a steady rate of 20ft/second/second. Examine the progress of the motor car during the first four seconds of its motion. The computer is set up to operate in "real time", that is to say, the time actually occupied by the motor car when accelerating. The problem layout of Fig. 1.3a shows a computing potentiometer "A" coupled to the input of Integrator "1", which in turn feeds Integrator "2". Voltmeters are connected into circuit to display the three parameters of interest. Potentiometer "A" is first adjusted so that its dial reads 2, corresponding to multiplication by the constant 0·2, to represent 20ft/s² scaled down to yield a voltage of appropriate magnitude for the integrators to handle. The output from the potentiometer is a steady voltage analogue of a steady rate of acceleration.

As soon as switch S3 is closed to the +V position, the velocity and distance meter pointers will start to move in a manner analogous to the motion of the motor car. Velocity will increase linearly with respect to time, while distance will be displayed as an accelerating pointer movement. Integrator "2" computes distance (s) as a voltage function of the square of time, in terms of $s = \frac{1}{2}at^2$.

With the problem of Fig. 1.3a, acceleration, velocity, and distance are immediately available to the computer operator as dial and meter readings. He can vary acceleration just by turning the dial of the potentio-

This photograph shows UNIT "A" being used to simulate a tuned LC circuit, consisting of an inductance of 5H in series with a capacitance of 5μF. The oscilloscope is displaying phase shift within the simulated circuit at the resonant frequency of 31Hz, and the trace also gives an indication of the damping factor or "Q" of the circuit



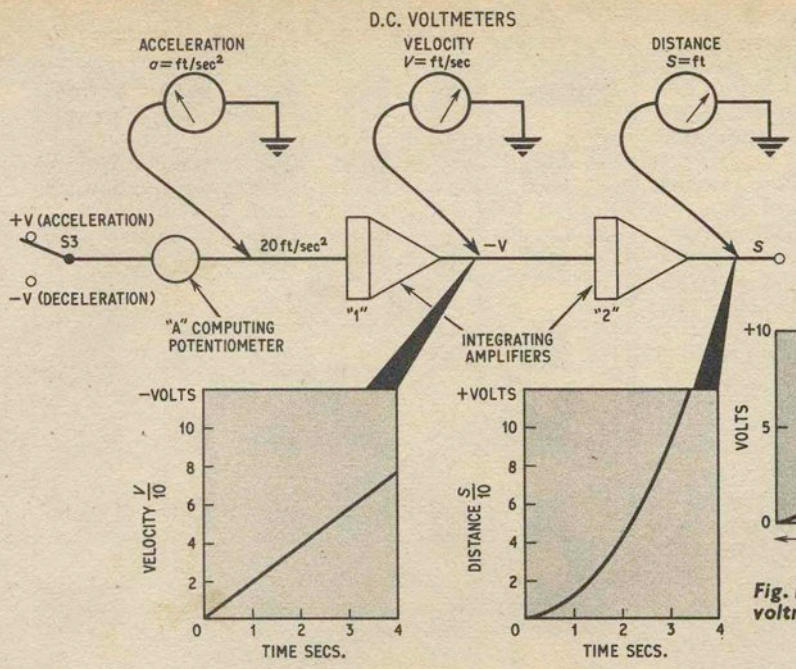


Fig. 1.3a (left). The use of integrators is illustrated in this diagram. In this example the rate of acceleration, velocity, and distance covered by a motor car are computed and can be read off the potentiometer dial and meter scales

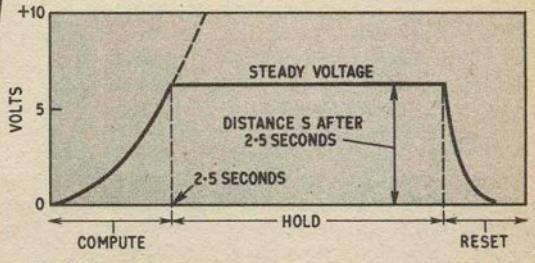


Fig. 1.3b. Arresting a computation to give a steady voltmeter reading

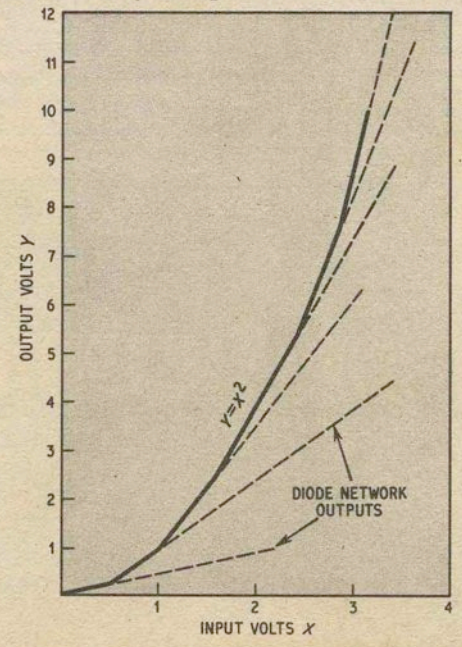
meter. If switch S3 is moved to the −V position, the car will decelerate and stop.

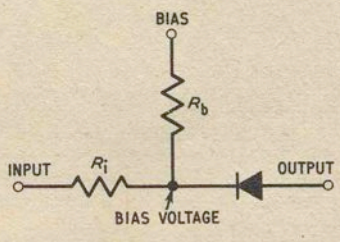
COMPUTE, HOLD AND RESET

It is obviously inconvenient to take readings from voltmeters when pointers are on the move, and it is impossible to do so if time t is very short, as with fast events, or when the computer is speeded up to some fraction of real time. The sequence governing switches S1 and S2, in Fig. 1.2c, is therefore arranged to provide three facilities, called "compute", "hold", and "reset".

The purpose of the "hold" facility is to allow a steady meter reading to be taken at any point on the voltage/time curve output of an integrator. The high gain introduced by the operational amplifier effectively multiplies the capacitance of C_f when the integrator input is disconnected from input resistors and reset resistance R_r. With amplification, C_f becomes the equivalent of a very large capacitor which is capable of holding a charge for a relatively long time. In practice, the ability of an integrator to "hold" or store a voltage will also depend on low amplifier drift.

Fig. 1.3b shows graphically the effect of compute, hold, and reset modes, when applied to the distance curve of Fig. 1.3a. In this case, it is necessary to halt the computation after an elapsed time of 2·5s, and obtain a value for distance in the form of a steady meter reading.





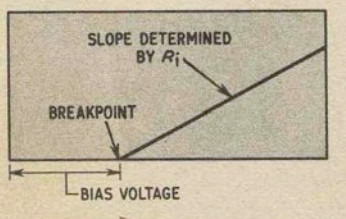


Fig. 1.4a (left). Illustrating how a mathematical function can be constructed from a series of straight line tangents

Fig. 1.4b (above). A single diode network and its output characteristic

The compute mode is initiated by opening S1 and closing S2 (Fig. 1.2c). After 2·5seconds, S2 automatically opens and the amplifier input is left floating, with C_f still connected between input and output and holding a stored charge. A meter coupled to the integrator output will show the distance travelled after 2·5s of acceleration.

The "hold" period can occupy several tens of seconds, and is usually at the discretion of the operator. To begin a new computer run, S1 is closed, discharging C_f through R_r, thus resetting the integrator output to zero. The input E_{ic} in Fig. 1.2c, is to allow an initial condition to be applied to the integrator, as in the case of a motor car which does not start from rest, but is already in motion when it accelerates. When computing and resetting times are shorter than about 1s, voltmeter answers will appear to be given at the instant of pressing the button which initiates the S1, S2 cycle.

The above description relates to a "single shot" computer run, where the operator adjusts, takes a reading, adjusts, and so on. In the repetitive mode, the hold facility is ignored and the computer keeps on repeating the answer curve, for display on an oscilloscope, chart recorder, or XY plotter.

DIODE FUNCTION GENERATOR

In many computer applications it is necessary to generate a voltage which varies according to some non-linear function not provided by normal operational amplifier techniques. The diode function generator of Fig. 1.2d will allow a mathematical function to be constructed from a series of straight line tangents, as shown in Fig. 1.4a.

Each straight line characteristic is obtained from a single diode-resistor network, and when the outputs from several networks are summed together a complete function will result. The shape of the final approximated curve is determined by adjustment of the network resistors. Apart from powers of x, and other functions, roots are achieved by placing the function generator in the feedback loop of an operational amplifier.

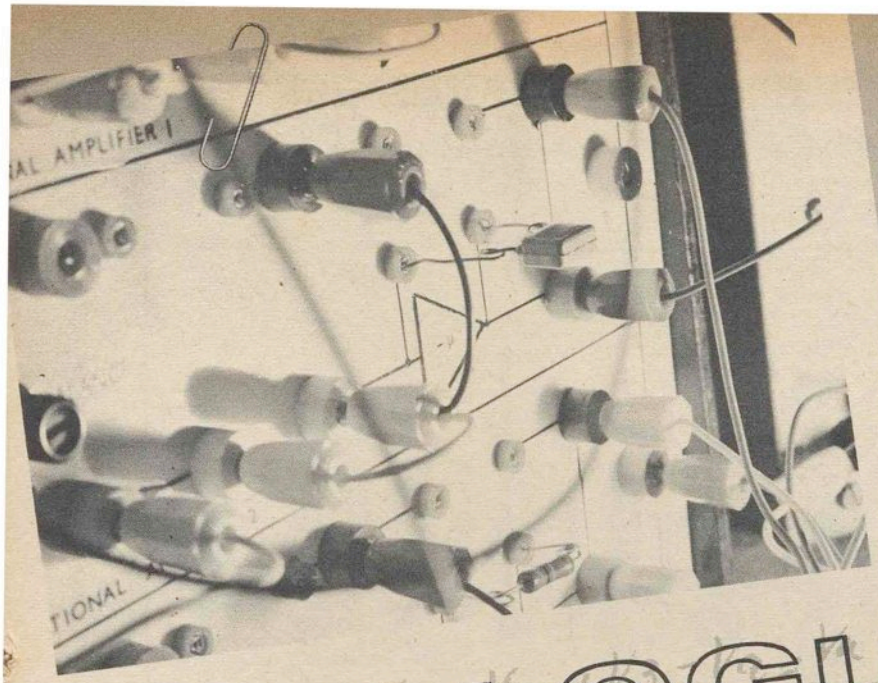
A single diode network appears in Fig. 1.4b, and the slope of its output characteristic can be varied by adjustment of R_1. The diode breakpoint (the voltage at which the diode starts to conduct) is dependent on the value of R_b.

MULTIPLIER

The computing potentiometer will multiply a variable by a constant, but special techniques must be used to multiply one variable by another variable. The process employed in modern computers is akin to modulation, where the gain of a circuit is controlled by an applied voltage.

The multiplier should yield a product of correct sign when multiplying negative or positive variables, and this is readily achieved with the self-excited time division circuit of Fig. 1.2e. The time division multiplier operates on the principle of modifying the mark-space and amplitude of a square wave in accord with two voltage inputs. The filter of Fig. 1.2e extracts the mean level of d.c. from the square waveform. An additional advantage of the Fig. 1.2e circuit is that it can be arranged to cater for more than two variables. For example, inputs $X1$, $X2$, and $X3$ multiplied by input Y.

Next month : Commencing the construction of UNIT "A".



PEAC

ANALOGUE COMPUTER

By D.BOLLEN

BEFORE embarking on constructional details, a few words must be said concerning measuring and test equipment required.

VOLTAGE STANDARD

It is necessary, at an early stage of computer construction, to establish a voltage standard for setting up the PEAC circuits.

Since *relative* voltage levels are more important than *absolute* levels, one particular voltmeter of proven reliability can serve as a voltage standard, and this might well be a reputable testmeter which has a large scale conveniently calibrated in terms of 0–10 volts, with a d.c. sensitivity of not less than 20,000 ohms per volt. Even if the testmeter has an error of 2 per cent of the indicated reading on d.c. ranges, it should be capable of reproducing a given reading, from day to day under similar room temperature conditions, with much greater accuracy.

In addition to use as a voltage standard, the testmeter can, of course, be employed for setting up problems, answer readout, comparative resistance checks, and for general testing of all circuits. There is nothing to prevent re-calibration of the computer to laboratory voltage standards at a later date, and this has been allowed for in the overall design of PEAC.

COMPUTER INSTRUMENTATION

Analogue computer instrumentation has much in common with electronic workshop equipment. Among those instruments likely to be of use to the computer operator are: an oscilloscope, a small collection of d.c. voltmeters, an audio oscillator, an a.c. voltmeter, and a component measuring bridge.

The oscilloscope need not conform to a modern specification, and could be a government surplus item. However, it is often an advantage to have a large screen area, and redundant television sets can be converted for computer readout purposes with excellent results. The limited bandwidth of magnetic deflection is no disadvantage at normal computer operating speeds.

D.C. voltmeters with centre zero scales are very useful for rough checks on the terms of a computer equation, where, for example, the wish is to see how y varies in relation to x when manipulating a simultaneous equation.

A sine wave oscillator, with attendant a.c. voltmeter, will often be employed for work on transfer functions, and for general electronic circuit simulation.

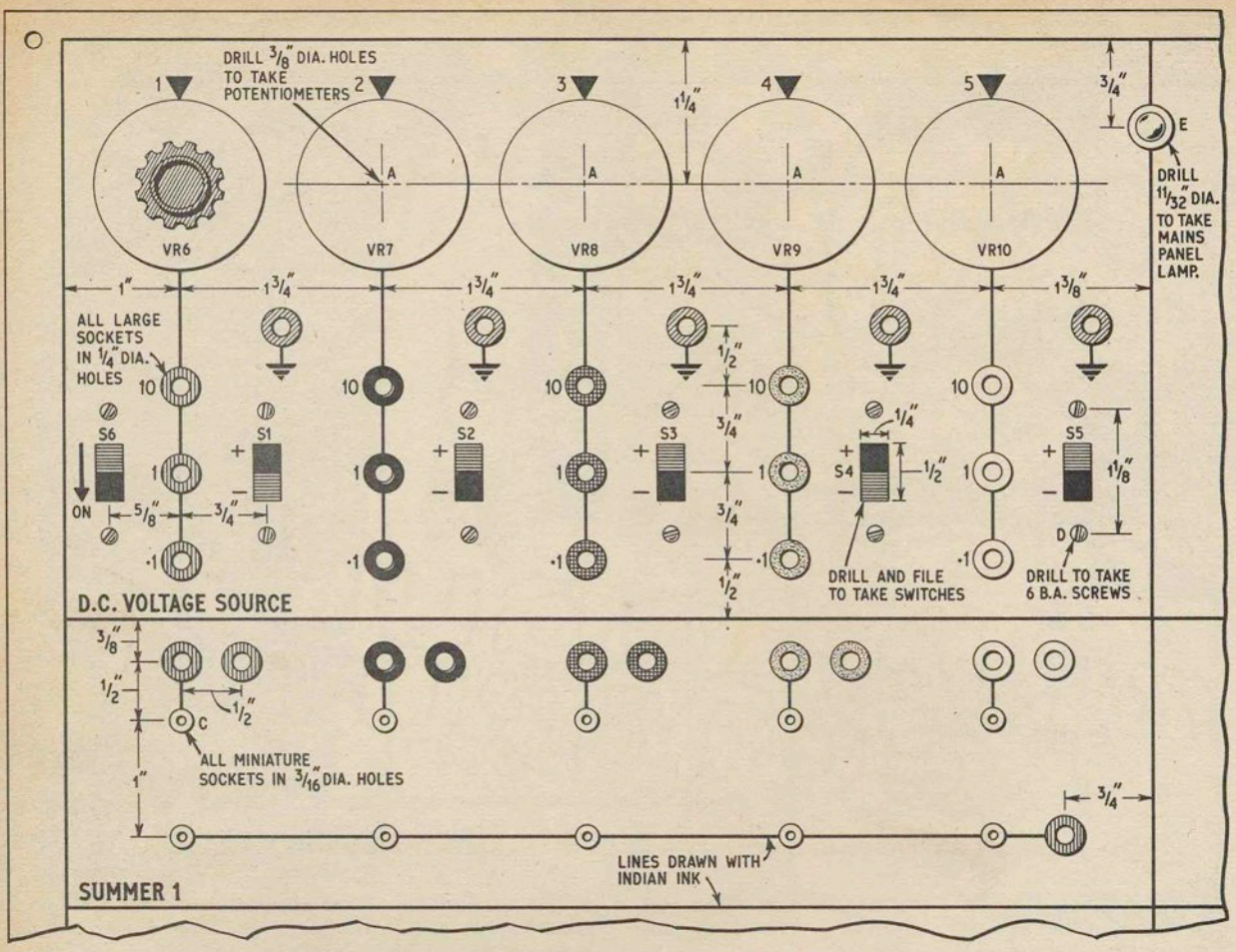
Finally, the component bridge is a help when making-up plug-in computing components, and for locating possible sources of error.

It is assumed that special classes of equipment, such as the XY plotter, will not be available to the amateur, and they are therefore excluded from further mention.

UNIT "A" CONSTRUCTION

The general form of construction adopted for PEAC is based on a series of boxes made with laminates of white Armaboard or Formica and hardboard. The resulting box is rigid and durable, with a surface which easily takes panel transfers and lines drawn in Indian ink. With such a construction, it is possible to achieve a professional appearance using only simple woodworking tools.

It is advisable to start with the UNIT "A" front panel and case. This slightly unusual procedure, of building the box before starting on internal circuits,



BLACK RED BLUE
WHITE YELLOW GREEN

Fig. 2.2. Left-hand portion of front panel. Drilling details, layout of components, and panel engraving. (Below the broken line, there are two further sections, each a replica of "Summer 1")

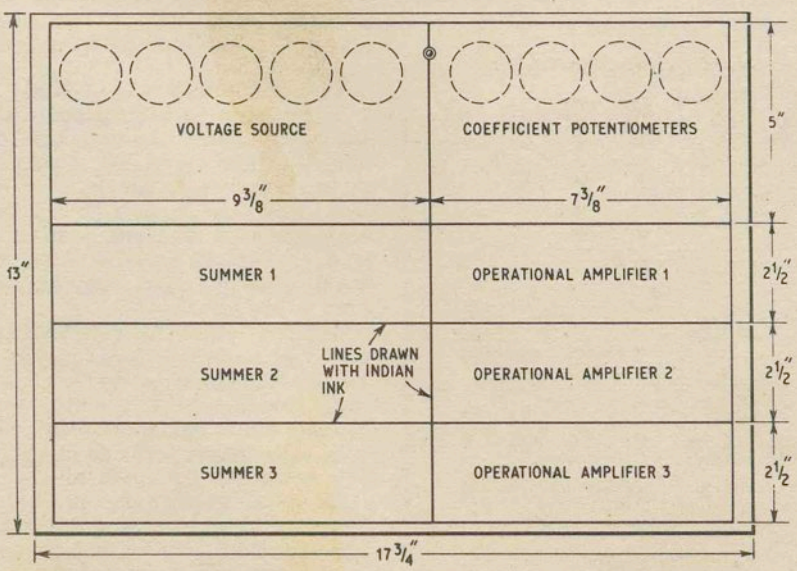


Fig. 2.1. UNIT "A" front panel. Overall dimensions and sectional dividing lines

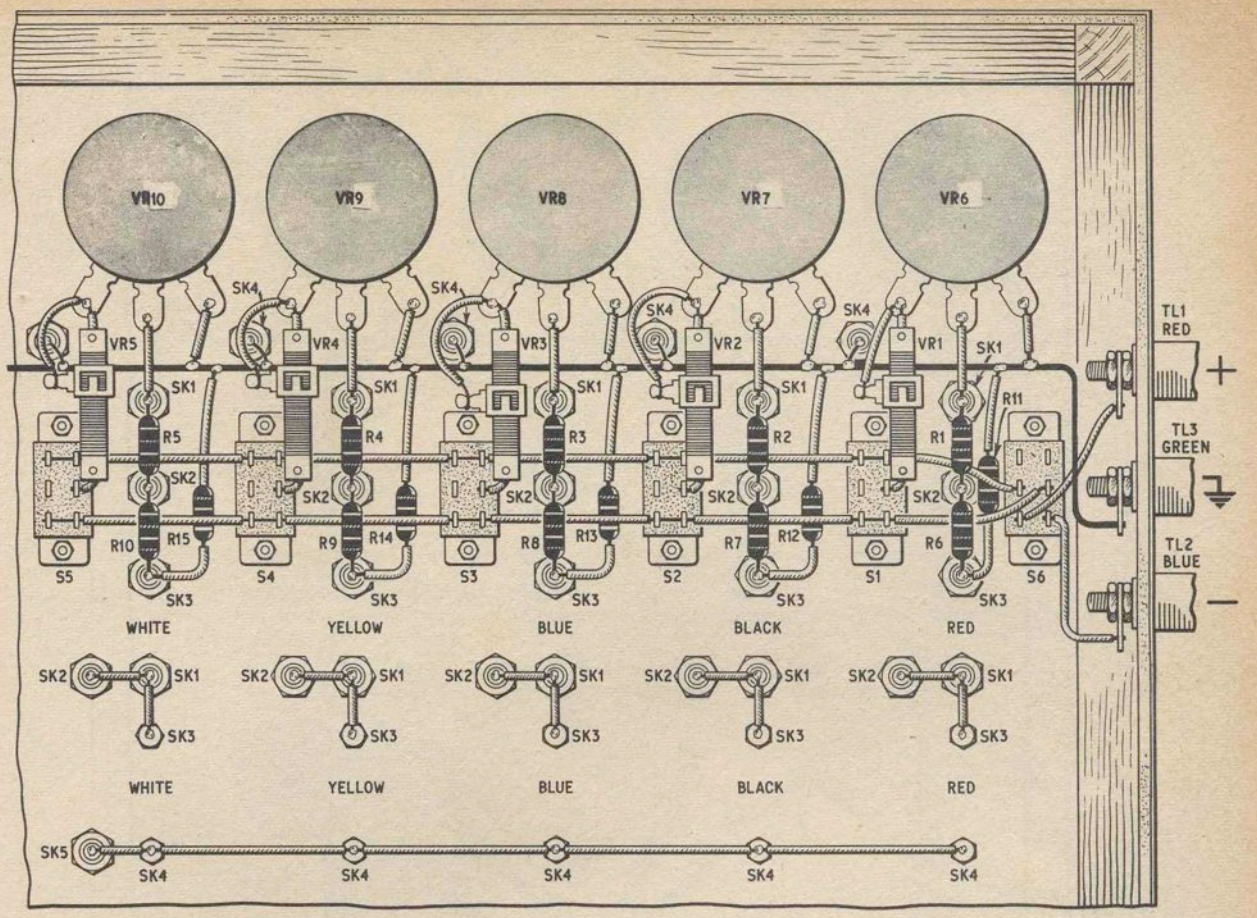
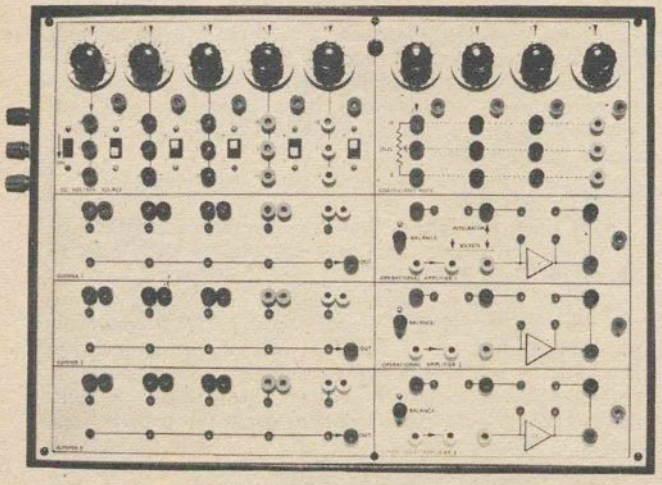


Fig. 2.3. Reverse side of front panel, left-hand portion (Fig. 2.2), showing components and wiring. Summer 2 and 3 are wired exactly as Summer 1 shown here. The three terminals TL1, 2 and 3 are mounted on the side of the box



UNIT "A" front panel

may be justified on two counts: firstly, the front panel really forms a circuit which is designed to be accessible, and is an important part of the unit; secondly, the method of construction chosen brings economy by dispensing with a self-supporting internal chassis assembly, and much of the internal gear is actually mounted on the front panel, or to the box itself.

UNIT "A" FRONT PANEL

To prepare the front panel, a sheet of white plastic laminate, slightly larger than its finished size of 13in × 17¾in, is glued to a sheet of hardboard of the same measurements with Evostick or a similar adhesive. When firm, the panel edges can be planed, rasped, or sandpapered down to size, while making sure that all is square. Next, taking Fig. 2.1 and the photograph of the front panel as a guide, mark out the main dividing lines with a pencil.

The positions of all holes and slots may be found by referring to panel drawings Fig. 2.2 and Fig. 2.5. Establish hole centres by first marking with a pencil, then indenting with a sharp spike. Note that all drilling should be carried out from the plastic laminate side of the panel, to avoid chipping the white surface. It is important to handle tools carefully, and prevent them skidding across the plastic surface and scoring it. When all holes have been drilled, deburr them on the reverse side of the panel with sandpaper, and check that components will fit correctly before applying a coat of clear varnish to the hardboard backing.

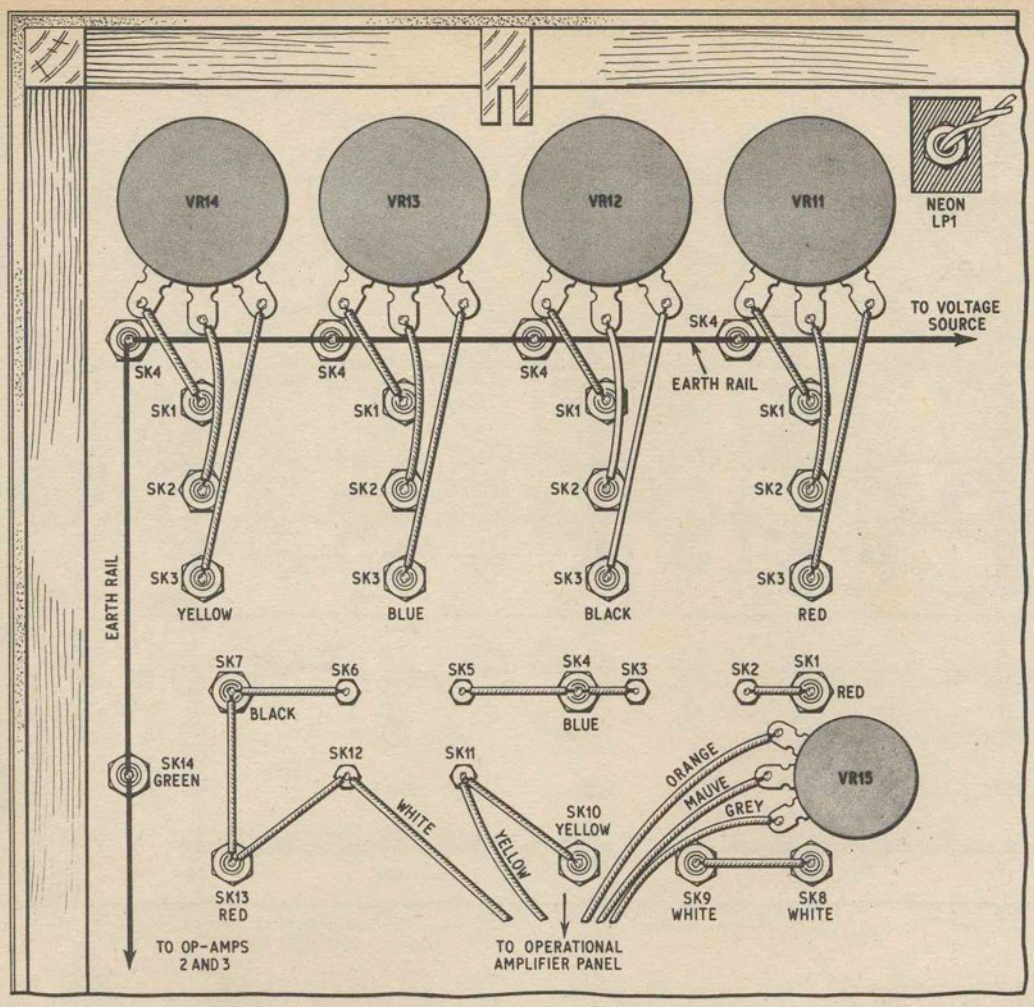
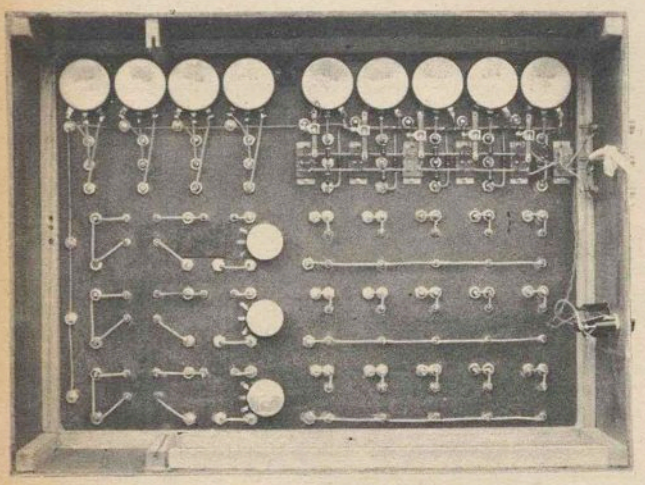


Fig. 2.4. Right-hand portion of front panel viewed from rear, showing components and wiring. Operational Amplifiers 2 and 3 are wired exactly as "Operational Amplifier 1" shown here



Rear view of UNIT "A" front panel

To finish the panel, draw in all lines and symbols with a nib pen and Indian ink. If any mistakes are made, the ink can be removed—when dry—with a typewriter eraser, and surface shine restored with metal polish. Lettering can be applied by the "rub-on" or "stick-on" transfer methods, and should be protected by a thin layer of clear varnish.

When the panel decor has dried, mount all sockets, potentiometers, knobs with dials, switches, and the neon mains lamp. Dials may be lined up on potentiometer spindles later.

UNIT "A" BOX

This time, the box is first constructed of hardboard on a wooden frame, and is later covered with plastic laminate. See Fig. 2.12.

Cut and finish the four hardboard panels to size, and cut the various lengths of softwood. The manner of assembly could be as follows: attach wood lengths *A* and *C* to top and bottom panels with panel pins or countersunk woodscrews, gluing all joints. Attach lengths *B* to side panels, bring panels together and secure. Next, position *D*, *E*, and *F*. Note that there is no length *D* at the back portion of the top panel so the slotted amplifier mount *F* should be lined up vertically with its companion *E*. All drilling must be left until the plastic laminate is in place.

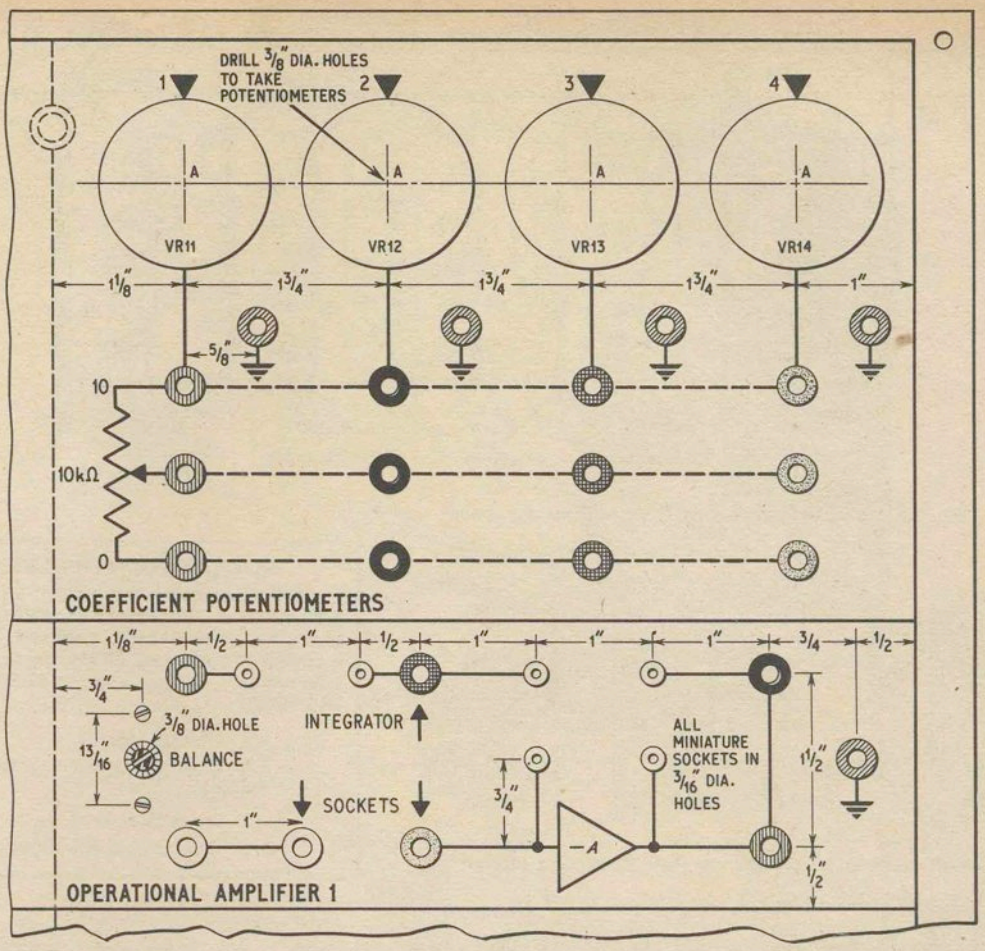


Fig. 2.5. Right-hand portion of front panel. Drilling details, layout of components, and panel engraving. Below the broken line there are two further sections, each a replica of "Operational Amplifier 1"

COMPONENTS . . .

UNIT "A" FRONT PANEL AND BOX

Resistors
R1–R5 9·1kΩ (5 off)
R6–R10 910Ω (5 off)
R11–R15 100Ω (5 off)
All 5%, ½W carbon film

Pre-set Potentiometers
VR1–VR5 250Ω miniature wirewound slider type (5 off)
VR15–VR17 50Ω wirewound panel mounting type (3 off)

Potentiometers
VR6–VR10 1kΩ 3W linear wirewound, ±20% or better, 270° effective rotation (5 off)
VR11–VR14 10kΩ 3W linear wirewound, ±20% or better, 270° effective rotation (4 off)

Switches
S1–S6 Double-pole, on/off slide switch (Radiospares) (6 off)

Plug
PL1 3 way panel mounting mains plug and cable connector

Fuse
FS1 1·5A cartridge fuse and 20mm fuseholder

Lamp
LP1 Neon indicator lamp (Radiospares "miniature 200–250V panel neon" with self-contained resistor)

Sockets
21 Red, 15 Black, 15 Blue, 15 Yellow, 15 White, 12 Green (painted green, see text)
48 miniature sockets, black or red to choice

Terminals
Insulated screw, to take 4mm stackable plugs (Radiospares). 1 Red, 1 Green, 1 Blue

Miscellaneous
Material for panel and box: Hardboard: 2 off 13in × 5in, 2 off 18in × 5in, 1 off 13in × 17¾in. White plastic laminate: 2 off 13in × 5in, 2 off 18in × 5in, 1 off 13in × 17¾in. Softwood: 52in × ½in square, 4in × ⅞in × ⅜in.
20 s.w.g. tinned copper wire. Insulated sleeving

Dials and knobs
Nine 0–10 270° dial knobs (Bulgin type K400), black or grey

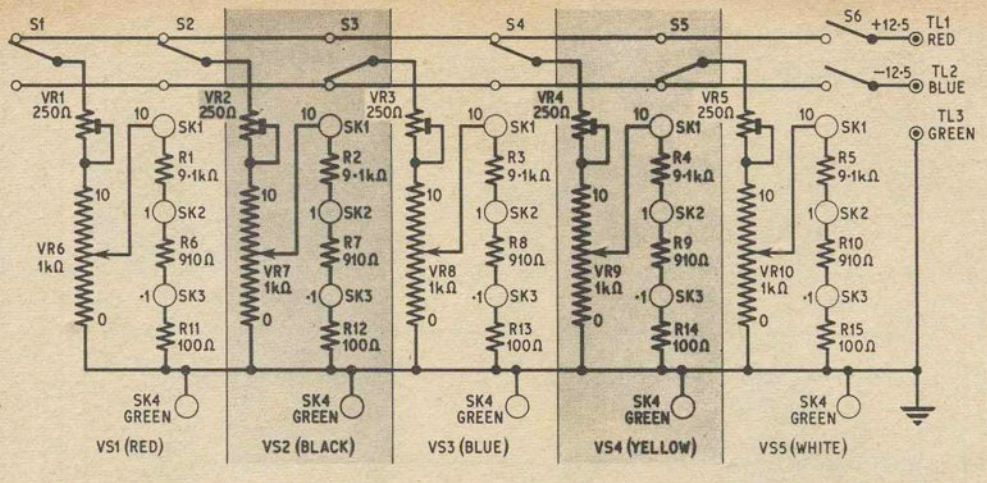


Fig. 2.6. Circuit diagram of Voltage Source section

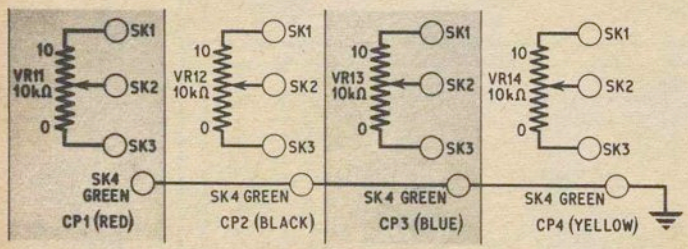


Fig. 2.7. Circuit diagram of Coefficient Potentiometers section

SOCKET IDENTIFICATION

The following abbreviations will be used in the programming instructions for PEAC. Applied as prefixes to socket (SK) numbers, they clearly establish the identity of the particular socket referred to. For example, "VS2/SK1"; "CP1/SK3" etc.

VS	Voltage source
CP	Coefficient potentiometers
S	Summer
I	Input (Summer)
OA	Operational Amplifier

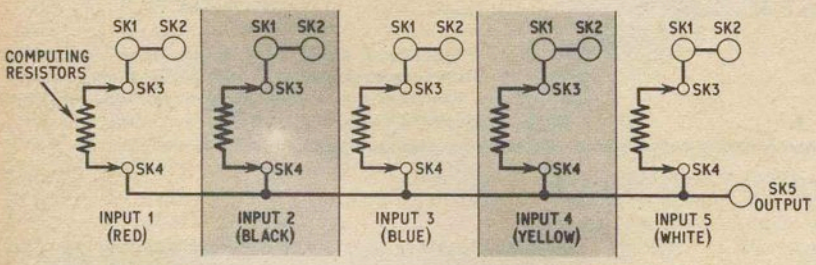


Fig. 2.8. Circuit diagram of Summer 1, 2, and 3

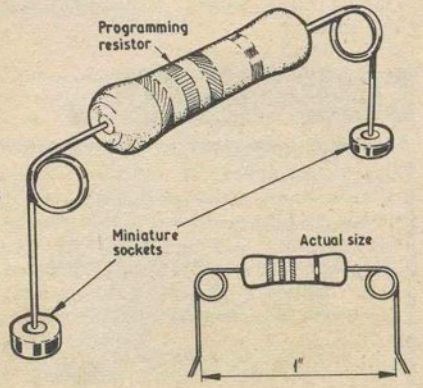


Fig. 2.11. Method of bending leads to make plug-in programming resistors

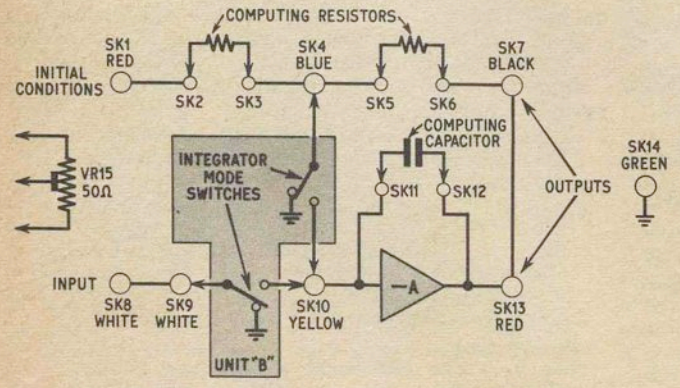


Fig. 2.9. Circuit diagram of Operational Amplifier 1, 2, and 3

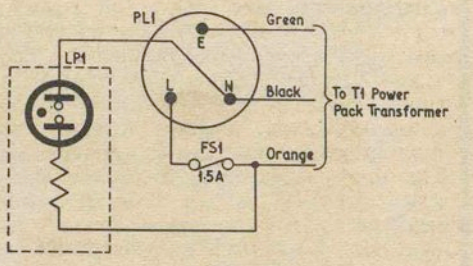
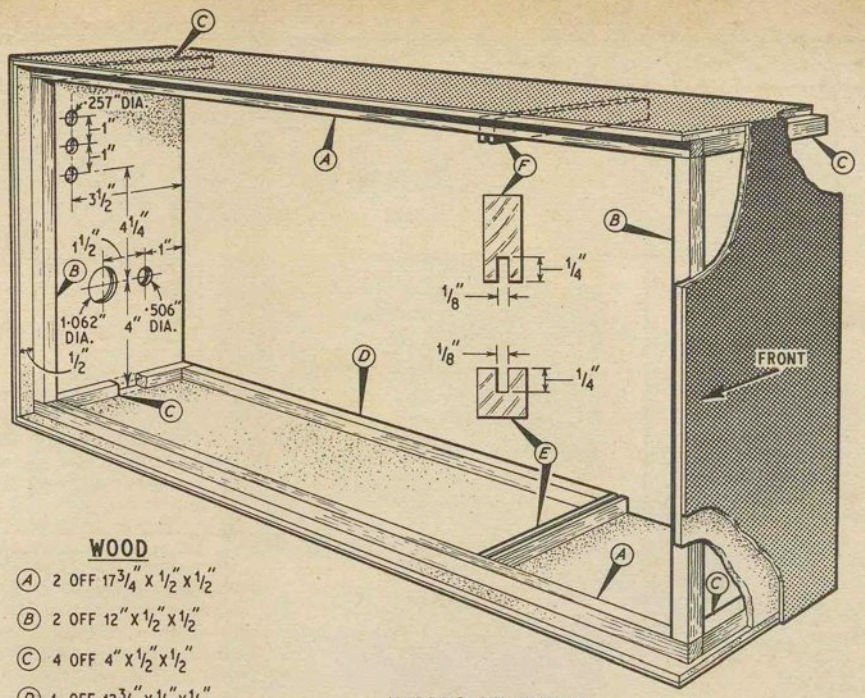


Fig. 2.10. Circuit diagram of mains supply



WOOD

(A) 2 OFF 17¾" X ½" X ½"

(B) 2 OFF 12" X ½" X ½"

(C) 4 OFF 4" X ½" X ½"

(D) 1 OFF 12¾" X ½" X ½"

(E) 1 OFF 4" X ½" X ½" WITH SLOT

(F) 1 OFF 4" X ⅞" X ⅜" WITH SLOT

HARDBOARD PANELS

2 OFF 13" X 5" (SIDES)

2 OFF 18" X 5" (TOP AND BOTTOM)

Fig. 2.12. Constructional details of UNIT "A" Box

Cut plastic laminate to fit hardboard panels with $\frac{1}{16}$in overlap, and glue to the box sides first. Reduce the overlap to size when the laminates are firm, before fitting the top and bottom surfaces. When trimming the top and bottom panels down to size, take care not to scratch and score the side pieces. For economy, the bottom plastic laminate layer can be omitted.

When satisfied with the laminated exterior, the 1·062in dia. hole can be made by a series of small drillings and finished with a half-round file. The box interior and wood may be varnished, but the raised lip at the front of the box is best painted black, or some dark colour, to contrast with the front panel.

The finished box is quite strong, and will support the full weight of a normal adult when the front panel is in place. However, it is recommended that this test should not be applied too often!

FRONT PANEL WIRING

Attach the front panel to its box, which will act as a convenient mount when wiring the back of the panel.

The bare earth wire linking all green sockets runs along the top half of the front panel and down its left-hand side, looking from the back; this should be soldered in place before embarking on the sleeved wiring. (No matching green sockets were available for the prototype, so odd coloured sockets were painted green with cellulose model aeroplane dope.)

The 4mm red, green, and blue terminal sockets on the side of UNIT "A" are designed to take stackable plugs, and will make available the power supply outputs to external sub-units. Wiring can proceed from the terminal sockets along the voltage source (see Fig. 2.3) and then to the rest of the front panel.

Circuit diagrams for all the various "sections" incorporated in the front panel are given in Figs. 2.6 to 2.10 inclusive. Wiring details are given in Fig. 2.3 and Fig. 2.4.

The summer and operational amplifier sections are triplicated—although only one of each of these sections has been shown in the diagrams Fig. 2.2 to Fig. 2.5 inclusive.

The purpose of the miniature sockets, which appear in the above mentioned diagrams, is to take the plug-in programming components; explained by Fig. 2.11. Resistor leads are preformed in the manner shown. The distance between miniature sockets is standardised at 1in, to allow the use of a special made-up two pin plug to support the bulkier components, such as large polyester capacitors.

When wiring up the operational amplifier sockets, ignore for the time being the coloured flexible wires shown in Fig. 2.4 as these are the flying leads from the operational amplifier panel, and will be referred back to when the time comes to mount the amplifiers.

Fit the mains connector PL1 and fuseholder for FS1 to the side of the box. Wire up the neon lamp LP1 and the fuse FS1 to PL1 as shown in Fig. 2.10.

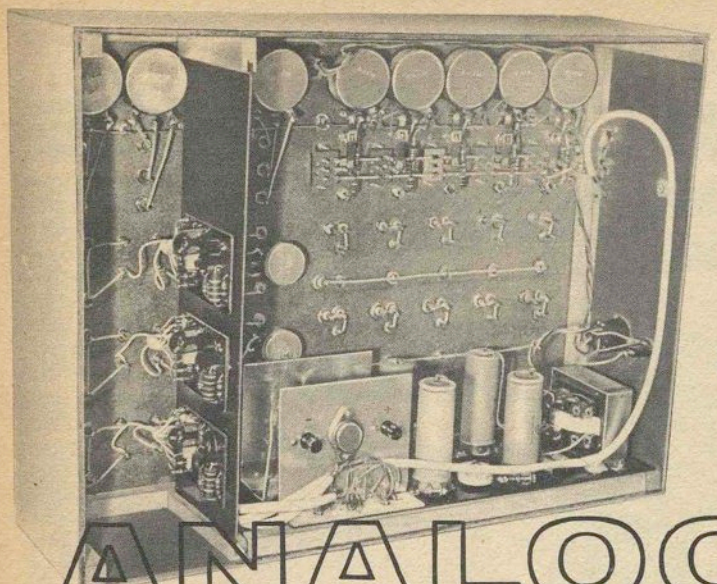
CORRECTION.

In Part 1, Page 40, last line of the equation in the example at top of right-hand column should read:

$$E_0 = -\left(5\tfrac{10}{10} - 3{\cdot}5\tfrac{10}{2} + 2\tfrac{10}{100}\right) = -(5 - (3{\cdot}5 \times 5) + 0{\cdot}2),$$

therefore $E_0 = 12{\cdot}3$.

Next month: Power supply and operational amplifiers



PEAC

By D. BOLLEN

ANALOGUE COMPUTER

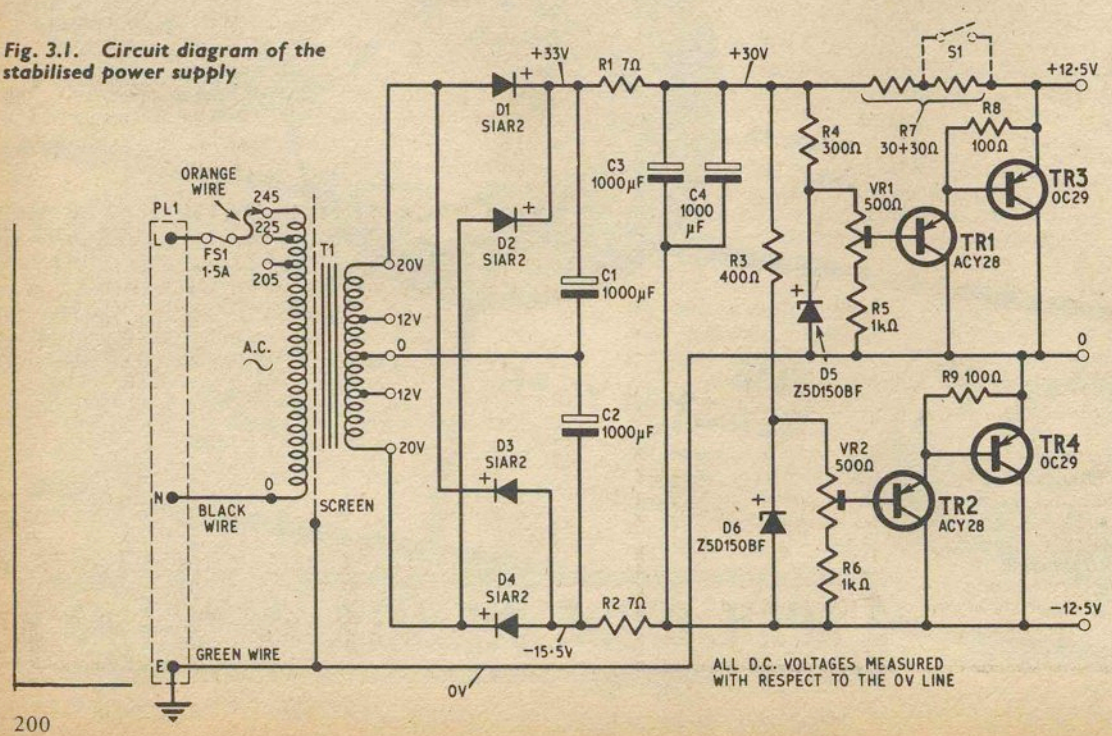
THE main design target for the PEAC power supply was a maximum voltage variation of not more than 1 per cent under all normal operating conditions. Several circuit configurations were tried, based upon either series or shunt regulation, but it was found that shunt regulation invariably gave the best performance for a given cost, plus the bonus of complete short-circuit protection. It was not considered to be a disadvantage for computer work, where nearly everything is switched on for most of the time, that a shunt regulated supply would be wasteful of power under no-load conditions.

The current reserve of the stabilised supply will just be sufficient to cater for the needs of UNITS "A to D". If further expansion of the computer is contemplated, beyond the inclusion of UNIT "D", a subsidiary unstabilised supply can be added to the computer at a late stage of construction, to power the relays of UNITS "B" and "D", and thus make available some extra current from the stabilised supply.

STABILISED POWER PACK

The circuit of Fig. 3.1 is based on a small, standard type of rectifier transformer, with bridge rectification

Fig. 3.1. Circuit diagram of the stabilised power supply



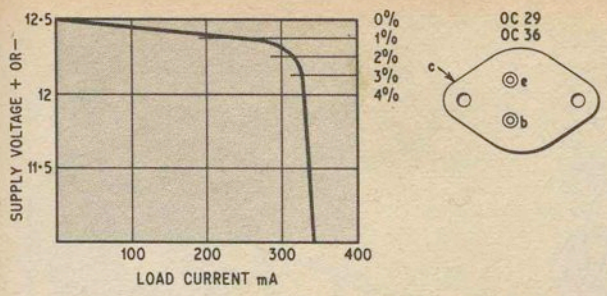


Fig. 3.2. Performance curve of stabilised power supply

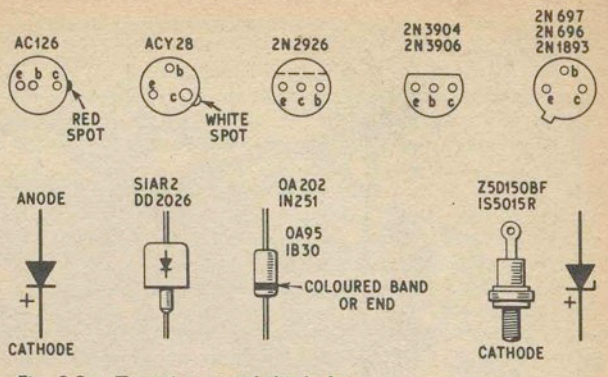


Fig. 3.3. Transistor and diode key

followed by two shunt regulators arranged in series to give positive and negative outputs relative to a zero voltage earthed centre-tap. Diodes D1–D4 provide full-wave rectification of the 40V r.m.s. nominal transformer output. Capacitors C1 and C2 are wired in series, with their common connection taken to the transformer centre-tap, and this doubles the capacitor voltage rating without the need for bleeder resistors. R1 and R2 achieve some measure of preliminary ripple smoothing while dropping the unregulated d.c. voltage to a safe value for C3 and C4.

COMPONENTS . . .

UNIT "A" POWER PACK

Resistors

R1, R2 7Ω 0·7A power resistors 5% (2 off)
R3 400Ω 5W wirewound 5%
R4 300Ω 5W wirewound 5%
R5, R6 1kΩ 2W carbon 10% (2 off)
R7 60Ω 0·7A power resistor 5% (two 30Ω in series, see text)
R8, R9 100Ω 1W carbon 10% (2 off)

Potentiometers

VR1, VR2 500Ω 3W panel mounting, wirewound (2 off)

Capacitors

C1–C4 1,000μF elect. 50V d.c. 900mA rippled (4 off)

Transformer

T1 Rectifier transformer. Standard mains primary. Secondary, 20V–0–20V 0·7A (Radiospares)

Diodes

D1–D4 S1AR2 (Westinghouse) *or* DD2026 (Lucas) (4 off)
D5, D6 Z5D150BF (STC) *or* IS5015R (Texas) (see text) (2 off)

Transistors

TR1, TR2 ACY28 (STC) *or* AC126 (Mullard) (2 off)
TR3, TR4 OC29 *or* OC36 (Mullard) (2 off)

Miscellaneous

Four capacitor clips to fit C1–C4
S.R.B.P. panel 4in × 12in × $\frac{1}{16}$in or $\frac{1}{8}$in
4 B.A. and 6 B.A. assorted screws, nuts, washers, and solder tags
Insulated sleeving
20 s.w.g. tinned copper wire
16 s.w.g. sheet aluminium 2 off 4in × 4in, and 2 off $1\frac{1}{2}$in × $1\frac{3}{4}$in.

SHUNT REGULATORS

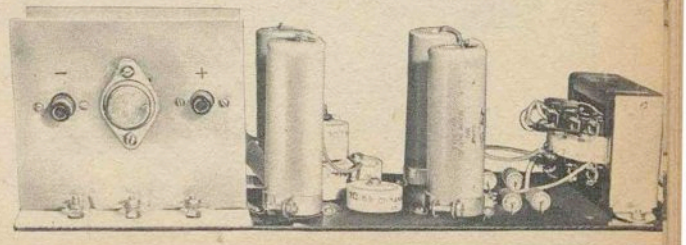
To understand the action of the twin shunt regulators, temporarily assume that the −12·5V output terminal is at zero voltage. The centre-tap and the positive outputs will then be positive in relation to the negative output. TR3 and TR4 collector-emitter voltages are both clamped at 12·5V, and the unregulated d.c. voltage is dropped across R7. Therefore, the voltage appearing at the junction of R7 and TR3 emitter is +25V relative to the assumed zero rail, with the centre-tap output at +12·5V. As all three output terminals are floating, it is a simple matter to connect the centre-tap output to an external earth and classify it as the zero voltage rail, with the other terminals forming positive and negative regulated outputs.

VR1 setting will determine the voltage across TR3, and VR2 the voltage across TR4. The range of adjustment of VR1 and VR2 is sufficient to allow for regulator diode (D5 and D6) tolerances on nominal voltage of ±15 per cent, and will therefore permit the use of manufacturers' rejects or "bargain" price regulator diodes. 10W diodes are specified for D5 and D6 in the Fig. 3.1 circuit, to achieve a low dynamic resistance, and reduce the short-term thermal changes which are inevitable when smaller regulator diodes are run at high temperatures.

Fig. 3.2 will give an idea of the capabilities of the regulated power supply, and maximum current limits. If an optional press-button switch is wired across one half of R7 (Fig. 3.1) output current can almost be doubled for short periods, and special purposes. The prolonged use of this extra current facility will, however, result in mains transformer overheating.

POWER PACK CONSTRUCTION

Low cost semiconductors were used throughout the prototype power pack. The diodes D1–D4 should have a p.i.v. rating of not less than 100V, and a maximum current rating of 1A or more. It is advisable to check all diodes with an ohmmeter, for high reverse resistance and correct polarity. The D5 and D6



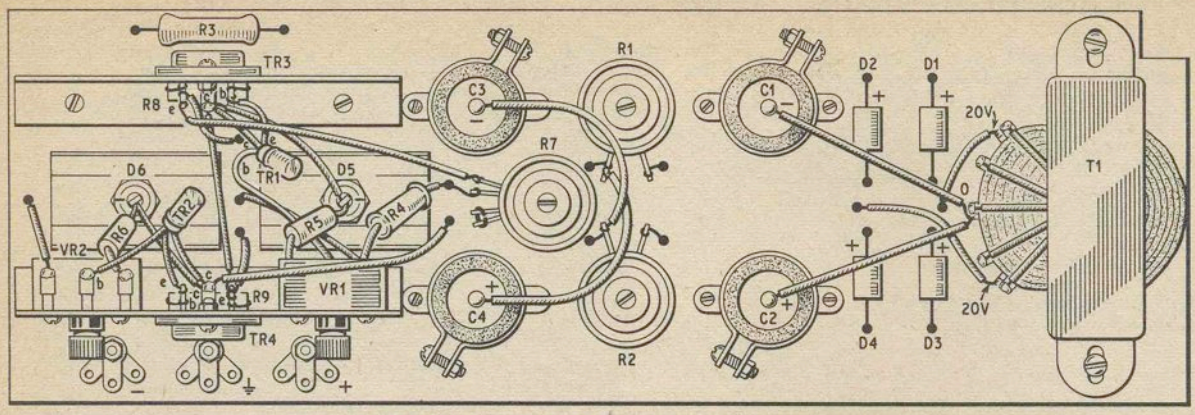


Fig. 3.4 Power supply component layout

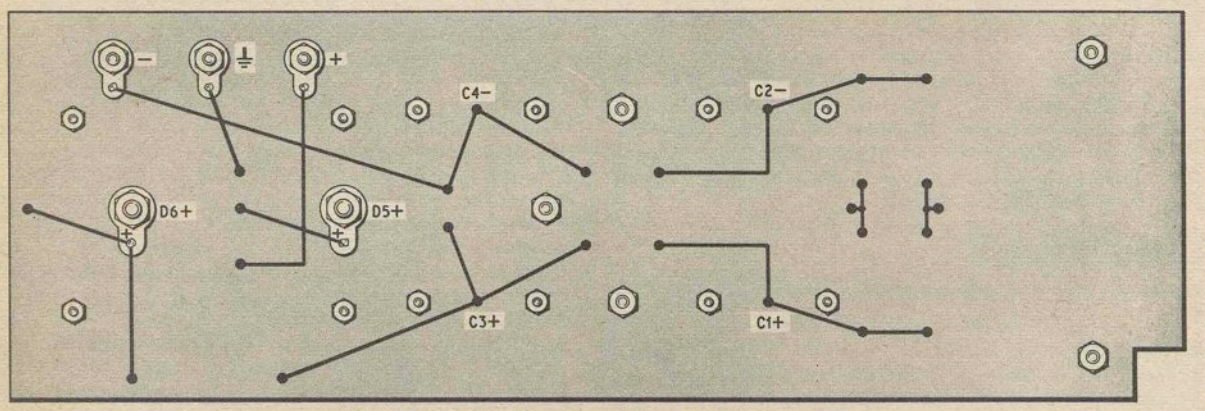


Fig. 3.5 Underside wiring of power supply panel

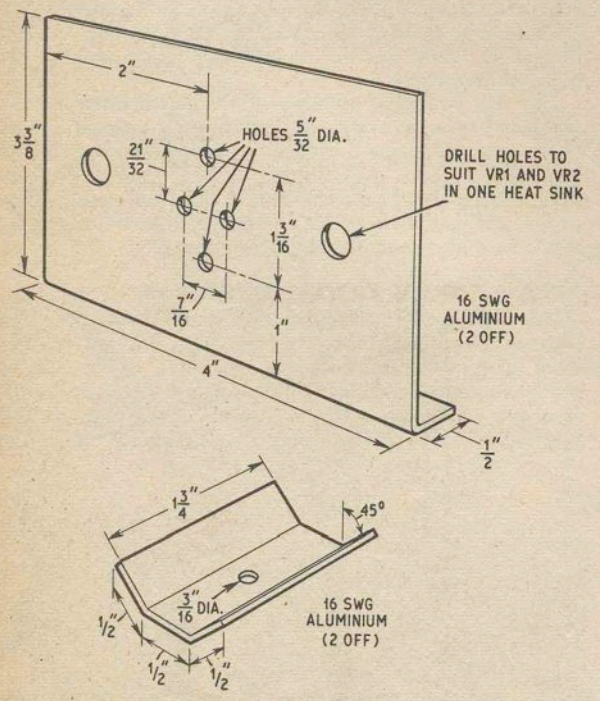


Fig. 3.6. Power supply heat sink details

measured voltage, when passing a current of about 100mA, can fall anywhere within the limits 12·5–17·5V.

If a choice exists, TR1–TR4 can be selected for highest *beta* gain, but matching is not necessary. Collector-emitter leakage currents of TR1 and TR2, with open circuit base, will preferably be below about 200μA at normal room temperature.

It is seriously recommended that the reader who intends to build PEAC should adhere closely to the semiconductor types specified here, and not consult other lists of equivalents. A key to transistor and diode connections appears in Fig. 3.3, and this covers all the semiconductors used in PEAC circuits.

Power pack components are assembled on a $\frac{1}{16}$in or $\frac{1}{8}$in s.r.b.p. panel measuring 4in × 12in. The panel sits on the wooden framework at the bottom of the UNIT "A" box. Component layout appears in Fig. 3.4, with the underside wiring in Fig. 3.5. Heat sinks for TR3, TR4, D5, and D6 are made up from 16 s.w.g. aluminium sheet, and measurements are given in Fig. 3.6.

First drill the s.r.b.p. chassis panel to accept hardware and wires, using Fig. 3.5 as a guide. Mount the mains transformer, capacitor clips, power resistors, and the three output terminal screws. Attach the regulator diodes, with their heat sinks and solder tags, to the panel, taking care not to damage the diode top terminals. Bolt TR4, VR1, and VR2 to the appropriate heat sink, solder R9 to TR4 emitter and base pins, and install the assembly on the s.r.b.p. panel. Similarly, bolt TR3 to its heat sink, complete with R8, and fix to panel.

Both power transistors should have a solder tag attached to their upper mounting bolts to make convenient connection to transistor collectors. Without insulating washers, TR3 and TR4 heat sinks will be "live", but damage is unlikely to result in the event of an accidental short-circuit.

Insert capacitors C1–C4 in clips, with polarity as indicated on Fig. 3.4. Also observe correct polarity when mounting diodes D1–D4. Before wiring up all components, insert R3 in the panel, alongside TR3 heat-sink.

COLOUR CODED WIRE

Wiring can start at the input end of the panel, with 6in lengths of orange, black, and green multi-stranded wire soldered to the live, neutral, and screen tags on the mains transformer. Red and blue wires are reserved exclusively for 12·5V d.c. positive and negative supply rails, with green wiring as the common earth throughout the computer.

Wire colour coding is almost essential for computer circuit interconnection, as it enormously simplifies fault tracing and assembly. However, the wiring of individual circuits, such as the power pack panel, can take the form of single colour sleeved 20 s.w.g. tinned copper wire.

It will be noticed (Fig. 3.4) that TR1 and TR2 are supported only by their leads, and this is to allow best positioning for good ventilation, well away from heat sinks. In the prototype R7 was made up from two 0·7A power resistor sections, to allow for the optional extra current facility mentioned earlier.

When power pack wiring is completed and checked, multiple solder tags can be fitted to the three output terminal screws.

TESTING THE POWER PACK

Connect the transformer input leads to the mains socket on the side panel of the UNIT "A" box, with the organge lead taken via FS1 (see Fig. 2.10 and Fig. 3.1), and, also join the neon indicator leads to the live and neutral mains socket screws.

Turn VR1 and VR2 fully anticlockwise and switch on. A quick check with a voltmeter will show if there is any serious departure from the voltages shown in Fig. 3.1. If any overheating of heat sinks or mains transformer seems imminent, switch off immediately and locate fault.

To set up the power pack, apply voltmeter leads to earth and positive output terminal, and advance VR1 for a reading of 12·5V. Repeat the procedure for the negative output and VR2. If it is impossible to bring an output to 12·5V, this will indicate a wiring fault or trouble with a regulator diode.

After the power pack has been left on for some time, VR1 and VR2 can be finally trimmed for exact outputs of $\pm$12·5V. With no external load on the power supply, TR3 and TR4 heat sinks can be expected to run fairly warm.

To ensure that power pack regulation conforms to the curve of Fig. 3.2, positive and negative outputs can be loaded by a selection of 5W resistors in series with an ammeter, while voltage is still being monitored. A worst case variation of 2 per cent change in voltage for 300mA change in current should be taken as an acceptable performance limit. When one half of R7 is temporarily shorted out, at least 50 per cent more current should be available before voltage drops beyond 2 per cent.

Locate the power pack inside the UNIT "A" box, and wire outputs to the main terminals TL1, TL2, and TL3. Voltage source dial alignment and setting up details will be discussed later, but a few rough checks with power on are in order, to see that all voltage source sockets and switches are functioning correctly.

OPERATIONAL AMPLIFIER

The most important analogue computing circuit is the operational amplifier; so named because it will perform a number of mathematical operations, such as addition, subtraction, change of sign, multiplication by a constant, division by a constant, and integration. All the thinking behind "op-amp" design is concerned with making the circuit as unobtrusive as possible, so that it can be regarded purely as an operational "black box".

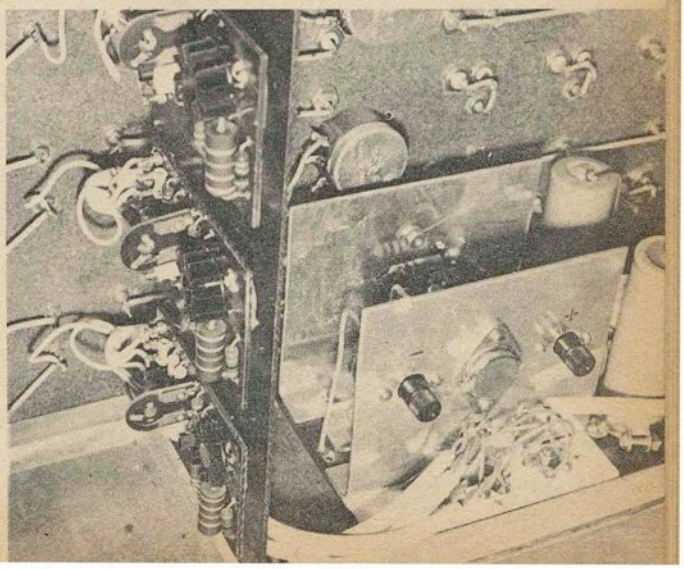
An analogue computer d.c. operational amplifier should comply with the following general requirements.

(a) Direct coupling between all stages to handle d.c. signals. Input and output terminals at earth potential in the absence of a signal, with 180 degree phase change (inversion) between input and output. Output voltage swings both positive and negative in relation to earth, and as large as the computer reference voltage ($\pm$10V).
(b) Large voltage gain in the open-loop configuration.
(c) Low output impedance.
(d) High input impedance.
(e) Very low input current.
(f) Sufficient bandwidth to cause negligible phase shift or attenuation of a signal up to the highest frequencies encountered.
(g) Insignificant output voltage drift over several hours.
(h) Good margin of stability when subjected to a wide range of different input, output, and feedback conditions.

Performance figures for UNIT "A" operational amplifiers are given in the Table 3.1, but to fully understand how some of the design problems are solved it is necessary to consult the actual "op-amp" circuit of Fig. 3.7.

OPERATIONAL AMPLIFIER CIRCUIT

The input stage of circuit Fig. 3.7 consists of a long-tailed pair (TR1, TR2), offering the advantages of high voltage gain, near zero input offset voltage relative to



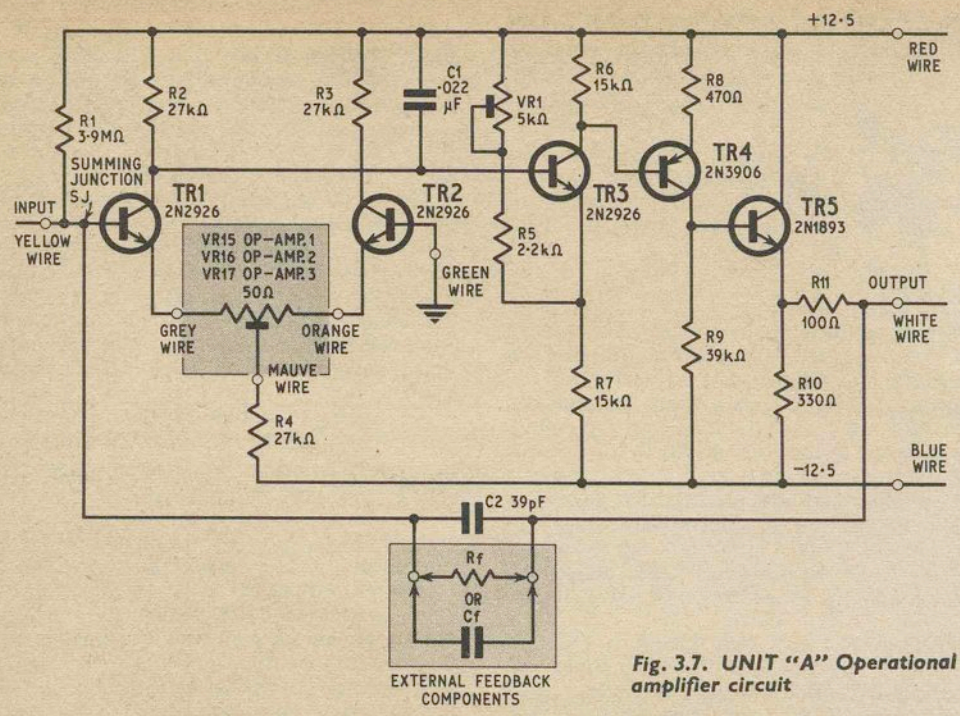


Fig. 3.7. UNIT "A" Operational amplifier circuit

COMPONENTS . . .

UNIT "A" OPERATIONAL AMPLIFIER

The following items are for a single amplifier, and are required in triplicate to cover the three amplifiers employed in UNIT "A".

Resistors

R1 3·9MΩ 5% carbon film
R2–R4 27kΩ 5% carbon film (3 off)
R5 2·2kΩ
R6, R7 15kΩ (2 off)
R8 470Ω
R9 39kΩ
R10 330Ω 2W
R11 100Ω
All ±10%, ½W carbon composition, except where otherwise stated

Potentiometer

VR1 5kΩ vertical skeleton pre-set

Capacitors

C1 0·022μF miniature polyester 250V d.c.
C2 39pF polystyrene 125V d.c.

Transistors

TR1–TR3 2N2926 orange (General Electric) *or* 2N3904 (Motorola) (3 off)
TR4 2N3906 (Motorola)
TR5 2N1893 (Bentron), 2N696, *or* 2N697 (General Electric).

Miscellaneous

S.r.b.p. panel 2in × 2¾in
Eight small turret tags
TO-5 transistor cooler Type BC105B (Bentron)
6 B.A. screws, nuts, and spacers
Stranded core p.v.c. wires; red, green, blue, orange, mauve, grey, yellow, and white
12in × 4in s.r.b.p. amplifier mount

Note: All transistors and cooler can be obtained from Rastra Electronics Ltd., 275–281 King Street, Hammersmith, W.6.

earth, and low drift with change in temperature when TR1 and TR2 are closely matched. The long-tailed pair also gives good rejection of drift induced by changes in supply voltage, and has a reasonably large input impedance at low collector current levels.

An input signal will undergo a phase change of 180 degrees between the base and collector of TR1, and the voltage datum level is shifted away from earth towards the positive rail voltage. Ignoring for the moment C1, the signal is passed straight to the base of TR3.

VR1, R5, and R7 form an adjustable potential divider across positive and negative supply rails, and the VR1 setting determines the working points of direct coupled stages TR3, TR4, and TR5. Front panel control VR15 sets the amplifier input at zero volts, while VR1 does the same for the output.

TR3, while contributing some voltage gain, also introduces another 180 degree change of phase, to bring the overall phase difference between the amplifier input and TR3 collector to zero. Obviously, the voltage at the collector of TR3 will be even closer to positive rail voltage than the collector of TR1, but this cumulative voltage shifting can be virtually eliminated by using a *pnp* transistor for TR4. At the same time, TR4 common emitter stage brings more voltage gain and another and final phase change of 180 degrees.

So, the situation at the collector of TR4, when VR15 and VR1 are at correct settings, will be no overall voltage shift, a total phase difference of 180 degrees, and a total voltage gain in the region of 5,000.

Finally, the addition of an emitter follower stage provides the low input impedance required for driving a variety of useful loads, without unwanted circuit complications. TR5 causes negligible further voltage shifting, adds no change of phase, and with a voltage gain very close to unity, will simply reduce the output impedance of the operational amplifier without modifying its other characteristics.

IMPORTANCE OF HIGH OPEN-LOOP GAIN

The ideal operational amplifier would have an infinite voltage gain when no feedback resistor was present, but since this is unattainable in practice, the effect of a finite open-loop gain on amplifier accuracy must be examined.

In Fig. 3.8, selected values of open-loop gain $-A$ are plotted against closed-loop gains $-G$, and percentage amplifier error. Closed-loop gains are normally restricted to 0·1–50 as this caters for almost all operational conditions, and it is seldom required to extend these limits. A different set of circumstances apply when the op-amp is used for integration, and these will be considered in detail later.

Very high $-A$ gains bring attendant drift and stability problems, and this in turn demands a larger number of components and more complicated circuitry to keep drift and stability within acceptable limits. At the opposite extreme, very simple amplifier circuits can

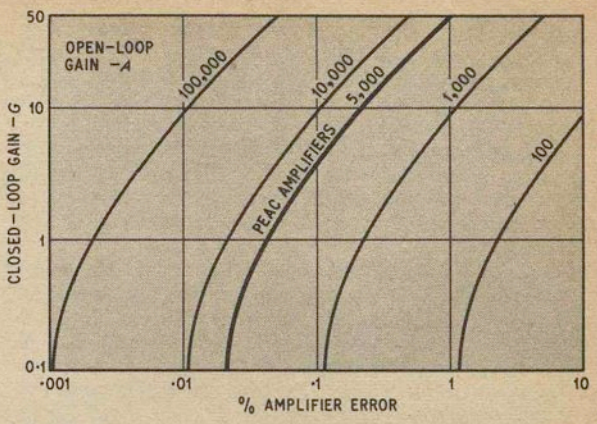


Fig. 3.8. Open-loop gain plotted against closed-loop gains and percentage amplifier error

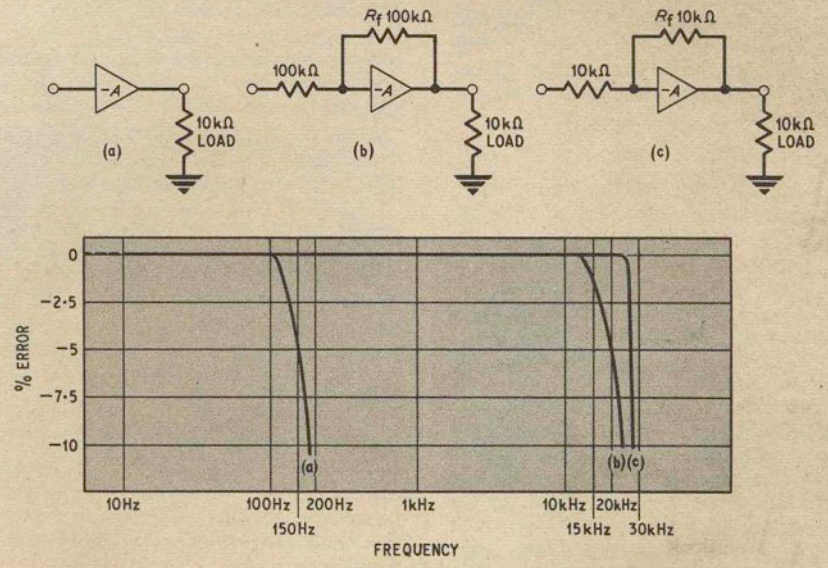


Fig. 3.9. Amplifier frequency response

TABLE 3.1

UNIT "A" OPERATIONAL AMPLIFIER. TYPICAL PERFORMANCE

Supply voltage ±12·5V ±0·5%
Open-loop voltage gain 5,000 d.c.—100Hz. 200 at 10kHz
Maximum output voltage ±10V for loads >2kΩ
±5V for loads >300Ω
Input impedance 40kΩ approx.
Input current 0·005μA for 1V out
Closed-loop frequency response 0–10kHz within 1% when R_f = 100kΩ
Equivalent input drift ±0·5mV per hour
Input offset voltage and current almost zero when amplifier correctly balanced
R.M.S. noise, referred to input with input open circuit 200μV
Normal maximum range of plug-in components
R_{in} 2–100kΩ
R_f 10–100kΩ
C_f 1–0·01μF
Stability unconditional with all normal problem layouts

be built to yield $-A$ gains in the region of 100–1,000, but when $-G$ approaches 50 the errors of such amplifiers would be near 10 per cent. Thus, if a low value for $-A$ was chosen, for the sake of simplicity, the range of available closed-loop gains would have to be restricted if the error was not to exceed one or two per cent, and this would place severe limitations on the operational flexibility of the amplifier.

It was assumed that PEAC operators would not wish to employ plug-in computing components with a selection tolerance better than, say, ±1 per cent. Therefore, the error contributed by the amplifier will preferably be less than external component errors, but not so small as to call for ridiculous extremes of circuit sophistication. The thickened curve of Fig. 3.8, corresponding to $-A = 5{,}000$, shows that the maximum error contribution of UNIT "A" amplifiers is 1 per cent or less for $-G$ gains of less than 50.

BANDWIDTH AND STABILITY

A direct coupled amplifier of the Fig. 3.7 type will display an almost constant phase change of exactly 180 degrees over a range of frequencies from d.c. to

about 20kHz. Thereafter, with increasing frequency, the phase angle will begin to shift until, at several hundred kHz, and especially when the amplifier has a high gain, sufficient positive feedback is present to cause sustained oscillation. To counteract this instability, small capacitors are suitably situated in the op-amp circuit to reduce gain at critical frequencies, and it follows that the use of such capacitors will place a limitation on the available frequency response of the amplifier.

C1 of Fig. 3.7 will block the unwanted high frequency content of incoming signals, and plays a major role in determining the bandwidth of the amplifier. If C1 is reduced in value, bandwidth will be increased, but so will the likelihood of instability. Needless to say, any form of instability will be highly detrimental to accuracy, and must be avoided at all costs. C2 works in a different way, by introducing negative feedback and consequent loss of gain at very high frequencies. Both capacitors act together to combat instability under the very varied conditions of operational amplifier use.

The measured frequency response of a representative UNIT "A" amplifier is given in Fig. 3.9, and is very linear up to the well-defined break frequencies of (a) open-loop, (b) with feedback resistor of 100 kilohm, and (c) when R_f = 10 kilohm.

DRIFT

If a d.c. amplifier is adjusted so that its output voltage is zero when there is no input signal, over an interval of minutes, hours, or days—depending on the amplifier, its power supply, and its surroundings—a spurious voltage will begin to appear at the output. A poor amplifier in adverse conditions will require frequent manual adjustments to keep its output at zero. Fortunately, drift errors are very small when an operational amplifier is used for summing and sign changing, due to the presence of a feedback resistor, and no adjustment of the amplifier will be called for during intervals of perhaps several hours, except in applications requiring a very high degree of accuracy. However, when the operational amplifier is being used as an integrator, with a capacitor in its feedback loop, it is quite possible for drift errors to exceed 1 per cent within a space of less than an hour if suitable precautions are not taken.

The figure quoted in Table 3.1 for drift is the amount of input voltage, either positive or negative, required at the amplifier summing junction to reset the amplifier output to zero after it has been allowed to drift for one hour following a preliminary computer warm-up period. In practical terms, a drift of about ±0·5mV

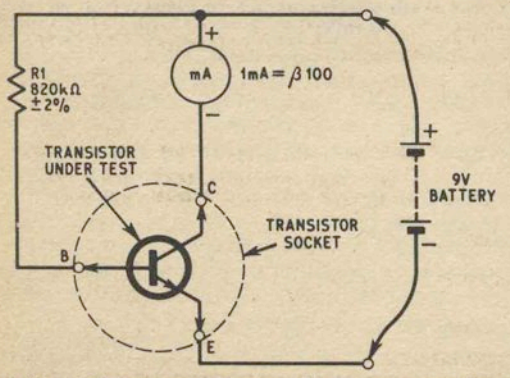
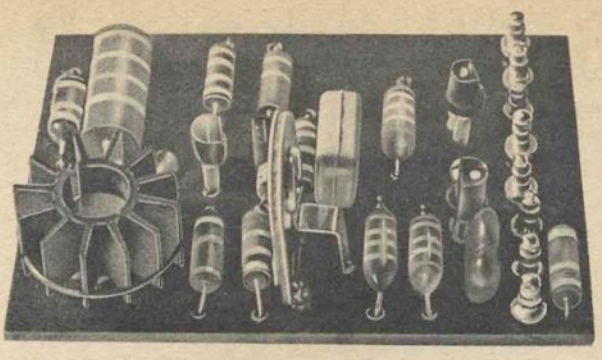


Fig. 3.10. Transistor test-rig. Note: reverse battery connections and milliammeter for pnp



per hour is not likely to prove to be too troublesome with most PEAC applications. Full scale analogue computers are sometimes installed in a temperature controlled computing room, and this considerably improves drift performance.

TRANSISTOR SELECTION

Several prototype UNIT "A" amplifiers were constructed using non-selected transistors, and about one third of the amplifiers failed to meet the specification of Table 3.1. Defects were due entirely to "spreads" in semiconductor characteristics, and disappointment will be avoided if all amplifier semiconductors are tested before use.

It has already been mentioned that the long-tailed pair input stage transistors (TR1 and TR2 in Fig. 3.7) should be matched. In all nine transistors of the same type will be required for TR1, TR2, and TR3 in the three operational amplifiers, and it will assist the matching and selection process if, say, one dozen transistors are purchased at the same time. No wastage will be involved as "spare" transistors can later be used up in other PEAC circuits.

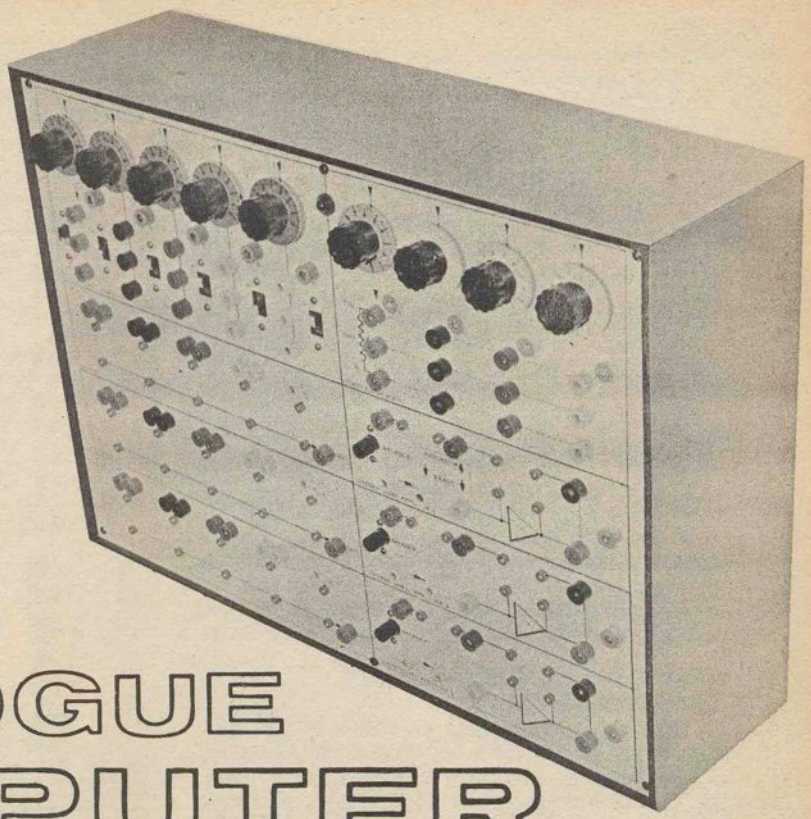
A simple test-rig circuit is given in Fig. 3.10 to facilitate the matching of TR1 and TR2, and the circuit can also be quickly adapted for checking other transistors. The test-rig could take the form of a transistor socket and resistor mounted on an odd piece of s.r.b.p., or Veroboard, with a testmeter employed as a milliameter.

Select each TR1–TR2 pair for near identical *betas* of 100 or more; this will dispose of six transistors. Do not attempt to pair off transistors of different types even if they do have the same *beta*. From the remaining transistors, choose three with the highest *beta* for TR3.

Although TR4 is a *pnp* transistor, it must be of silicon construction for low leakage drift. The majority of *pnp* silicon types at present on the market are unsatisfactory for use in the op-amp circuit because they exhibit almost no gain at all at very low collector current levels. Of all the types so far tested only the 2N3906 was found to be consistently good at low currents, therefore a suitable equivalent cannot be quoted. To check TR4, reverse the battery leads to the Fig. 3.10 test-rig, and switch connections to the milliameter before plugging in the *pnp* transistor. TR4 should display a *beta* of about 50 or more.

When handling plastic encapsulated transistors, which tend to look alike, take note that lead connections do not necessarily conform to a common pattern. In particular, notice the lead differences between types 2N2926 and its equivalent 2N3904, and remember that the 2N3906 is *pnp*. To avoid mishaps, always refer to Fig. 3.3 before applying current to the transistor.

By
D. BOLLEN



PEAC
ANALOGUE COMPUTER

THE constructional details for UNIT "A" were completed last month. UNIT "A" is, itself, a complete, self-contained computing equipment, and the method of operation, with practical examples, is described in this article.

PATCHING LEADS

The best plugs to use for patching the computer are those of "split-pin" construction, as they can quickly be attached to wires without the aid of a screwdriver. It is a help if plugs are obtained in various colours, and are mated to different coloured wires to allow easy identification.

For the majority of problems capable of solution by UNIT "A", certain patching leads may be left in position on the front panel. For example, coefficient potentiometers are almost always used with the "0" end of their resistance track connected to earth (link SK3 to SK4 for CP1, CP2, CP3, and CP4, Fig. 2.7).

Similarly, until such time as integrator mode switching is brought into use, the integrator sockets depicted in Fig. 2.9 are joined together by means of a special three-way patching lead consisting of two short lengths of wire joined by a plug, with a plug at each end. Looking at Fig. 2.9, OA1/SK4, SK9, and SK10 are linked, and repeat for OA2 and OA3. Three more semi-permanent patching leads are made up to link each operational amplifier to its companion summer network. Connect OA1/SK8 to S1/SK5, and do the same for OA2/SK8–S2/SK5, and OA3/SK8–S3/SK5.

The rearrangeable patching leads should be of assorted lengths and colours, the longest to patch from, say, CP4/SK2 to S3/I1/SK1, diagonally across the UNIT "A" front panel, and the shortest to link nearly adjacent sockets.

COMPUTING RESISTORS

If a comprehensive range of ± 1 per cent high stability computing resistors was purchased all at once, to meet every requirement, the cost would probably exceed £20. There are after all 101 preferred values in a ± 1 per cent range covering resistors from only 10 kilohm to 100 kilohm. Nevertheless, in the period when the computer operator is learning how to handle PEAC, and a high degree of accuracy is not essential, the majority of ordinary problem set-ups can be catered for by a small number of ± 1 per cent and ± 2 per cent plug-in resistors. A resistor selection list, with suggested values of R_f and R_{in} for standard op-amp closed-loop gains, is given in Table 4.1. Also, a component list included in this article sets out minimum quantities, with tolerances, of computing resistors.

Computing capacitors will be discussed later, in connection with integration.

SETTING UP THE VOLTAGE SOURCE

To set up all voltage source outputs, first remove the dials from VR6 to VR10 (Fig. 2.2), and turn the potentiometer spindles fully anticlockwise. If the potentiometers have flats on their spindles, make up blanking pieces consisting of small segments of hardwood or plastic, so that control knobs can be conveniently located at a selected position on each spindle. Connect the positive lead of a sensitive d.c. voltmeter (0–1V, 20 kilohm/V) to VS1/SK1, and the negative voltmeter lead to VS1/SK4 (Fig. 2.6), then set slide switch S1 for a positive voltage output. Switch on the computer power supply and S6.

Carefully rotate VR6 spindle clockwise until a very small voltage appears, just sufficient to slightly deflect

the meter pointer away from zero. Now place a dial knob on VR6 spindle, without disturbing the potentiometer setting, and align so that the "0" division on the dial is vertical and opposite the pointer mark on the surface of the front panel. Tighten the dial knob grub screw.

Switch off S6 and replace the 0–1V meter with the 0–10V d.c. meter which has been chosen to serve as a voltage standard for the computer, while retaining the same meter lead polarity. Rotate VR6 dial until the "10" division is opposite its pointer, and switch on S6. Now adjust slider resistor VR1 from the back of the UNIT "A" box, for a precise reading of 10V on the "standard" meter. Repeat the above procedures for outputs VS2, VS3, VS4, and VS5, and remember to adjust only the particular slider (VR1–VR5) which is associated with the output being set up.

When all the voltage source dials are aligned, return to VS1 and make sure that its output is still +10V. Switch off S6, reverse the "standard" voltmeter leads, and set S1 for a negative output. Switch on S6 again and check the voltmeter reading; if it is not exactly 10V, go to the back of the UNIT "A" box and trim the power pack control VR2 (Fig. 3.4), this ensures that voltage source negative and positive outputs are equal.

SETTING UP THE COEFFICIENT POTENTIOMETERS

Insert a patching lead to link CP1/SK3 to CP1/SK4 (Fig. 2.7), and do the same for CP2, CP3, and CP4. Take a long patching lead from VS1/SK1 to CP1/SK1. Remove the dial from VR11 (Fig. 2.5) and rotate spindle fully clockwise. With the negative lead connected to any earth socket, insert the "standard" meter positive lead into CP1/SK2 after first setting S1 for a positive output. Adjust VS1 dial for a meter reading of 10V. Rotate CP1 spindle carefully anti-clockwise until the meter pointer just beings to drop below the 10V division. Replace CP1 dial knob on VR11 spindle, align the "10" division with the pointer, and tighten the grub screw. Repeat for CP2, CP3, CP4.

With a 10V input to CP1/SK1, and a 0–10V meter connected to CP1/SK2, it is a simple matter to check the agreement between dial divisions and voltage output from the coefficient potentiometer. If there are serious discrepancies between voltage output and dial reading this will indicate that the effective electrical rotation of the potentiometer differs from the 270 degree dial calibration. Errors can often be minimised by slight readjustment of the dial knob on its spindle, to spread the error over the entire scale. Generally

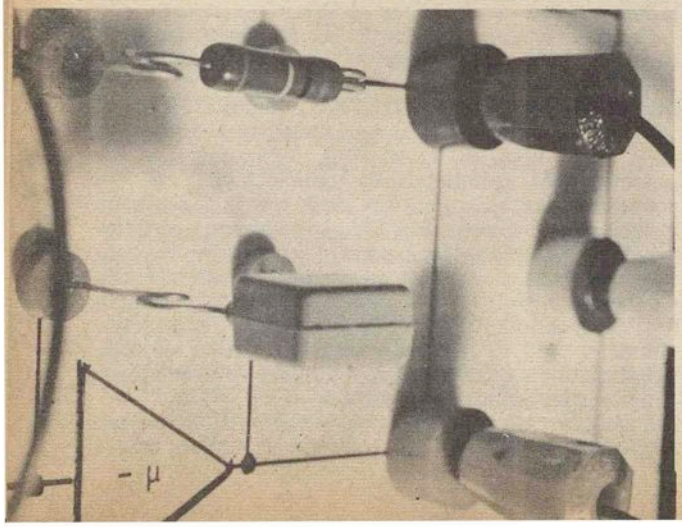


TABLE 4.1
SUGGESTED VALUES OF COMPUTING RESISTOR FOR STANDARD CLOSED-LOOP GAINS

Op-amp gain	All resistors ±2% unless otherwise stated	
$\frac{R_f}{R_{in}} = -G$	R_{in}	R_f
0·1	100kΩ	10kΩ
0·2	100kΩ	20kΩ
0·3	33kΩ	10kΩ
0·4	40kΩ ± 1%	10kΩ
0·5	20kΩ	10kΩ
0·6	33kΩ	20kΩ
0·7	13kΩ	9·1kΩ
0·8	20kΩ	16kΩ
0·9	20kΩ	18kΩ
1·0	10kΩ	10kΩ
	100kΩ	100kΩ
2·0	10kΩ	20kΩ
3·0	3·3kΩ	10kΩ
	33kΩ	100kΩ
4·0	4kΩ ± 1%	10kΩ
	40kΩ ± 1%	100kΩ
5·0	20kΩ	100kΩ
6·0	3·3kΩ	20kΩ
7·0	13kΩ	91kΩ
8·0	2kΩ	16kΩ
9·0	2kΩ	18kΩ
10·0	10kΩ	100kΩ
20·0	5kΩ ± 1%	100kΩ
30·0	3·3kΩ	100kΩ
40·0	4kΩ ± 1%	100kΩ
50·0	2kΩ	100kΩ

speaking, the dial setting error should not be worse than 5 per cent at all settings between "1" and "10" dial divisions. The whole question of computing potentiometer accuracy will be raised later, in connection with the Master Potentiometer of UNIT "B".

SETTING UP THE OPERATIONAL AMPLIFIERS

It is usual to check operational amplifiers either before the start of a computation, or at the beginning of the day, but the computer builder may wish to assure himself that his amplifiers are all that they should be when first brought into service. The zero-setting procedure given at the end of Part 3 of this series will have eliminated all but obscure faults. The front panel balance controls (VR15, VR16, and VR17, Figs. 2.4 and 2.9) are deliberately designed to have a limited range of adjustment, so that an amplifier fault will be clearly indicated as an inability to zero-set from the front panel.

To quickly check each amplifier, insert 10 kilohm feedback resistors into miniature sockets SK11 and SK12 for OA1, OA2, and OA3 (Fig. 2.9), and ensure that the operational amplifiers are already linked to their summing networks. Insert 10 kilohm input resistors into S1/I1/SK3–SK4, S2/I1/SK3–SK4, and S3/I1/SK3–SK4 (Fig. 2.8). Patch VS1/SK1 to S1/I1/SK1 (Figs. 2.6 and 2.8) and connect the negative lead of a voltmeter to OA1/SK13, with the positive lead going to any convenient earth socket.

Check that OA1 output is exactly zero when S6 is off. If not, zero-set by means of balance control VR15. Obtain a positive voltage from VS1 by switching on S6 and setting S1 and VR6, and monitor VS1 output with a second voltmeter connected to SN1/SK2 red, and an

COMPONENTS . . .

UNIT "A" COMPUTING RESISTORS AND PATCHING LEADS

Resistors

3 off 2kΩ ±2%
3 off 3·3kΩ ±2%
3 off 4kΩ ±1%
3 off 5kΩ ±1%
3 off 9·1kΩ ±2%
5 off 10kΩ ±1%
5 off 10kΩ ±2%
3 off 13kΩ ±2%
3 off 15kΩ ±2%
3 off 16kΩ ±2%
3 off 18kΩ ±2%
3 off 20kΩ ±2%
3 off 33kΩ ±2%
3 off 40kΩ ±1%
3 off 91kΩ ±2%
5 off 100kΩ ±1%
5 off 100kΩ ±2%

(All metal oxide or carbon film, 1 W)

Plugs

1 dozen of each colour: red, black, blue, yellow, and white, to fit front panel sockets (see text).
1 dozen miniature plugs, to fit miniature sockets

Wire

Stranded core single p.v.c. wires in assorted colours (14/·0076in).

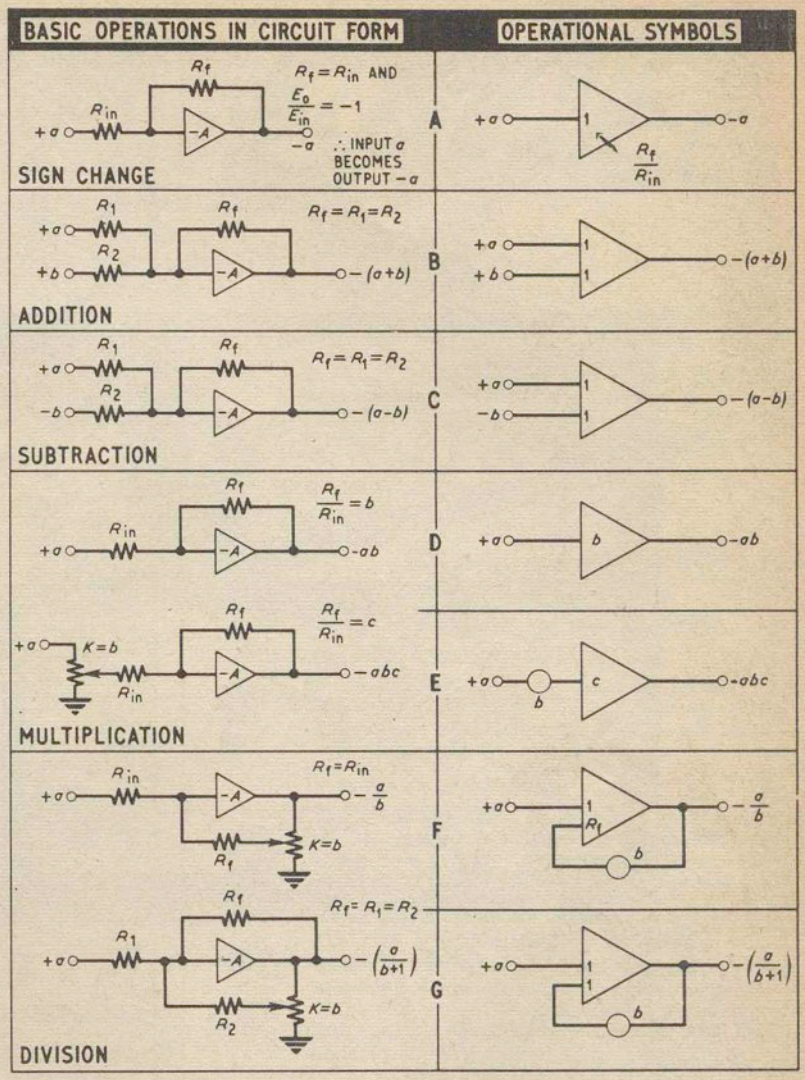


Fig. 4.1. (right) These diagrams indicate how the operational amplifier can be used to solve various algebraic equations

earth socket. Remember that a positive input voltage results in a negative operational amplifier output voltage.

Since input and feedback resistors are both 10 kilohm, the operational amplifier gain will be unity, and both voltmeters should give precisely the same readings. Double check by interchanging voltmeters. Now see that the operational amplifier will faithfully "track" any input voltage of ±10V or less when a temporary output load of 2 kilohm is connected from OA1/SK7 to earth.

The above tests are repeated for OA2 and OA3 by transferring the patching lead from VS1–S1/I1/SK1 to S2/I1/SK1, and then to S3/I1/SK1, and at the same time reconnecting voltmeters to the appropriate summer and operational amplifier sockets.

SOFTWARE

Under the heading of "software" comes all the paperwork associated with drawing up a programme for the computer. The time spent on preparing a programme for PEAC can vary from a few minutes to several days, depending on the skill of the programmer and the nature and complexity of the problem.

The intention is to give a few typical programme examples as an introduction to using the computer. They will consist of a short written *routine*, plus programme layouts. The layouts will be in a duplicated form, of symbolised diagram and patching circuit, so that the reader can compare analogue computer symbols with actual circuits and patching procedures. A newcomer to analogue computers will best learn programming techniques by working with PEAC, and this will also help to increase his knowledge of more advanced mathematics.

ROLE OF THE OPERATIONAL AMPLIFIER IN EQUATION SOLVING

Now that the time has come to consider UNIT "A" as a computer, instead of as a collection of circuits handling voltages, it is appropriate to adopt a slightly different approach. Voltages will now be replaced by the letters or numbers of an algebraic equation, *a*, *b*, *c*, *d*, *x*, *y*, 2, 3, 4, 5, and so on. Computing resistors loose their individual identity and are considered only as ratios $\frac{R_f}{R_1}$, $\frac{R_f}{R_2}$, etc., which are also denoted by equation letters or numbers. The same applies to coefficient potentiometer settings.

Sign change. In the circuit of Fig. 4.1a, an input voltage classified as term *a*, reappears at the op-amp

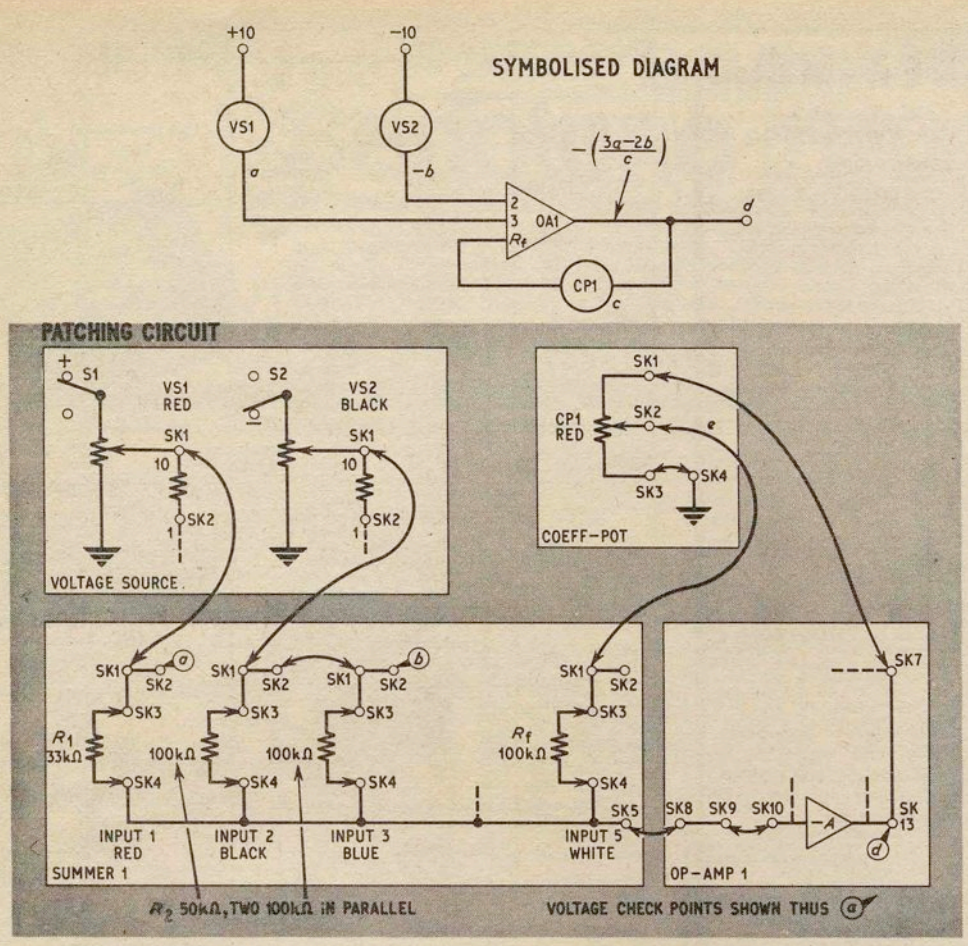


Fig. 4.2 Programme layouts for $\frac{3a-2b}{c}=d$

output as term $-a$, when the $\frac{R_f}{R_{in}}$ ratio is unity. One way of looking at this operation, which is common to all single operational amplifier configurations, is to assume that a has been multiplied by -1, hence $\frac{R_f}{R_{in}}=-1$. In effect, to multiply by -1 is to move a mathematical term from one side of its equation to the other, so sign change can be used to transpose.

The operational symbol of Fig. 4.1a avoids the bother of inserting resistors and their values when drawing up a programme layout on paper. The figure inside the triangle—in this case "1"—merely indicates that the computing resistor ratio, or alternatively the operational amplifier gain, is unity.

Addition. In Fig. 4.1b, positive terms a and b are added to yield an output $-(a+b)$, which can also be written $-a-b$. If $-(a+b)$ is applied as an input to a second unity gain operational amplifier, to give two sign changes, it will be converted to $a+b$. Note that the figures in the operational symbol triangle show that $\frac{R_f}{R_1}=1$, and $\frac{R_f}{R_2}=1$.

Subtraction. The only difference between Fig. 4.2b and Fig. 4.2c is that term b has been made a negative quantity. The operational amplifier output is therefore $-(a-b)$ or $-a+b$.

Multiplication. In Fig. 4.1d, R_f and R_{in} are adjusted so that $\frac{R_f}{R_{in}}=b$. Hence, a is multiplied by factor b to become an output $-ab$. The letter inside the operational symbol triangle shows that the $\frac{R_f}{R_{in}}$ ratio is b.

Fig. 4.1e gives an alternative method of achieving multiplication. A computing potentiometer is connected to the op-amp input to multiply a by a factor b. Therefore, with an input ab, and $\frac{R_f}{R_{in}}$ adjusted to equal c, the result is an output $-abc$.

Division. When a computing potentiometer is wired as in Fig. 4.1f, with R_f connected to its slider, term a will be divided by constant b when $R_f=R_{in}$. Note that R_f is written inside the symbol triangle to show that b is a divisor.

It can sometimes happen that a feedback resistor is inadvertently left plugged into an operational amplifier when it is re-programmed for a division operation, and this will result in the circuit of Fig. 4.1g. Instead of an output $-\frac{a}{b}$ the operational amplifier will yield $-\left(\frac{a}{b+1}\right)$.

COMBINED OPERATIONS

The configurations of Fig. 4.1 have many similarities, which lead naturally to the combination of several operations. In fact, it is possible to perform, say, ten additions or subtractions, three multiplications, and one division operation all at once using a single operational amplifier with several inputs and coefficient potentiometers.

PROBLEM EXAMPLE 1.
SOLVING A SIMPLE EQUATION

UNIT "A" can solve a linear algebraic equation consisting of more than ten unlike terms, but a simple example with only four terms will serve as an adequate practical introduction to programming.

Take $$\frac{3a - 2b}{c} = d \qquad \text{(Eq. 4.1)}$$

the letters a, b, and c are regarded as known quantities, and d is the unknown, but the equation can be transposed to solve for any unknown.

Eq. 4.1 is implemented on the computer as shown in the Fig. 4.2 patching circuit. Two voltages corresponding to a and $-b$ are taken from the voltage source to summer S1, where a is multiplied by $\frac{R_f}{R_1} = 3$, and $-b$ is multiplied by $\frac{R_f}{R_2} = 2$.

The machine equation for the problem is,

$$\frac{\frac{R_f}{R_1}a - \frac{R_f}{R_2}b}{c} = d \qquad \text{(Eq. 4.2)}$$

and if R_f is made 100 kilohm the equation will take the form of

$$\frac{\frac{100}{33}a - \frac{100}{50}b}{c} = d \qquad \text{(Eq. 4.3)}$$

Computing resistor values could equally well be $R_f = 10$ kilohm, $R_1 = 3{\cdot}3$ kilohm, and $R_2 = 5$ kilohm, to yield the same multiplication ratios. Since a 50 kilohm resistor is not included in the short list of Table 4.1, two 100 kilohm resistors are patched together in parallel in the patching circuit Fig. 4.2.

Routine. To set up Eq. 4.1 on UNIT "A", first of all ensure that the voltage source switch S6 is off. Insert computing resistors into the positions shown in Fig. 4.2 patching circuit, and connect the computing elements together with patching leads. Set VS1 and VS2 dials to zero, and CP1 to "10", corresponding to a divisor of 1. Wire a voltmeter to OA1/SK13 and zero-set the operational amplifier by means of VR15. Next connect a voltmeter to S1/I1/SK2, and switch on S6. Set VS1 dial for a trial value of $a = 2$V. Transfer the voltmeter from S1/I1/SK2 to S1/I3/SK2, and set VS2 dial for a trial value of $b = -2$V.

UNIT "A" will now be computing

$$\frac{(3 \times 2) - (2 \times 2)}{1} = 2 \qquad \text{(Eq. 4.4)}$$

with $a = 2$, $b = -2$, $c = 1$, and therefore $d = 2$. When a voltmeter is linked to OA1/SK13 it will be discovered that the output voltage d is actually -2V, due to the operational amplifier sign change. Remedy by reversing the readout meter leads. If the output voltage is not exactly -2V, recheck voltages for a and $-b$. To check the exact setting of CP1 dial for any value of c, temporarily remove the patching lead from CP1/SK1. Patch CP1/SK1 to a precise $+10$V from a spare voltage source output, and connect a voltmeter to S1/I5/SK2. The voltmeter will then indicate the potentiometer coefficient while taking into account the loading effect of R_f (see Fig. 4.3). A voltmeter reading of 4·75V is equivalent to a coefficient of 0·475. CP1 can now be patched back into the problem set-up. With a 100 kilohm resistor for R_f, CP1 will be dividing by numbers equal to or less than unity. If R_f is changed to 10 kilohm, the range covered by CP1 will become 0–10. Therefore, increasing c by a factor of 10 can be seen quite clearly to be the same as decreasing computing resistor ratios by a factor of 10.

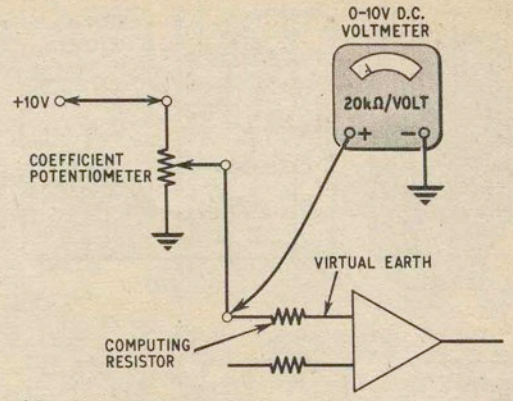


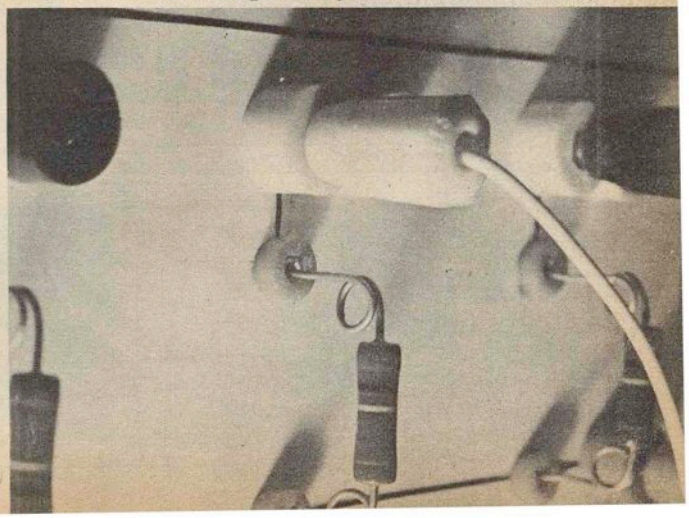
Fig. 4.3. Voltmeter method of determining coefficient potentiometer settings

With UNIT "A" now programmed for Eq. 4.1, it is possible to investigate fully the problem for all reasonable values of a, b, c, and d, and for any unknown without the need for transposing terms or altering the problem set-up. For example, to find a when b, c, and d are known, set b and c and adjust a for an operational amplifier output equal to d. Always monitor an input voltage with a voltmeter when it is being adjusted.

To see how serious computing errors can occur at extreme limits, set VS1 and VS2 so that terms $3a$ and $-2b$ are virtually equal, and $d \simeq 0$. Also, set CP1 to near zero and observe that d will pass beyond the 10V operational amplifier maximum output swing.

PROBLEM EXAMPLE 2.
ANALYSIS OF VOLTAGE DIVIDER CIRCUIT

The voltage divider of Fig. 4.4a is often encountered in electronic circuits. At first sight, a network consisting of only two resistors might be considered far too simple to merit investigation by means of a computer,



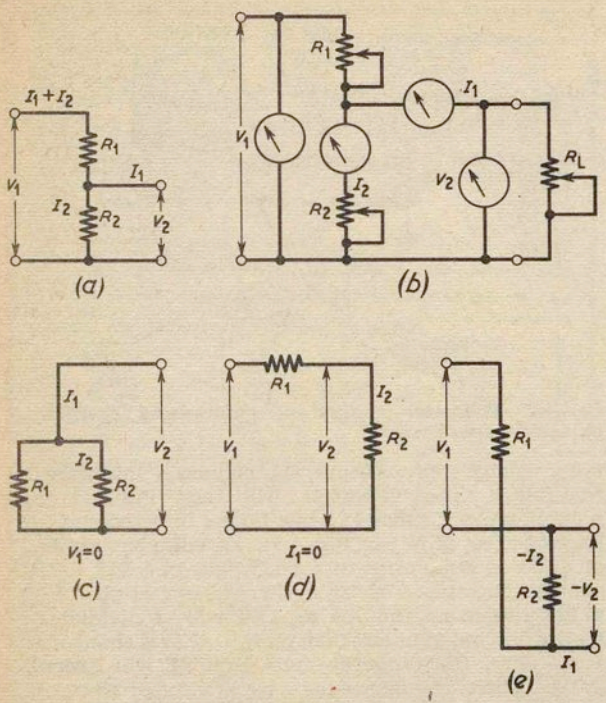


Fig. 4.4. (a) voltage divider circuit; (b) direct simulation of (a); (c), (d) and (e), three variations on (a)

but it does involve at least six variable quantities V_1, V_2, I_1, I_2, R_1, and R_2, and to solve a problem for any unknown, one of six equations would be required, based on

$$R_1 = \frac{V_1 - V_2}{I_1 + I_2} \qquad \text{(Eq. 4.5)}$$

and

$$R_2 = \frac{V_2}{I_2} \qquad \text{(Eq. 4.6)}$$

Thus, although it would be ridiculous to use the computer to find one specific answer to one particular voltage divider problem, the paperwork involved in solving six equations for several sets of variables could become surprisingly laborious. What the computer does in fact allow is the solution to literally any voltage divider problem under any conditions, without the need for re-programming.

To solve Eq. 4.5 and Eq. 4.6 simultaneously on UNIT "A', the equations are first transposed for terms V_2 and I_2, which are common to both.

$$V_2 = V_1 - R_1(I_1 + I_2) \qquad \text{(Eq. 4.7)}$$

and

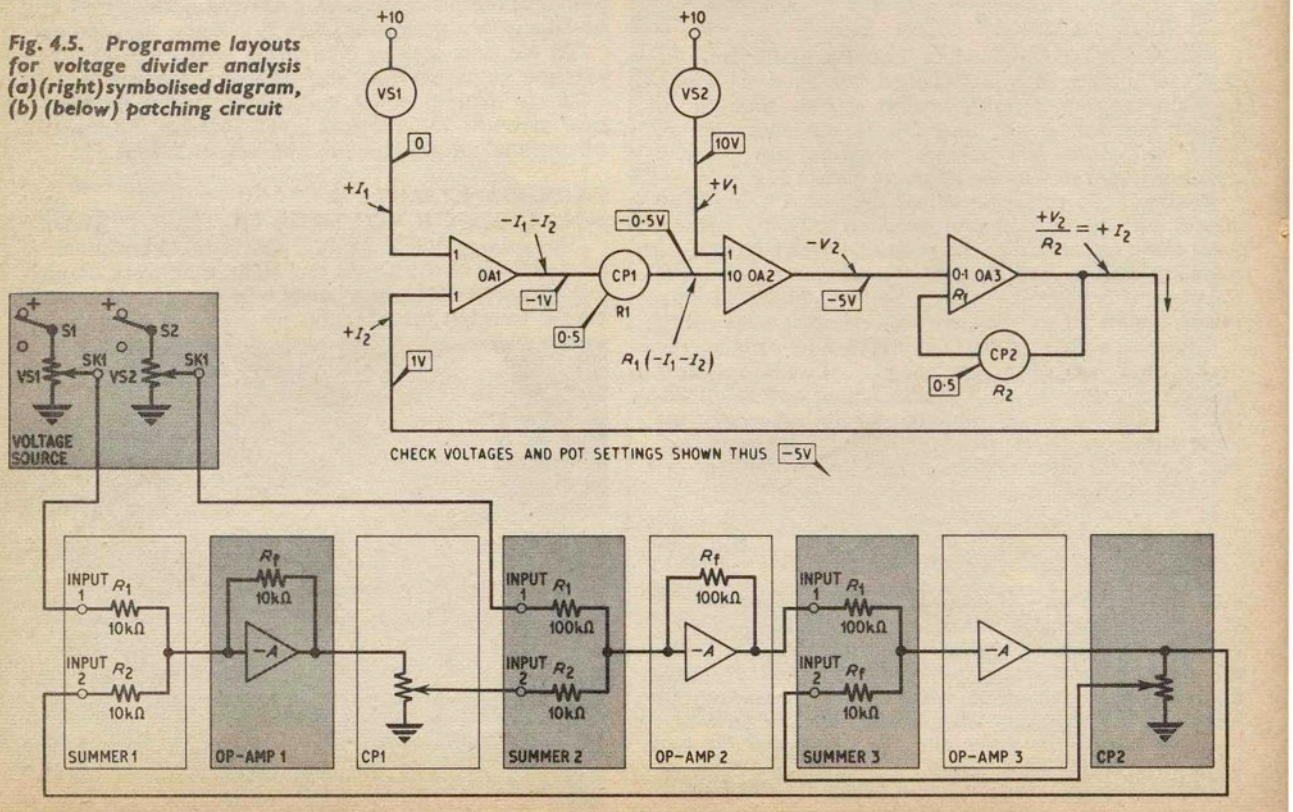
$$I_2 = \frac{V_2}{R_2} \qquad \text{(Eq. 4.8)}$$

Next, both equations are linked to give a self-enforcing systems, shown diagrammatically as,

$$V_1 - R_1(I_1 + I_2) = V_2 \longrightarrow \frac{V_2}{R_2} = I_2$$

where the answer to Eq. 4.5 is one of the terms of Eq. 4.6 (V_2), and the answer to Eq. 4.6 is one of the

Fig. 4.5. Programme layouts for voltage divider analysis (a) (right) symbolised diagram, (b) (below) patching circuit



terms of Eq. 4.5 (I_2). To see how the problem is set-up on the computer, refer to Fig. 4.5, and note the changes of sign involved.

Routine. Switch off S6 and insert all computing resistors and patching leads, except the link between OA3 output and OA1 input, which carries the voltage analogue of I_2. Zero-set OA1, OA2, and OA3 in that order, using a voltmeter applied to each operational amplifier output socket in turn. Now patch the link between OA3 output and OA1 input into circuit. Set VS1 to "0", and VS2 to "+10". The voltmeter method of Fig. 4.3 is employed to set CP1 and CP2 both for a coefficient of 0·5. Temporarily remove the patching leads from CP1/SK1 and CP2/SK1, and connect the "top end" of the potentiometer tracks to a 10V reference voltage. Adjust CP1 and CP2 for outputs of 5V. Exactly the same procedure is adopted when it is necessary to "read off" values for R1 and R2, although approximate readings can be taken from CP1, CP2 dials.

The check voltages in the diagram of Fig. 4.5 correspond to the above voltage source and coefficient potentiometer settings, and provided that there is general agreement with Ohm's law, any desired values can be given to the voltages, currents, and resistances in Fig. 4.4a. The check voltages could apply to actual voltage divider quantities of, say, $V_1 = 10V$, $V_2 = 5V$, $I_1 = 0mA$, $I_2 = 1mA$ (1 machine volt = 1mA), $R_1 = 5$ kilohm, and $R_2 = 5$ kilohm, where VS1 covers the range 0–10mA, VS2 0–10V, CP1 0–10 kilohm, and CP2 0–10 kilohm. Suppose instead that V_1 had been assigned the value of 1,000V, when R_1 and R_2 were both only 5 ohms. One machine volt would now be equivalent to 100A, and V_2 would equal 500V. The ranges covered by computing potentiometers in the latter case would then be VS1 0–100A, VS2 0–1,000V, CP1 0–100, and CP2 0–10 ohms.

Unless informed otherwise, the computer assumes that V_1 is an ideal voltage which originates from a source of infinitely small resistance. Hence, if $V_1 = 0$, this corresponds to a short-circuit, and gives the variation of Fig. 4.4c. Alternatively, if I_2 is made equal to nought, the voltage divider circuit is transformed into a load resistor R_2 in series with a source resistor R_1. given by Fig. 4.4d.

One further variation will serve to show the flexibility of the programme. In Fig. 4.4e the resistance network R_1 and R_2 is made to couple two sources of voltage V_1 and $-V_2$, and this occurs when I_1 is made larger than $I_2 + I_2$, or in other words, when I_2 swings negative.

The layout of Problem Example 2 is an instance of indirect simulation, where the computer solves equations and imitates the behaviour of the simulated circuit. In this indirect "model" of a voltage divider, relationships between governing equations and actual circuit parameters are made obvious, and the abstractions of mathematics are brought to life as tangible voltmeter and dial readings.

Another way of simulating the Fig. 4.4a circuit is by a direct "model", shown in Fig. 4.4b, which employs coefficient potentiometers for R_1, R_L, and R_L, voltmeters for V_1 and V_2, and current meters for I_1 and I_2. Although feasible, the direct model is less elegant, is not so adaptable to extreme cases, and is subject to errors which do not occur when the voltage divider is simulated indirectly.

Next month: Using UNIT "A" to solve a second order differential equation. Indirect simulation of LC circuits, spring pendulums, and servo-mechanisms by means of integrators.

REGULATED POWER SUPPLY

continued from page 284

	VOLTS						mA	A
	A	B	C	D	E	F	I_2	I_1
No load current	1·0	0·17	14·2	0·68	0·47	2	65	2·7
	2·88	0·145	11·4	0·5	0·38	6	40	2·1
	5·8	0·12	7·0	0·36	0·28	12	18	1·4
1A Load	0·99	0·165	14·1	0·61	0·40	2	36	1·9
	2·86	0·143	11·3	0·41	0·30	6	18	1·3
	5·78	0·119	6·9	0·23	0·17	12	3·5	0·32

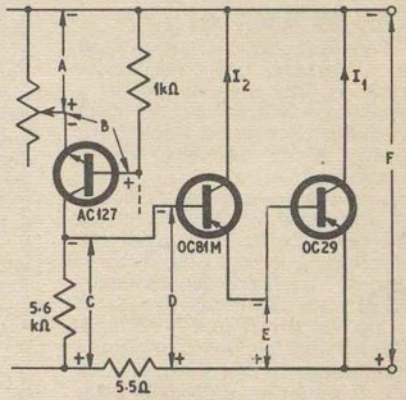


Fig. 10. Test measurements for fault-finding

CALIBRATION OF OUTPUT VOLTAGE

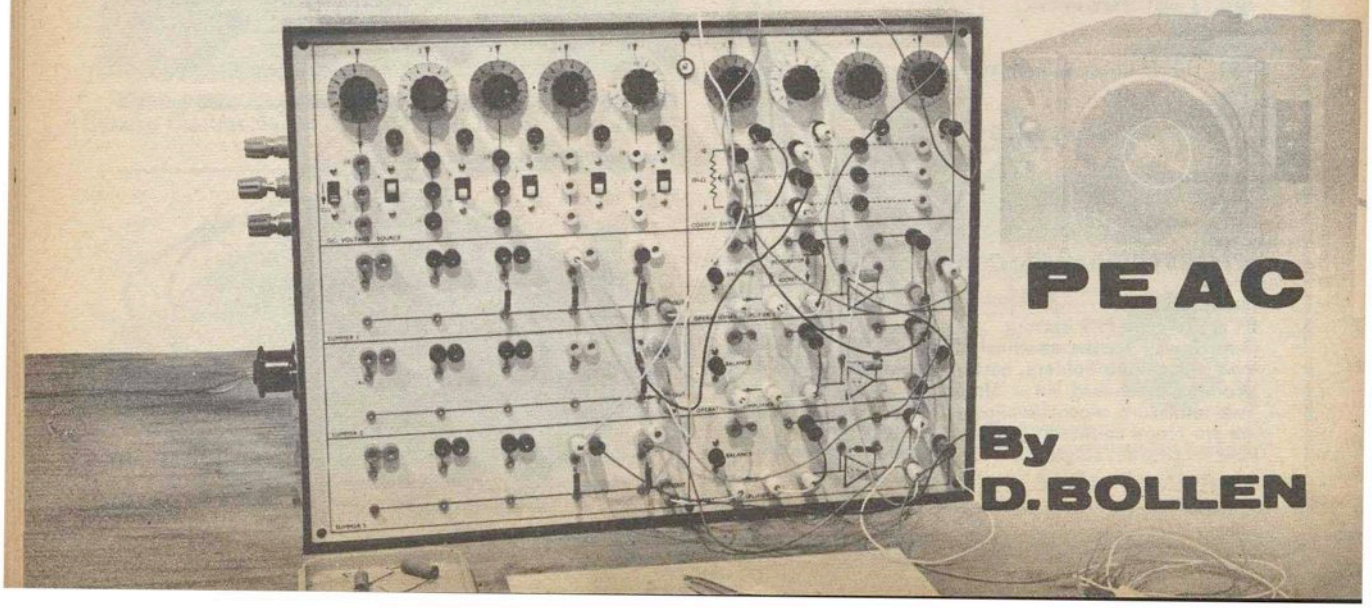
After checking the voltmeter accuracy against an AVO or similar instrument known to have good accuracy itself, the Regulated Volts dial should be adjusted as follows.

Switch S2 to "Regulated" and S3 to "Volts" and turn VR1 until 1V is obtained at the output (best seen on the AVO). Loosen the knob and rotate to indicate 1V on the calibrated dial. Lock the pointer knob grub screw while indicating the correct 1V. Rotate VR1 until the dial indicates 12V output. Now adjust VR2 until 12V output (measured) is obtained.

VOLTAGE CHART

Fig. 10 gives typical voltages at six points in the d.c. amplifier circuit for three different output voltages. Reference to these voltages and to the currents of the super-alpha pair TR2, TR3 should assist in any fault-finding. ★

ANALOGUE COMPUTER



By D. BOLLEN

THE detailed explanation concerning the operation of UNIT "A" is continued in this month's article, with further practical examples.

We resume by considering the use of the operational amplifier as an integrator.

An operational amplifier will be handling time as well as voltage when acting as an integrator, so some means must be found of inserting intervals of time onto the computer. One method is to employ external oscillators to provide known functions of time in terms of frequency. An input to an integrator might consist of a steady d.c. voltage which is switched on for a time t (step function or square wave), or alternatively, a sinusoidal voltage of frequency f and period $1/f$.

If a graph is drawn of the resulting integrator output function, and this is the form that answers to problems involving change or motion will usually take, the X axis of the graph will be calibrated in intervals of time, with voltage on the Y axis. It follows that an oscilloscope, which also uses time on the X axis and voltage on the Y axis, can provide a convenient form of output display, especially when an integrator is operating at high speed.

The operational amplifier is converted to an integrator when a capacitor C_f is inserted, in place of a resistor, in the feedback path; see Fig. 5.1. When an input voltage $-E_{in}$ is applied to the integrator by means of a simple switch S for a time t, the output E_o will take the form of an increasing ramp voltage proportional to t with slope

$$-E_{in}\ \frac{1}{R_{in}C_f}$$

Note that the operational amplifier will continue to invert an input voltage even when used as an integrator.

THE INTEGRATOR IN EQUATION SOLVING

The electronic analogue computer does provide a powerful technique for obtaining rapid solutions to problems involving calculus, which cannot be equalled either by numerical methods or by a digital computer.

If differentiation and integration are regarded as straightforward mathematical operations, it will be found that the terms of, say, a second order differential equation can be manipulated on the computer in much the same way as the terms of a "steady state" algebraic equation.

For example, when an equation term y is differentiated against time its derivative dy/dt is obtained, and a second differentiation yields the second derivative d^2y/dt^2. The reverse process is where integration of the second derivative d^2y/dt^2 produces the first derivative dy/dt, and another integration gives y as the result.

Fig. 5.2 shows how a simple integrator can handle equation terms. Combined operations are made possible by cascading integrators, while using coefficient potentiometers and computing component ratios for summation, multiplication, and division (Fig. 4.1).

The process of differentiation, although feasible if care is taken, is generally avoided on analogue computers because it gives rise to unstable operational amplifier configurations, but this imposes only a slight limitation since integration can be employed—in the majority of cases—in place of differentiation.

INTEGRATOR ACCURACY

The transfer accuracy of an operational amplifier, when it is used as an integrator, will be theoretically limited by its finite value of open-loop gain. However,

TABLE 5.1

C_f	R_{in}	t
1μF	100kΩ	2·8sec
	10kΩ	800ms
0·1μF	100kΩ	280ms
	10kΩ	80ms
0·01μF	100kΩ	28ms

Maximum value of t for an error of 1%

the situation is much more complicated than with, for example, a summing amplifier (Fig. 3.8) since the amplifier error can no longer be defined in terms of the simple relationship between closed-loop and open-loop gains.

As a guiding principle, integrating amplifiers may have very large values of closed-loop gain provided that the time t of an input function remains small. Closed-loop integrator gains of 1,000 or more are not uncommon in transistor computers, since low voltages and low impedances discourage the use of computing resistors of more than 100 kilohm, and capacitors of more than 1μF are too bulky. Table 5.1 is calculated for UNIT "A" amplifiers, and sets out the maximum allowable interval t for selected values of C_f and R_{in}, where the amplifier transfer error must not exceed one per cent.

Errors due to unwanted drift voltages also become significant when t is long and C_f is small. The greatest care must be exercised when zero-setting integrators to eliminate offset voltages, for good accuracy at long time intervals. Also, the computer should not be subjected to fluctuations of ambient temperature when computations cover several hours of integrator use.

COMPUTING CAPACITORS

The computing capacitors used for PEAC will normally lie within the range 0·01–1μF, and the three values most commonly employed are 0·01μF, 0·1μF, and 1μF. Polystyrene is the preferred capacitor dielectric, for high insulation resistance, but polyester makes an acceptable second best. Mica, paper, and ceramic capacitors should be avoided.

Small value polystyrene capacitors of ±1 per cent and ±2 per cent tolerance are easily obtained, but 0·1μF and 1μF precision components are rare and expensive. To get around this difficulty, the bridge circuit of Fig. 5.3 was devised to allow computing capacitors to be made up from specially selected low cost ±20 per cent capacitors.

The circuit of Fig. 5.3 can be constructed in breadboard form on Veroboard or s.r.b.p., with miniature sockets to take C_x and R1. If an audio signal generator is not available to supply the bridge with about 10V r.m.s. at 1kHz, a signal could be obtained from a transistor multivibrator powered by the 25V computer power supply. Headphones serve to detect the null point when the bridge is in balance, and should have an impedance of about 2 kilohms.

The method of making up a computing capacitor of, say, 1μF is as follows. A capacitor panel of plain or perforated s.r.b.p. is fitted with small turret tags as in Fig. 5.4. A ±20 per cent capacitor of about 0·68μF is wired into position on the capacitor panel before it is plugged into the bridge C_x sockets, and a 1 kilohm

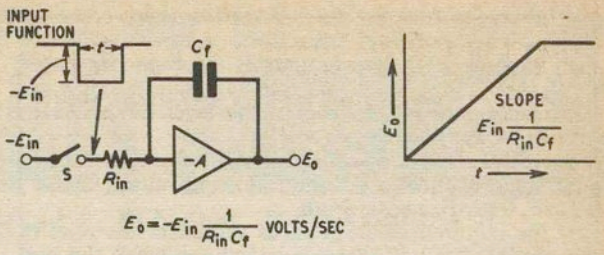


Fig. 5.1. The operational amplifier as an integrator

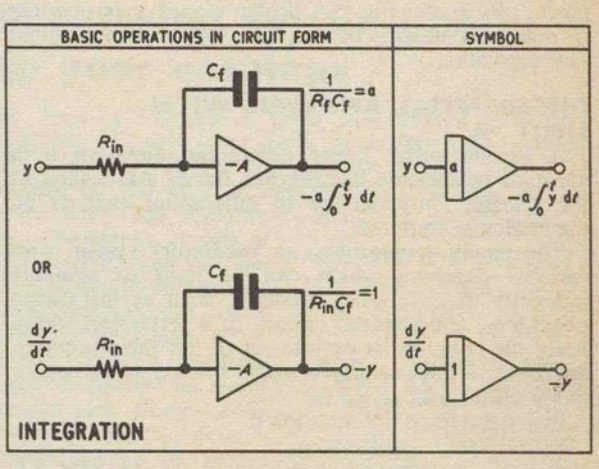


Fig. 5.2. The handling of equation terms by a simple integrator

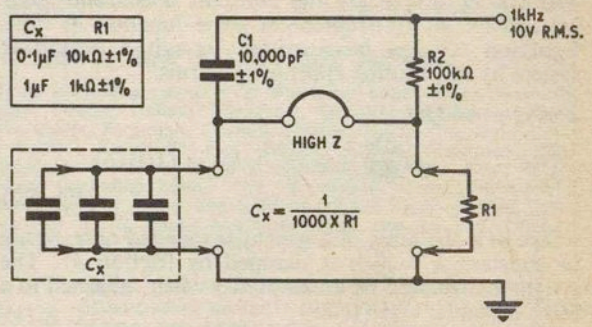


Fig. 5.3. Bridge circuit used for making up computing capacitors

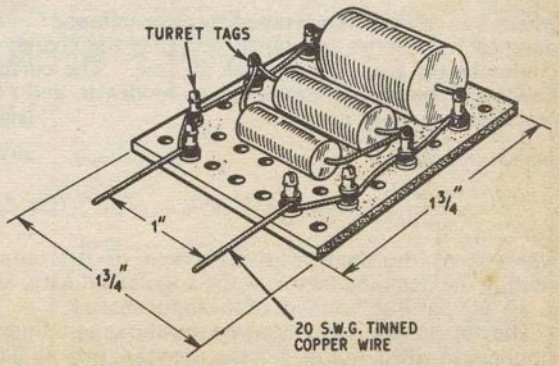


Fig. 5.4. Computing capacitor plug-in panel

resistor is inserted for R1. Assorted polystyrene or good quality polyester capacitors of lower value are then temporarily connected across the capacitor panel to increase C_x by small increments, while listening on the headphones for a drop in the level of the 1kHz tone as C_x approaches 1μF.

A typical computing capacitor might finally consist of a parallel combination of the following values, 0·68μF, 0·22μF, 0·02μF, and 0·005μF.

If the required value of C_x is exceeded, the note in the headphones will increase in volume when the null point is passed. Allow capacitors to cool off after soldering, and before making a measurement, as heat can cause a temporary or permanent change in capacitance. With the Fig. 5.3 bridge circuit it is possible to detect increments of less than 0·01μF in a nominal 1μF capacitor.

DIFFERENTIAL ANALYSIS WITH UNIT "A"

A second order linear differential equation with constant coefficients has become firmly established as the "classic" introduction to differential analysis on the analogue computer.

The equation describes an oscillatory system with variable damping which can be used to simulate indirectly many physical systems, such as the spring pendulum, a tuned *LC* circuit, or a servomechanism. Also, the equation is easy to set up on the computer, and does not necessarily demand the use of integrator mode switching.

In general form the equation is,

$$a\frac{d^2y}{dt^2} + b\frac{dy}{dt} + cy = f(t) \qquad \text{(Eq. 5.1)}$$

where a, b, and c are the constant coefficients, y is unknown, and $f(t)$ represents some function of time. Equation 5.1 can be rewritten to suit a particular system by substituting appropriate terms.

Spring pendulum

$$m\frac{d^2y}{dt^2} + \mu\frac{dy}{dt} + ky = f(t) \qquad \text{(Eq. 5.2)}$$

where m is the mass of a weight suspended on a spring of constant k, which is damped by friction μ. The weight is displaced by an amount y when subjected to a force dependent on $f(t)$.

Tuned LC circuit

$$L\frac{d^2Q}{dt^2} + R\frac{dQ}{dt} + \frac{1}{C}Q = f(t) \qquad \text{(Eq. 5.3)}$$

where L is an inductance tuned by a capacitance C, and damped by a series resistance R. Q is the charge in coulombs on C at any instant of time. The current flowing in the tuned circuit is given by dQ/dt, and $f(t)$ represents an input function.

Servomechanism

$$\frac{d^2\theta_o}{dt^2} + 2\zeta\omega\frac{d\theta_o}{dt} + \omega^2\theta_o = \omega^2\theta_i \qquad \text{(Eq. 5.4)}$$

where θ_o is the angular displacement of the output shaft, ζ the damping factor, ω the angular velocity, and θ_i the angular displacement of the input shaft.

The obvious similarity between the above equations is emphasised when, in Fig. 5.5, it is seen that they all have virtually the same problem layout on the computer. Furthermore, as the computer will allow operation at almost any fraction or multiple of real time, a spring pendulum and a tuned *LC* circuit can be simulated simultaneously, and interesting electro-mechanical parallels can be seen to exist between the properties of inductance and mass, resistance and friction, and capacitance and elasticity.

The only real difference between the analogous behaviour of a weight on a spring, a servo shaft, and a tuned *LC* circuit is that the *LC* combination will normally resonate at a much higher frequency.

PROBLEM EXAMPLE 3. TUNED CIRCUIT ANALYSIS

UNIT "A" will simulate any series tuned circuit by solving Equation 5.2, and will give answers in the form of a.c. meter readings or oscillograms. Tuned circuits resonating in the MHz region are catered for by slowing down the problem to some convenient decadal fraction of real time, so that a simulated circuit on the computer which is, for example, resonating at 300Hz, will serve as a model for a real circuit resonating at 30MHz, with suitable rescaling of L, C, and t.

To initially determine the relative values of L, C, R, voltage V, and current I, without too much paperwork, it is helpful to start with a representative tuned circuit which allows computer operation in real time, at frequencies convenient for display by an a.c. voltmeter or an oscilloscope. 50Hz is a good frequency to employ as a datum because it can be readily obtained from the mains supply, and rounded values of $L = 1$H and $C = 10\mu$F will also offer resonance at 50Hz.

Taking the circuit of Fig. 5.6a as a starting point, from the knowledge that a series tuned circuit will exhibit an impedance equal to R at resonance, the r.m.s. current flow at 50Hz will be E_i/R, or 20mA when $E_i = 2$V r.m.s. and $R = 100$ ohms.

It is necessary to rearrange the basic equation, Equation 5.2, for the computer by dividing through by L, and solving for the second derivative.

$$\frac{d^2Q}{dt^2} = -\frac{R}{L}\frac{dQ}{dt} - \frac{1}{LC} + \frac{f(t)}{L} \qquad \text{(Eq. 5.5)}$$

Substituting known values from Fig. 5.6a,

$$\frac{d^2Q}{dt^2} = \frac{100R}{1\text{H}}\frac{dQ}{dt} - \frac{1}{1\text{H} \times 10^{-5}C}Q + \frac{f(t)}{1\text{H}} \qquad \text{(Eq. 5.6)}$$

$f(t)$ in the present case represents a sine wave input of 2V r.m.s. In other circumstances the input function could be a square wave of amplitude E_{in} and period $2t$.

Equation 5.6 is solved on the computer by successive integration. Looking at the symbolised diagram of Fig. 5.6b, it can be seen that there are two closed-loops, one linking the output of OA1 via CP1 to OA1/Input 1, and the other passing through OA1, OA2, and OA3, via CP2, and thence back to OA1/Input 3. The coefficient of CP1 will be multiplied by the gain factor associated with OA1/Input 1. CP2 coefficient is multiplied by the product of gains OA1/Input 3, OA2, and OA3, i.e. 1,000 × 100 × 1 = 100,000.

d^2Q/dt^2, obtained from the sum of the voltages present at the inputs of OA1, is initially assumed to be present. After one integration OA1 provides an output dQ/dt, and from this all the terms on the right hand side of Equation 5.6 are assembled. So, dQ/dt is multiplied by $R/L = 100$, using CP1 set for a coefficient of 0·1, and is taken back to OA1/Input 1 where it is then added to $f(t)/L = 2$V r.m.s.

Moving in the other direction on the symbolised diagram of Fig. 5.6b, dQ/dt is integrated by OA2 to obtain $+Q$. Inverting amplifier OA3 changes the sign of Q before passing it on for multiplication by $1/LC = 100{,}000$ (CP2 coefficient of 1). $-(1/LC)Q$ is then added, at OA1/Input 3, to

$$-\frac{R}{L}\frac{dQ}{dt} + \frac{f(t)}{L}$$

and the sum of all OA1 input voltages yields the required d^2Q/dt^2. Because there are two closed-loops in the computer set-up the equation will be self-enforcing.

Routine. Switch on UNIT "A" power supply and allow a warm-up time of at least 15 minutes. Ensure that the three operational amplifiers are disconnected from their summer networks, and have no feedback components. Apply 10V d.c. voltmeter leads to OA1/SK13 and an earth socket, and zero-set OA1 for an output voltage of less than ± 1V from the back of the UNIT "A" box, by means of VR1 (Fig. 3.7). Repeat for OA2 and OA3.

Set up the problem according to the patching circuit of Fig. 5.6b, but omit the feedback capacitors and the patching link between OA3/SK13 and CP2/SK1. Set CP1 dial to approximately "1". Connect the voltmeter to miniature socket OA1/SK6 (Fig. 2.9) and zero-set OA1 again, but this time using the front panel control VR15.

Next, zero-set OA2 using VR16, and OA3 using VR17. Insert 0·1μF computing capacitors into OA1/SK11 and SK12, and OA2/SK11 and SK12, and make good the link between OA3 output and CP2. Set CP2 for a dial reading of "10". Apply the voltmeter to OA2/SK7 and zero-set the complete assembly of amplifiers by adjustment of VR15(OA1) only.

The problem layout will now be ready for dynamic checks and should not need to be re-zeroed for several hours if UNIT "A" is being operated in stable ambient temperature conditions.

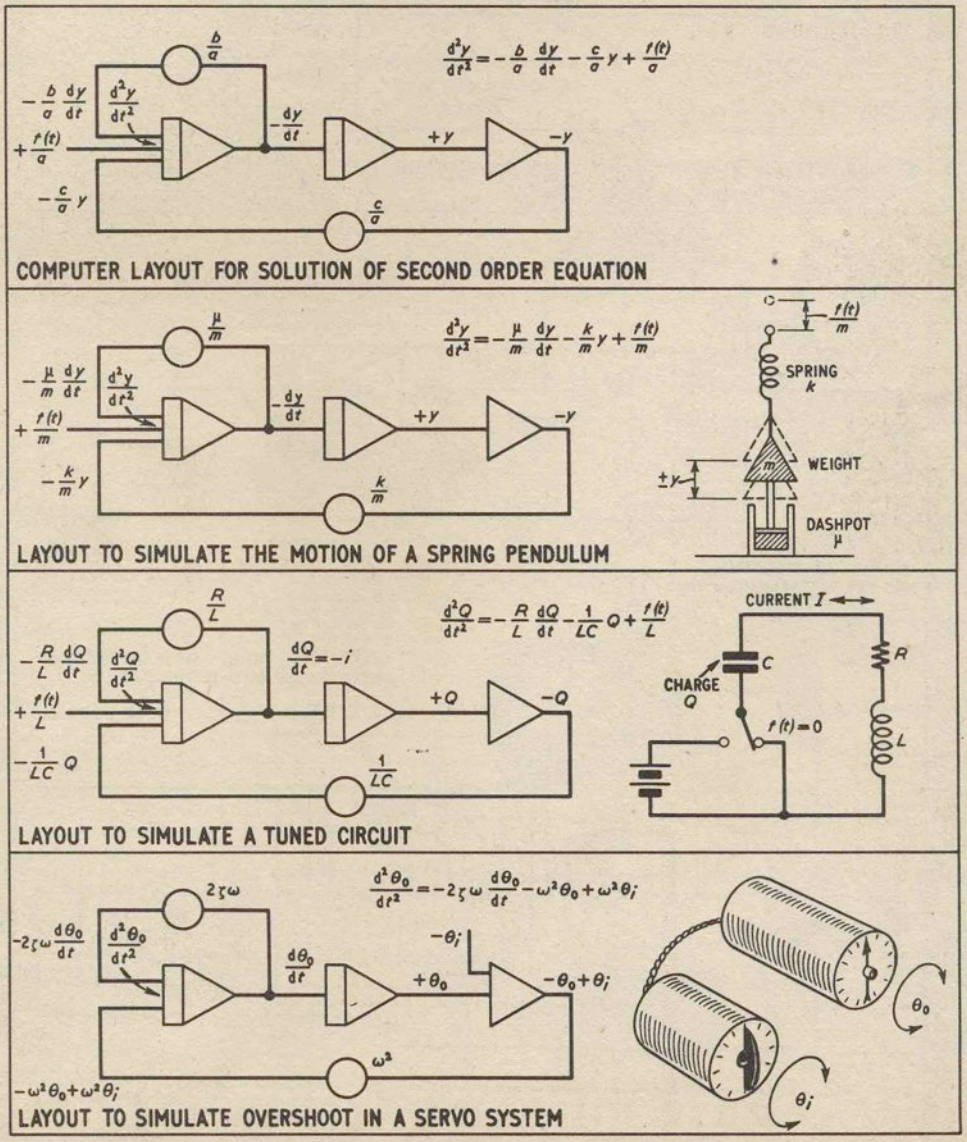


Fig. 5.5. A second order differential equation applied to physical systems

TABLE 5.2

SHOWING HOW COMPUTER OPERATING FREQUENCIES ARE RELATED TO CP2 SETTING AND AMPLIFIER CLOSED-LOOP GAINS

Resonant Frequency f	Typical Values L	C	CP2 Coefficient	$\frac{1}{LC}$	Amplifier Gains OA1 Input 3	OA2	OA3
0·05Hz to 0·5Hz	1,000H	10,000μF	0·1	0·1	10	10	0·1
	100H	1,000μF	1·0	10	10	10	0·1
5Hz to 50Hz	10H	100μF	0·01	10^3	1,000	100	1·0
	1H	10μF	1·0	10^5	1,000	100	1·0
500Hz	100mH	1μF	1·0	10^7	1,000	1,000	10
1kHz	100mH	0·2μF	1·0	5×10^7	1,000	1,000	50

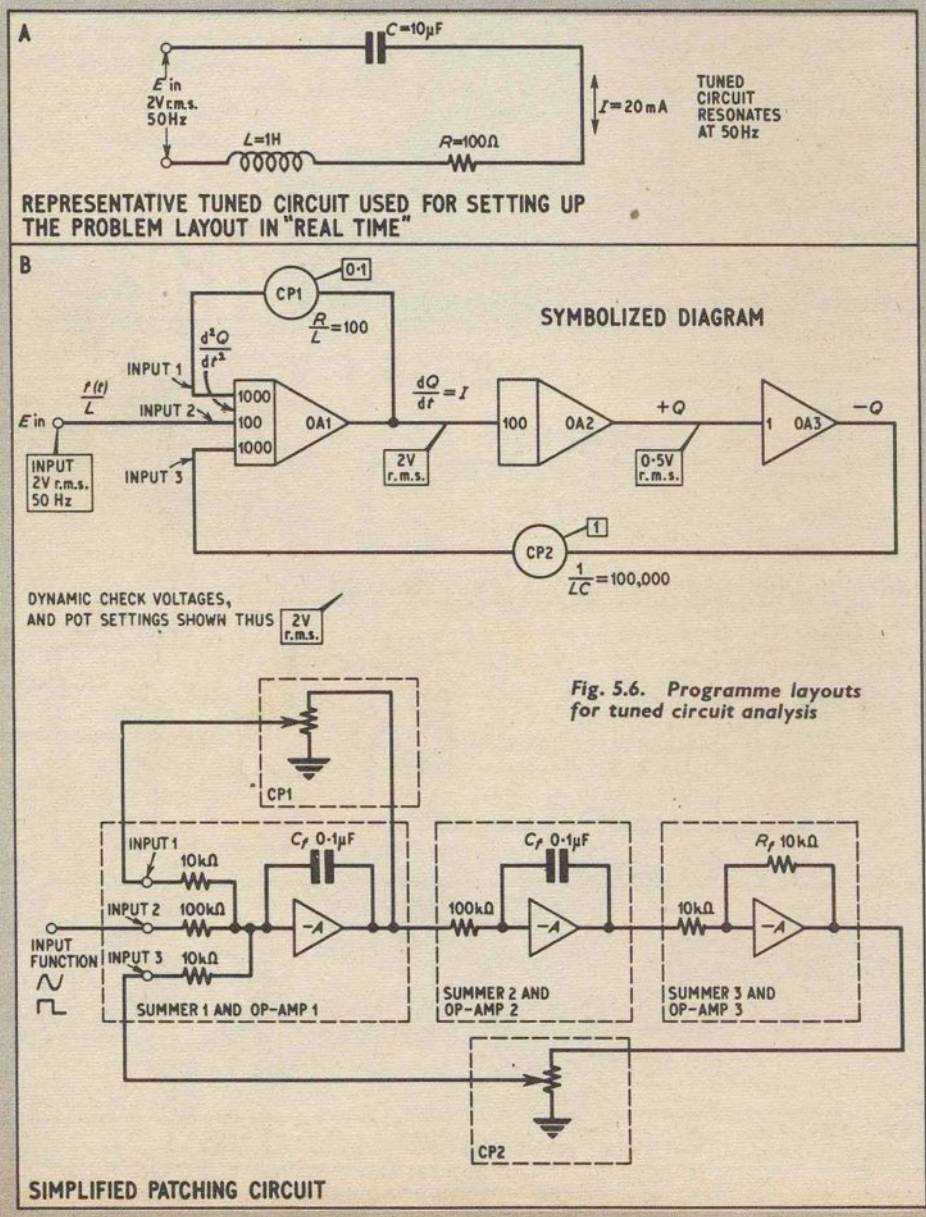


Fig. 5.6. Programme layouts for tuned circuit analysis

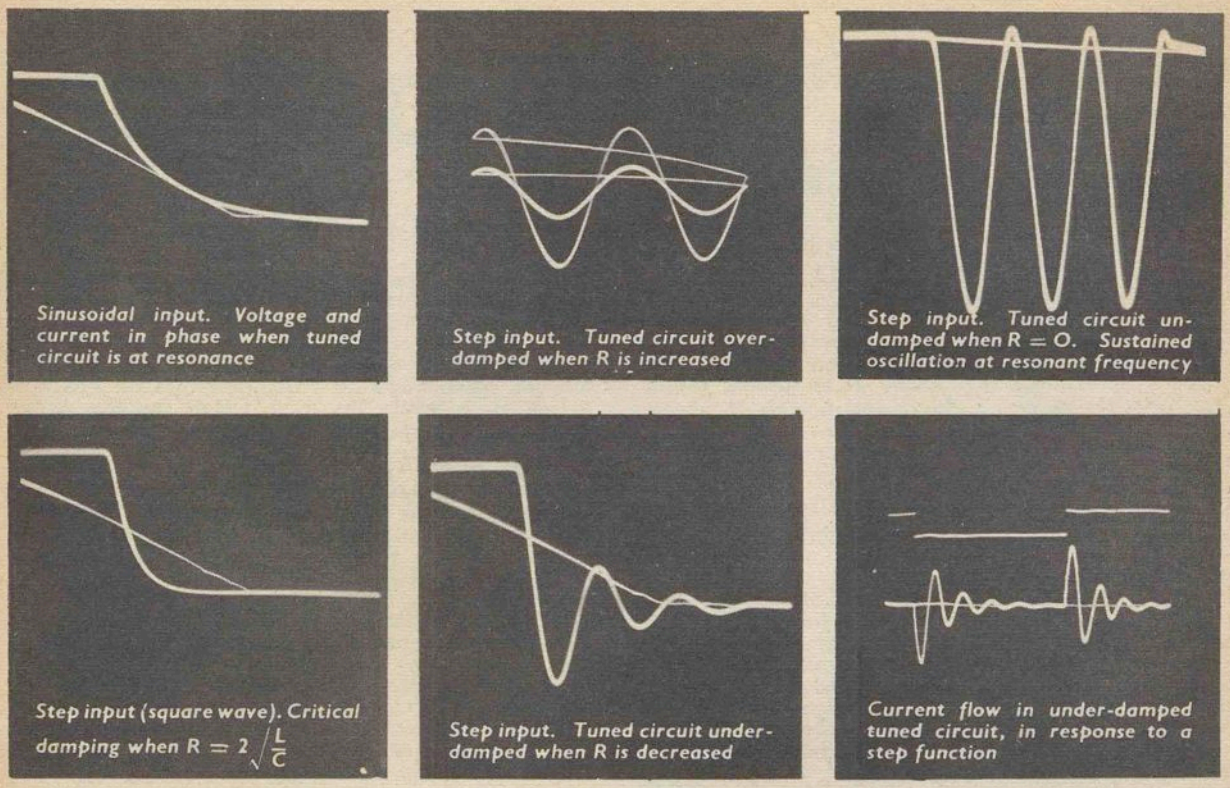


Fig. 5.7. Response of a simulated tuned circuit

Apply a 2V r.m.s. 50Hz signal to OA1/Input 2, and monitor by means of a reliable 10V a.c. meter of not less than 1 kilohm/volt sensitivity. The input function should preferably come from a low impedance source to avoid serious loading errors when the voltmeter is removed. Next, connect the a.c. voltmeter to the output of OA1 and adjust CP1 so that OA1 input and output voltages are exactly equal. CP1 could alternatively be set by the reference voltage and d.c. voltmeter method mentioned earlier, for a coefficient of 0·1. If the CP2 setting is altered it will be discovered that the simulated circuit goes off resonance, and can be tuned by CP2 between approximately 5Hz and 50Hz.

UNIT "A" will now be ready for analysis of the Fig. 5.6a tuned circuit, and will also cover a useful range of other values for L, C, and R in real time.

When handling sinusoidal or step functions, an amplifier will still have a maximum output voltage swing of $\pm$10V, but this will be the peak voltage value. To check for overloading with an a.c. meter, ensure that amplifier output voltages do not exceed 7·07V r.m.s. for a sine wave function, and 5V mean for an equal mark-space square wave.

RESCALING PROBLEM EXAMPLE 3.

To rescale the problem for larger or smaller values of L and C, beyond the coverage of CP2, and by abandoning real time operation, note that a tenfold increase in tuned circuit frequency corresponds to a hundredfold increase in $1/LC$. For most applications, where the series resistance R will lie between zero and just beyond critical damping ($R > 2\sqrt{[L/C]}$), the scaling of R/L can stay as it is for all reasonable values of L and C, but should anyway only be changed by adjustment of the gain factor at OA1/Input 1. Similarly, the $f(t)/L$ gain of 100 at OA1/Input 2 can remain fixed.

It is not necessary to use inconveniently large or small input functions when rescaling for new voltages and currents. 2V r.m.s. could equally well represent an input function of, say, 0·2V r.m.s., and from Ohm's Law the current I will automatically become 2mA, instead of the former 20mA, even though it is still represented by 2 computer volts.

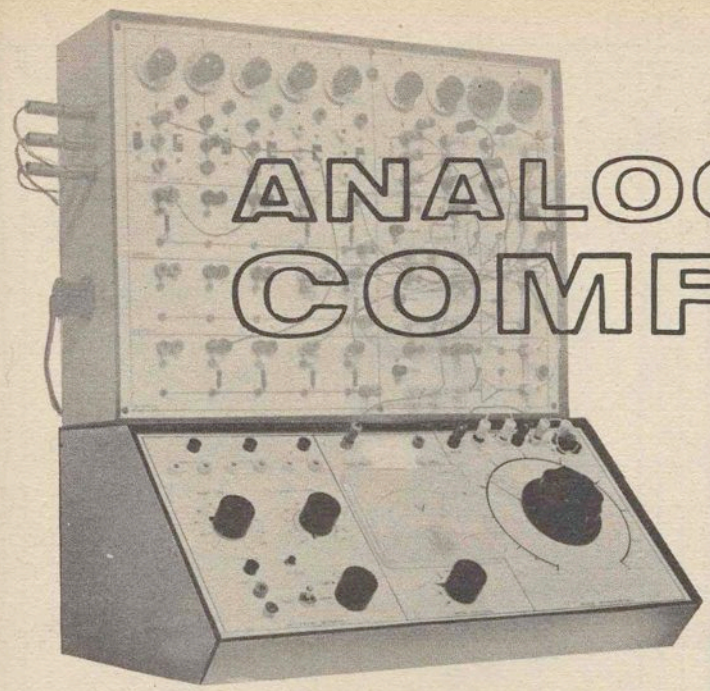
If it is desired to extend the computer operating time, by adjustment of integrator and inverting amplifier closed-loop gains, refer to Table 5.2, while remembering that integrator closed-loop gains are calculated on the basis of $1/R_{in}C_f$ where R is in ohms and C is in farads.

For reasons of reduced accuracy, it is not advisable to use computer operating frequencies above 1kHz or below 0·05Hz in connection with Problem Example 3. It should be mentioned that although frequencies in the region of 0·05Hz are too low for display on an a.c. coupled oscilloscope, the behaviour of a system can be demonstrated in slow motion by the oscillating movement of a d.c. voltmeter pointer (centre-zero).

Some typical oscillograms are given in Fig. 5.7 to show the response of a simulated tuned circuit. If the computer oscilloscope is provided with a good graticule, and has a linear response, amplitude and time measurements which are accurate to within approximately 5 per cent may be obtained straight from the trace.

The behaviour of a real tuned circuit can be evaluated by comparison with a simulated circuit. A tracing is made of the real circuit oscilloscope display, and is then superimposed on the readout given by the simulated circuit. The computer is adjusted so that time scales are related by a known factor, and tracing and readout display are identical, then quantitative measurements are taken from the computer voltages and dial settings.

Next month: The construction and operation of UNIT "B"



ANALOGUE COMPUTER

PEAC

By D. BOLLEN

THE PEAC basic equipment has now been dealt with and this month we commence a detailed description of the chief ancillary unit. Subsequent articles will cover the remaining two ancillary units.

Perhaps it should be repeated at this stage that the three ancillary units are purely optional add-on items. The additional facilities they each provide, are indicated in the PEAC Specification (January 1968, page 38).

PEAC UNIT "B"

UNIT "B" reinforces the facilities of UNIT "A", but does not introduce new computing circuit elements. A master potentiometer and a suitably scaled readout meter improve the accuracy and ease of handling of UNIT "A", while the integrator mode switching circuit opens up further possibilities in the solution of Calculus problems.

UNIT "B" FRONT PANEL

It may not be necessary to use hardboard for the front panel if a thick grade of plastic laminate is used, since the wooden surround in the box front gives plenty of support.

Prepare a $17\frac{3}{4}$in $\times$ $8\frac{3}{4}$in white laminate panel and establish hole centres with a sharp spike, from the drawings Fig. 6.1 and Fig. 6.2. Next, drill only the holes for all sockets, S7, S8, the meter mounting studs, and cut out a hole for the meter body with a fretsaw.

Beginning with the master potentiometer dial, draw a 300 degree arc of radius $2\frac{11}{16}$in with a pencil compass (refer to Fig. 6.2). Divide the arc into 3-degree divisions with protractor and pencil. The accuracy of the master potentiometer will benefit from careful preparation of the dial. Draw in the dial arc and divisions with Indian ink.

Rub-on transfers are suitable for the dials of VR18 and VR19, and will save time, but make sure that the transfer gives main divisions spaced at 30-degree intervals, for a 1–10 calibration.

When dials are complete, drill holes to take the spindles of VR18–VR20, S9 and S10. Draw in all ink lines, add transfer numerals, and varnish.

BOX CONSTRUCTION

Commence building the UNIT "B" box by cutting out two side panels from hardboard; they are shown in Fig 6.3. Fix $\frac{1}{2}$in square softwood lengths *A*, *B*, *C*, and *D* to the inside of the side panels. Join the side panels together by means of horizontal lengths *E*, and *F*, using countersunk woodscrews and glue. Square up with the assembly placed on a flat surface.

Cover the box framework with hardboard top, bottom, and front strip panels, and, when firm, reduce overlapping edges with a rasp and sandpaper. Finish off the box with a layer of white plastic laminate, and paint exposed hardboard edges to match the UNIT "B" box.

MASTER POTENTIOMETER AND NULL METER

A d.c. voltmeter connected to the slider of a computing potentiometer will impose a small load, and when the voltmeter is removed the measured coefficient will increase slightly, to the extent of about $1\frac{1}{2}$ per cent in the case of a 10V 20,000 ohms/volt meter, and a 10 kilohm potentiometer set with its slider near mid-track. One way of avoiding the error is to leave the voltmeter connected to the potentiometer after a coefficient reading has been taken, but this is seldom convenient.

Ideally, the instrument used to measure coefficients or computer voltages should impose no load at all, and this condition can be satisfied fairly easily by employing an accurately calibrated master potentiometer.

In Fig 6.4, a permanent load is placed on the coefficient potentiometer CP by the computing resistor R_{in}, thus causing a significant dial setting error. To find the true coefficient of CP, both potentiometers are supplied with a reference voltage of + 10V, so that potentiometer coefficients of 0–1 will be multiplied by 10 to conform to a 0–10 dial calibration. When

COMPONENTS . . .

UNIT "B" FRONT PANEL

NOTE: All front panel controls are numbered consecutively, following on from UNIT "A", but internal sub-assemblies have individual component numbering.

Potentiometers
VR18 100kΩ carbon linear
VR19 100kΩ carbon linear
VR20 25kΩ wirewound, 3in, 25W instrument potentiometer. (G. W. Smith & Co. (Radio) Ltd., 3 Lisle Street, London, W.C.2)

Switches
S7 Miniature push button, push to make, one pole
S8 Toggle, single pole changeover
S9 4 pole, 3 way rotary
S10 2 pole, 6 way rotary

Sockets
5 red, 3 black, 5 blue, 4 yellow, 4 white, and 2 green

Knobs
One Bulgin K403, 2⅜in knob with 3in skirt. Three Radiospares type PK 1⅛in knobs with pointers

Meter
M1 "Sew" MR85P, 100–0–100μA, internal resistance 1,000Ω

Miscellaneous
Plastic laminate (thick) for front panel, 1 off, 17¾in × 8¾in. Rub-on dial transfers and letters, black (Radiospares)

UNIT "B" MASTER POTENTIOMETER

Resistors
R1 200Ω R3 47Ω R5 820Ω
R2 820Ω R4 47Ω R6 200Ω
All 5%, ½W carbon film or metal oxide

Pre-set potentiometers
VR1—VR4 100Ω wirewound (4 off) panel mounting type

Miscellaneous
16 s.w.g. aluminium sheet 6in × 4in. Tag strip with three tags.

UNIT "B" READOUT METER

Resistors
R1 82kΩ 10% R3 7·5kΩ 5% All ½W, carbon composition
R2 22kΩ 10% R4 1·2kΩ 10%

Pre-set potentiometers
VR1 22kΩ
VR2 10kΩ
VR3 2·2kΩ
VR4 1kΩ
All miniature horizontal mounting skeleton construction

Meter protection diodes
D1, D2 OC71 or similar "inverted" germanium transistor (2 off)

Miscellaneous
S.R.B.P. panel 2⅛in × 2in.

UNIT "B" INTEGRATOR MODE SWITCH

Resistors
R1 10kΩ R4 4·7kΩ R7 27kΩ
R2 10kΩ R5 27kΩ R8 4·7kΩ
R3 1kΩ R6 1kΩ R9 10kΩ
R10 10kΩ R12 3·3kΩ R14 1kΩ
R11 1kΩ R13 10kΩ R15 560kΩ
All 10%, ½W carbon composition

Pre-set Potentiometers
VR1 10kΩ
VR2 5kΩ Both vertical mounting

Capacitors
C1 1,000μF elec. 15V
C2 1μF polyester 250V d.c. C6 1μF polyester 250V d.c.
C3 1·4μF polyester 250V d.c. C7 1·4μF polyester 250V d.c.
C4 14μF elec. 25V C8 14μF elec. 25V working.
C5 0·1μF polyester 250V d.c. C9 0·068μF polyester 250V d.c.
(The values of C3, C4, C7, and C8 are approximate—see text)

Transistors
TR1–TR6 ACY28 *or* AC126.

Diodes
D1, D2 OA95 (2 off)
D3–D14 1B30 (Radiospares) (12 off)

Reed Coils
RLA, RLB Miniature triple 12V Osmor type MT12V (2 off)

Reed Switches
RLA1—RLA3 } Hamlin MRG2, 20-40AT (R.T.S. Ltd.,
RLB1—RLB3 } P.O. Box 11, Gloucester St. Cambridge) (6 off.)

Miscellaneous
S.R.B.P. panels: 1 off 6½in × 2½in; 1 off 3in × 2in.
Small turret tags.

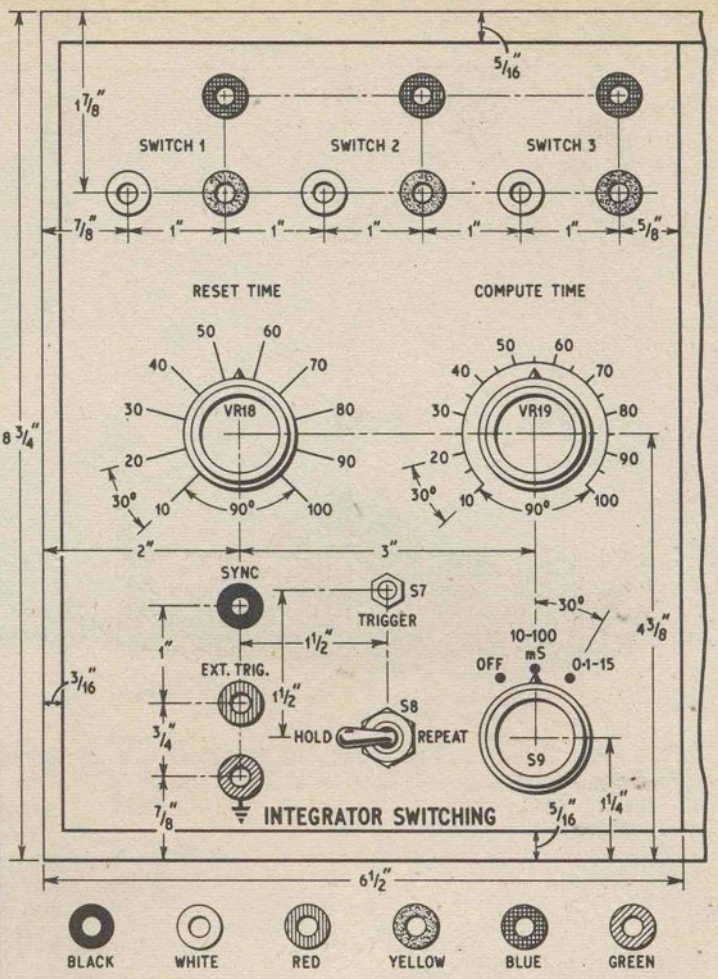


Fig. 6.1. UNIT "B" front panel, integrator switching section

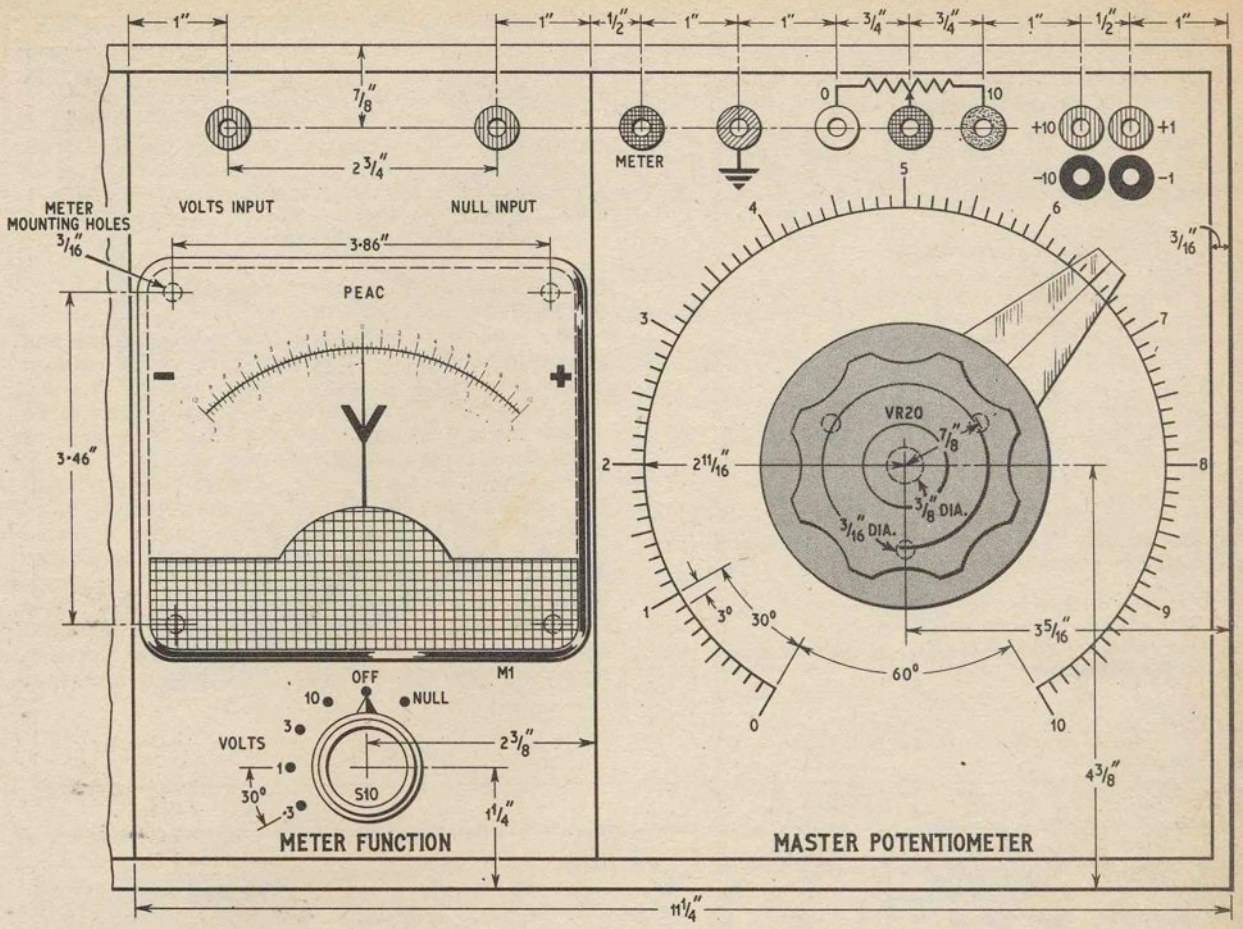
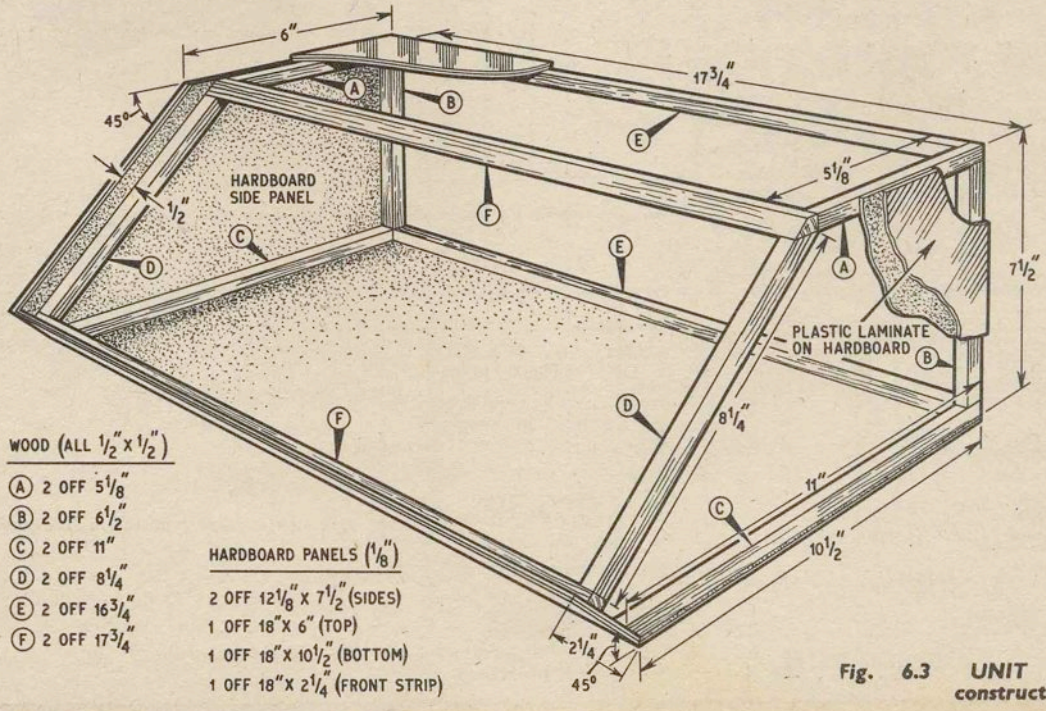


Fig. 6.2. UNIT "B" front panel, readout meter and master potentiometer



WOOD (ALL $1/2$" x $1/2$")

- (A) 2 OFF $5\,1/8$"
- (B) 2 OFF $6\,1/2$"
- (C) 2 OFF 11"
- (D) 2 OFF $8\,1/4$"
- (E) 2 OFF $16\,3/4$"
- (F) 2 OFF $17\,3/4$"

HARDBOARD PANELS ($1/8$")

- 2 OFF $12\,1/8$" x $7\,1/2$" (SIDES)
- 1 OFF 18" x $10\,1/2$" (BOTTOM)
- 1 OFF 18" x $2\,1/4$" (FRONT STRIP)

Fig. 6.3 UNIT "B" box constructional details

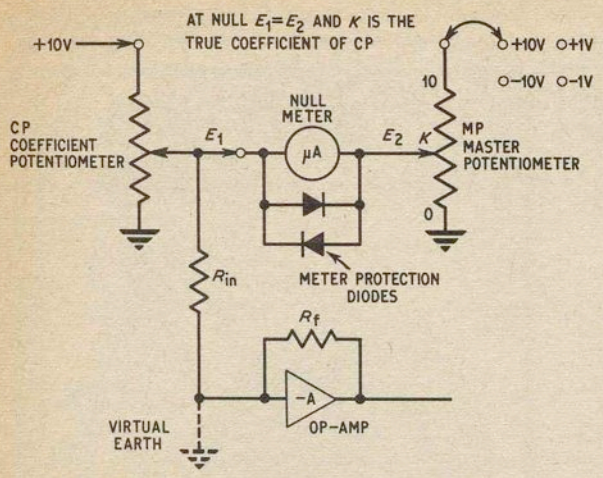


Fig. 6.4. Master potentiometer circuit for measuring coefficients

Fig. 6.5 (below). Circuit diagram of readout meter and master potentiometer

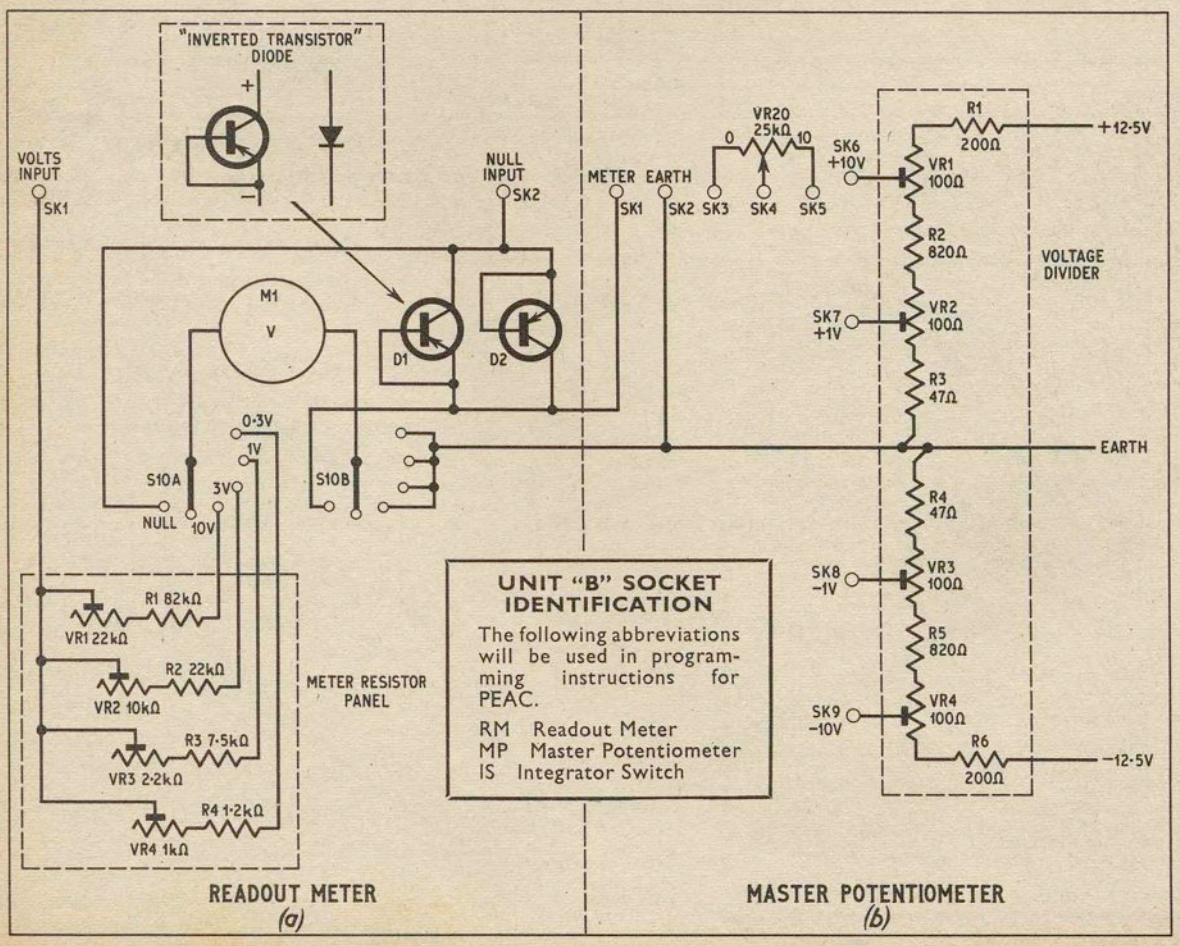
the voltage at the slider of CP is identical to the slider voltage of MP, no current flows through the null meter, and the true coefficient of CP can be read straight off the dial of MP.

Since no current flows at null point, no load is imposed, and the input resistance of the measuring circuit is virtually infinite. Meter protection diodes are included to preserve good meter sensitivity without allowing damaging currents to flow through the meter when the circuit is off balance.

READOUT METER AND MASTER POTENTIOMETER CIRCUITS

One meter movement serves for null indication and voltage measurement. Considering first the readout meter circuit Fig 6.5a, miniature pre-set resistors VR1–VR4 will permit calibration of each meter range to an external voltage standard, and also help to eliminate discrepancies between ranges.

The way in which meter protection diodes D1 and D2 are wired may be unfamiliar to the reader, so some explanation is called for. If a transistor is operated "inverted", that is with collector-emitter polarities reversed, it will exhibit a very low "on" resistance when the base is near emitter potential. With base connected straight to emitter, the transistor therefore becomes a diode with lower than normal forward resistance, and yet will still offer a high resistance



reverse characteristic. The arrangement eliminates the need for a meter series resistor while still giving adequate protection.

In Fig. 6.5b, VR20 is a 3in instrument potentiometer of good linearity. The voltage divider network, composed of R1–R6 and VR1–VR4, taps off four standard voltages from the computer power supply, so that the master potentiometer will measure inputs of 0 to + 1V, 0 to − 1V, 0 to + 10V, and 0 to − 10V on its 0–10 scale. The accuracy of the master potentiometer, bearing in mind the 14in scale length, approaches that of a laboratory voltmeter.

FRONT PANEL AND MASTER POTENTIOMETER ASSEMBLY

Mount all sockets, potentiometers VR18–VR20, switches S7–S10, and meter, on the UNIT "B" front panel. Make up an aluminium bracket from the measurements given in Fig. 6.6, and glue it to the front panel, along with the small tag strip, in the position shown in Fig. 6.7. A hot soldering iron applied to the aluminium bracket will solidify the epoxy resin glue in a matter of minutes, sufficient to hold the bracket in place until the joint sets hard.

Rest the front panel inside-out on the UNIT "B" box front, to protect panel markings during assembly. Mount pre-set voltage divider potentiometers VR1–VR4 to the aluminium bracket, and then proceed with the

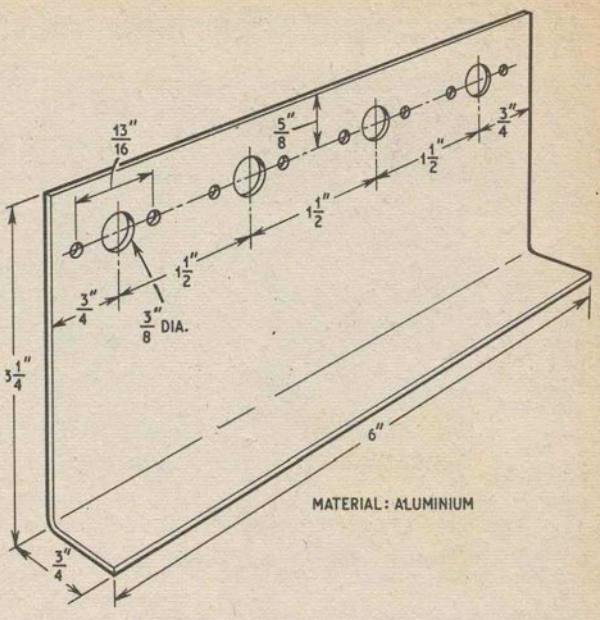


Fig. 6·6. Mounting bracket for pre-set potentiometers

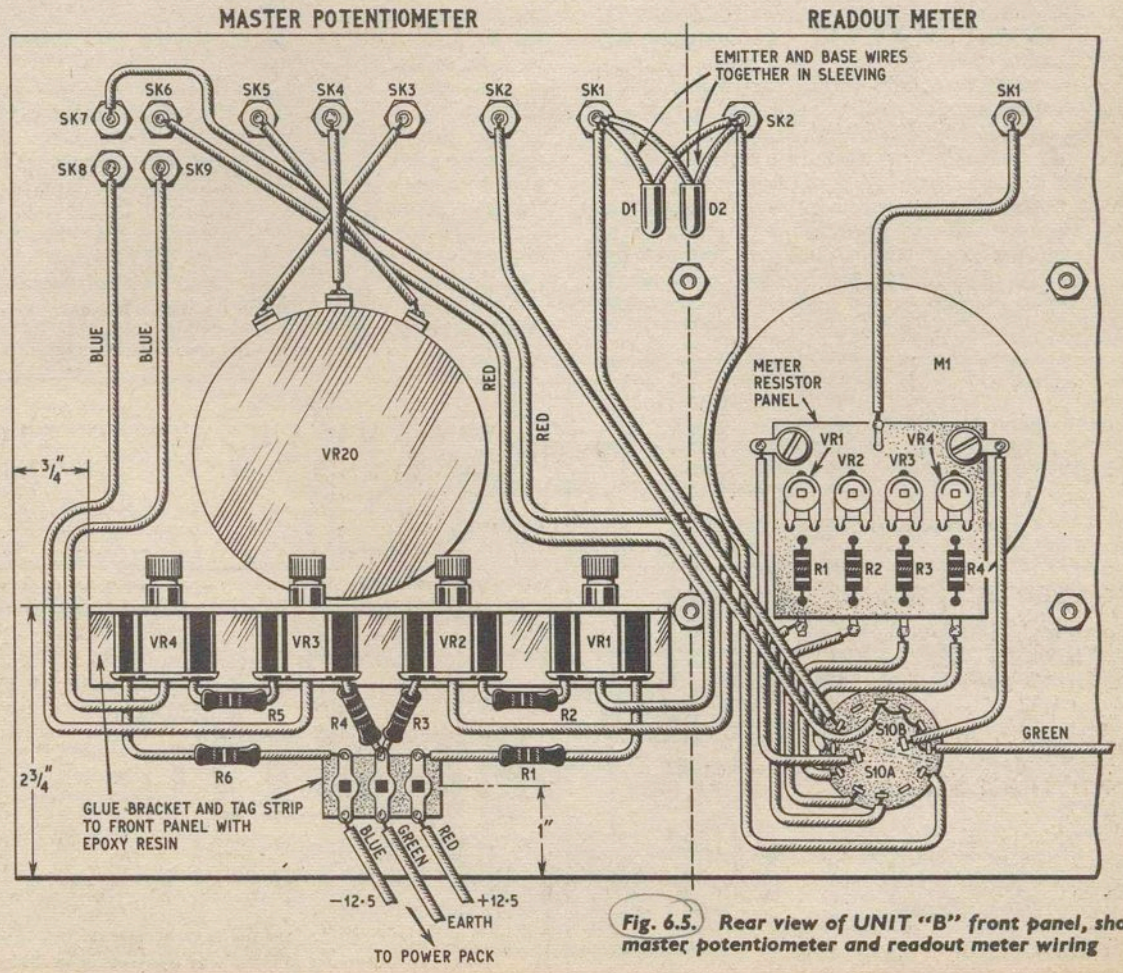


Fig. 6.5. Rear view of UNIT "B" front panel, showing master potentiometer and readout meter wiring

Fig 6.7

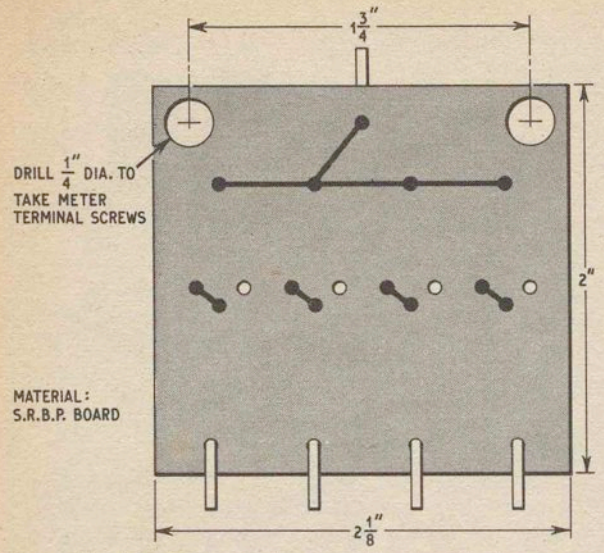


Fig. 6.8. Meter resistor panel, underside view

wiring of master potentiometer components, using 20 s.w.g. tinned copper wire and sleeving.

READOUT METER ASSEMBLY

Make up the meter resistor panel shown in Figs 6.7 and 6.8, and attach to the meter terminals. Solder D1 and D2 to MP/SK1 and RM/SK2, then complete S10 and resistor panel wiring.

As centre-zero voltmeters with 10–0–10 and 3–0–3 scale calibrations are not readily available, a scale will have to be made. Perhaps the most satisfactory way of fabricating a new and really accurate meter scale is to draw it two to four times full size, photograph it, and then have the resulting negative enlarged back to the original size on glossy photographic paper. The enlarging can be done commercially if the oversize drawing carries a thick black line to represent a length of 1in on the finished scale, just outside the scale perimeter.

When taking the photograph, ensure that the camera lens is in line with the centre of the scale card, and that the film plane is parallel to the surface of the oversize drawing, to prevent optical distortion.

Another tip, use white Formica for the drawing, as then mistakes in ink can be erased without leaving unsightly grey areas.

To remove the existing scale from the meter, prise off the transparent meter front, and carefully remove the scale card by undoing the two holding screws. Measurements can then be taken for preparing the oversize drawing.

To fit the new scale, cut out the photographic reproduction and paste it over the old scale, with edges and mounting holes of both scales properly registered.

SETTING UP MASTER POTENTIOMETER AND READOUT METER

With red, green, and blue p.v.c. covered wires, connect the master potentiometer tag strip (Fig 6.7) to the solder tags on the power pack output terminals. Also, temporarily link the rear of MP/SK2 to the green earth wire. Rotate VR20 spindle fully clockwise and patch MP/SK2 to SK3, MP/SK5 to SK6, MP/SK1 to SK4, and link RM/SK2 to VS1/SK1. Switch on the computer and S6, and adjust VS1 for an exact +10V. Now obtain a null on the readout meter by setting VR1 on the voltage divider bracket, from the back of UNIT "B" box.

Repeat for VR2 with an input of +1V by transferring the patching lead plug from MP/SK6 to SK7, and again for VR3, SK8, with an input of −IV, and VR4, SK9, with an input of −10V.

After that, while still nulling with a −10V input, rotate VR20 spindle slightly clockwise, until the meter pointer just begins to move away from zero. Place the large knob on VR20 spindle, with the transparent plastic cursor aligned with the "10" division, and tighten the grub screw. Set VR20 cursor to the "5" division and check for null with an input of —5V. It may be necessary to slightly re-position VR20 knob on the spindle, and trim VR1–VR4 again to minimise errors.

Calibration of the readout meter is straightforward. Apply a selection of known voltages to RM/SK1 and

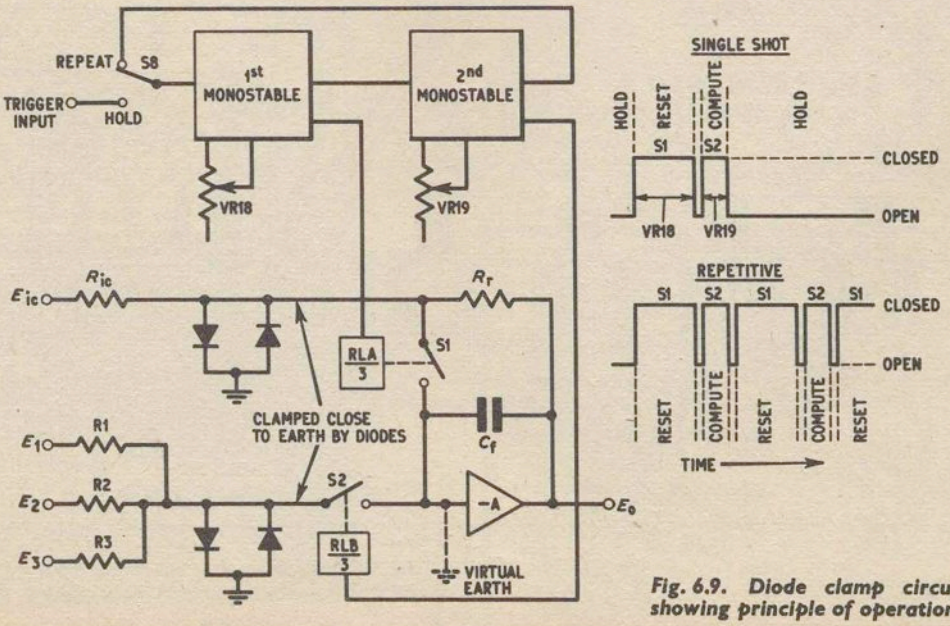


Fig. 6.9. Diode clamp circuit, showing principle of operation

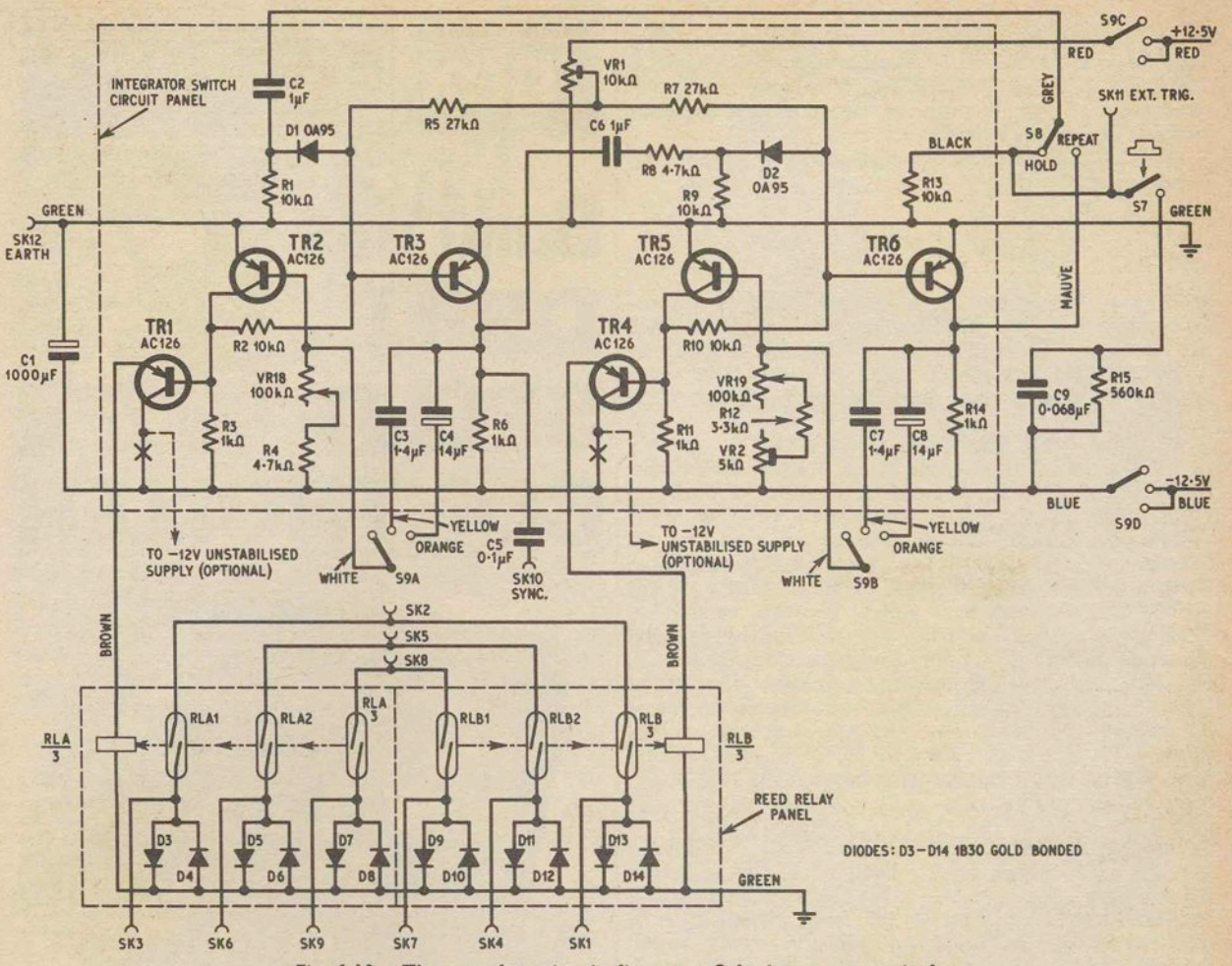


Fig. 6.10. The complete circuit diagram of the integrator switch

adjust VR1–VR4 on the resistor panel for optimum accuracy on each range.

INTEGRATOR MODE SWITCHING

The simplest type of integrator switch employs a mechanical relay with several sets of contacts, driven by an astable multivibrator, and this system is used for small demonstration and educational analogue computers. The relay is arranged to "gate" the inputs of several amplifiers simultaneously.

The PEAC integrator switch goes a stage further, with reed relays for a "clean" switching action at high speeds, full initial condition facilities, and a circuit based on two independently timed monostable multivibrators.

Referring back to the basic integrator switch shown in Fig 1.2c, two changeover switches S1 and S2 are opened and closed in a pre-determined sequence, governed by an external timing circuit. It is important to ensure that integrating amplifier input resistors are not left floating when they are disconnected from the virtual earth summing junction, as this could seriously disturb input and other computer voltages, hence the presence of S1 and S2 earthed contacts.

DIODE CLAMPS

To eliminate the need for expensive reed switches with changeover contacts, diode clamps can be used instead of an earthed contact, see the alternative amplifier circuit of Fig 6.9. The diodes do not interfere with the normal working of the integrator, but will nevertheless hold resistor junctions close enough to earth to prevent load variations when S1 and S2 are open, and this modification more than halves the cost of switching components.

In the block diagram of Fig 6.9, the 1st monostable—controlled by VR18—determines the period of closure of S1. When S1 opens after a timed interval, a pulse is delivered to the input of the 2nd monostable, thus closing S2. S2 will remain closed for an interval controlled solely by VR19.

For "single shot" operation, a trigger pulse applied to the 1st monostable input, when S8 is switched to "hold", will initiate the closure of S1 (reset) and bring the integrating amplifier to its initial condition.

As soon as S1 opens, S2 closes (compute) and connects input resistors to the summing junction. At the end of the compute period, S1 and S2 are both open (hold), the monostables are quiescent, and the amplifier output voltage is held steady by the action of capacitor C_f. The next computer run is started by another trigger pulse applied to the 1st monostable input.

Repetitive operation is achieved by passing the output pulse from the 2nd monostable back to the input of the 1st monostable, when S8 is switched to "repeat". S1 and S2 are then made to open and close alternately, and the "hold" facility is deleted.

The method of inserting an inital condition voltage is as follows. When S1 is closed the reset resistor R_r is connected between the amplifier output and summing junction, and can therefore be regarded as a feedback resistor in parallel with C_f.

As long as S1 remains closed, R_{ic} will be acting as an input resistor, so that

$$E_o = - E_{ic} \frac{R_r}{R_{ic}}$$

and $E_o = - E_{ic}$ when $R_r = R_{ic}$. R_{ic} and R_r are disconnected from the amplifier summing junction when S1 opens, but C_f will "remember" the initial condition voltage and hold the amplifier output steady prior to the application of compute voltages when S2 closes.

INTEGRATOR SWITCH CIRCUIT

The complete circuit of the integrator switch is shown in Fig 6.10. The 1st monostable consists of TR2 and TR3, with RLA actuated by emitter follower TR1. VR18 continuously covers two ranges given by C3 (10–100ms), and C4 (0·1–1s). Components associated with the 1st monostable input are C2, R1, and D1.

The 2nd monostable is almost identical to the 1st. TR4 drives RLB, C7 and C8 offer the same timing range coverage as C3 and C4, and input components are C6, R8, R9, and D2. However, more care is taken to establish the correct values for 2nd monostable timing capacitors C7 and C8, and VR2 allows precise calibration of the "fast end" of the VR19 timing scale, so that compute intervals can be determined by a reasonably accurate dial setting.

VR1 establishes the working point of both monostables, to achieve reliable operation at all dial settings. S7 is a push button on the front panel for starting a "single shot" computer run. Full control of an oscilloscope trace, from UNIT "B" front panel, can be realised by suitable connection to the integrator switch circuit. With S8 switched to "hold", the mode sequence can be triggered repetitively, with a variable hold interval, by the oscilloscope timebase output or by a separate oscillator. Consistant syncronisation of the trace, with continuous or single-sweep timebases, is made possible by linking IS/SK10 to an appropriate oscilloscope input

A SEPARATE SUPPLY

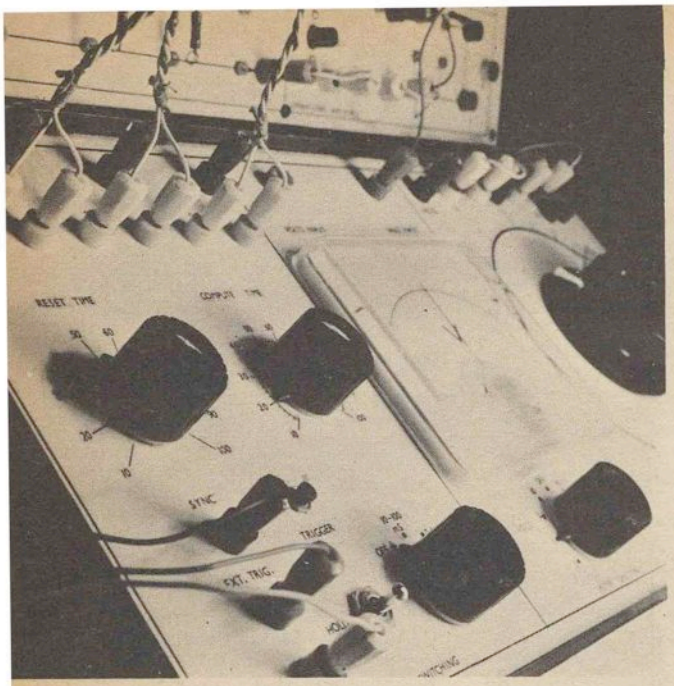
The load capacity of the existing stabilised power supply can be improved by wiring the collectors of TR1 and TR4 (shown dotted in Fig. 6.10) to a separate −12V unregulated supply, which can be housed inside the UNIT "B" box, and in this event C1 could be omitted from the Fig. 6.10 circuit, as it merely serves to prevent current pulses from flowing in the negative stabilised supply line during relay switching.

RLA and RLB consist of two triple-switch coils, catering for the needs of three integrating amplifiers. A duplicate relay panel could be added later, by wiring relay coils in parallel, to increase the switching capacity to six amplifiers.

CORRECTION

In Fig. 5.7, the captions for the first and second oscillographs (top row, left and centre) should be transposed.

Next month: Assembly and setting up of the Integrator Switch; practical examples in the use of this section. Introduction of UNIT "C" Function Generator.



on its blocks, and, following Fig. 6.10 and Fig. 7.3, wire all controls and sockets to the turret tags on the two sub-assembly panels, again with p.v.c. covered flexible wire, long enough to allow the switching circuit panel to be turned over for underside inspection. Run red and blue wires from S9, and a green wire from IS/SK12, to the power pack output solder tags, and fit knobs to S9, VR18, and VR19.

SETTING UP THE INTEGRATOR SWITCH

Time intervals can be measured with fair accuracy when an operational amplifier is employed to integrate known voltages, and this method is useful for setting up the integrator switch.

Begin by temporarily soldering 8μF electrolytic capacitors in the C4 and C8 positions, with 1μF polyester capacitors for C3 and C7 (circuit Fig. 6.10).

Set VR1 and VR2 with sliders at mid-track, on the integrator switch panel.

Connect integrating switch to the operational amplifier by linking IS/SK7 to OA3/SK9, IS/SK8 to OA3/SK10, and IS/SK9 to OA3/SK4. Fit 100 kilohm computing resistor in S3/I1/SK3 and SK4. Join S3/I1/SK1 to VS1/SK2 and switch off S6. Insert a 2 kilohm reset resistor in OA3/SK5 and SK6, and join S3/SK5 to OA3/SK13.

ANALOGUE COMPUTER

PEAC

By D.BOLLEN

TO COMPLETE the construction of UNIT "B", we have now to deal with the integrator switching section, the circuit diagram for which has already been given, see Fig. 6.10.

INTEGRATOR MODE SWITCH ASSEMBLY

Cut and drill the 6¼in × 2½in s.r.b.p. panel shown in Fig 7.1, and rivet turret tags in the positions shown. From six transistors select two with the highest current gain for TR2 and TR5. Mount all components, except range capacitors C3, C4, C7, and C8, on the s.r.b.p. panel and wire up.

Prepare the 3in × 2in relay panel, from Fig. 7.2. Fix turret tags and mount RLA and RLB reed coils. Next, insert miniature diodes D3–D14, with alternating polarities along the row of diodes, and complete underside wiring. To finish off the relay panel, place three reed switches in each coil and secure by soldering the lead out wires to appropriate turret tags.

Wooden blocks are glued to the rear of the UNIT "B" front panel to serve as mounts for switching circuit panel and relay panel (see Fig. 7.3). Note that the relay panel is fitted end-on into slots cut in its mounting blocks, and the switching circuit panel is secured by two woodscrews.

After first attaching lengths of black and white p.v.c. covered multi-strand wire to the terminals of VR18 and VR19, screw the switching circuit panel in position

Switch on the computer and allow a warm up period before zero setting OA3 from the back of the UNIT "A" box, by means of VR1 on the OA3 amplifier panel. Insert a 1μF computing capacitor into OA3/SK11 and SK12.

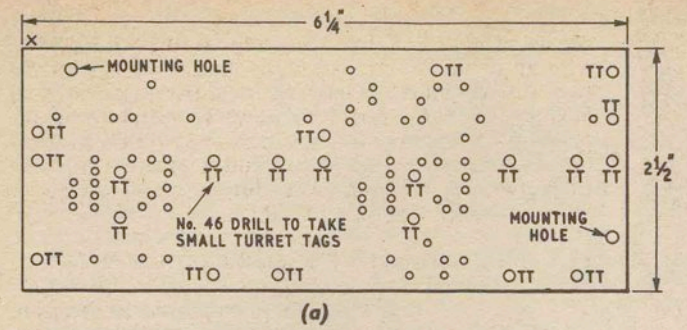
With S8 switched to "hold", S9 on the 0·1–1s range, and VR18 and VR19 rotated fully clockwise, press S7 to run the integrating amplifier through reset, compute, and hold sequence.

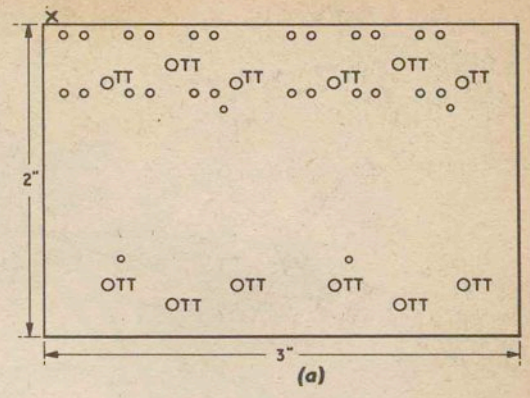
Listen for two clicks from the reed relays, and observe that the readout meter pointer will move close to zero. If the relays click more than twice, or not at all, adjust VR1 on the integrator switch panel.

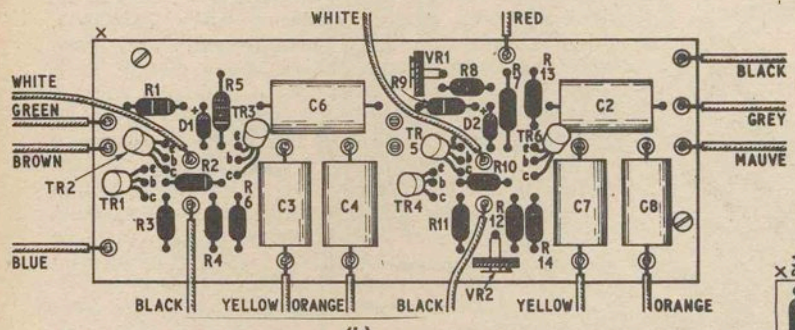
To obtain a true zero output from the amplifier, when integrating a zero input voltage, adjust VR17 (OA3 balance control) while repeatedly pressing S7. If there is a slow drift away from zero output several seconds after S7 was last pressed, retrim VR1 on the OA3 amplifier panel.

As the gain of OA3 is set at 10 (1μF for C_f and 100 kilohm for R_{in}), an input of −0·9V "gated" by the integrator switch for an interval of 1s should give rise to an amplifier output of exactly +9V. Switch on S6 and adjust VS1 for −0·9V, monitored at S3/I1/SK2 by a voltmeter.

Now when S7 is pressed, and with VR19 still rotated fully clockwise, the readout meter reading should rise to somewhere below +9V and stay there.







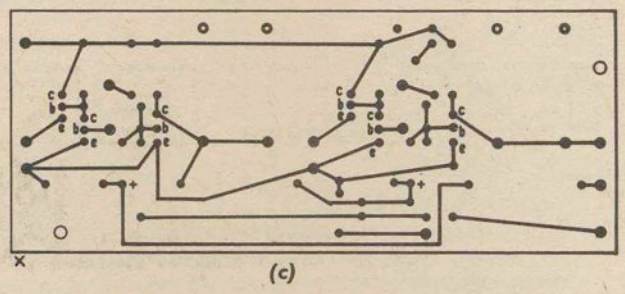
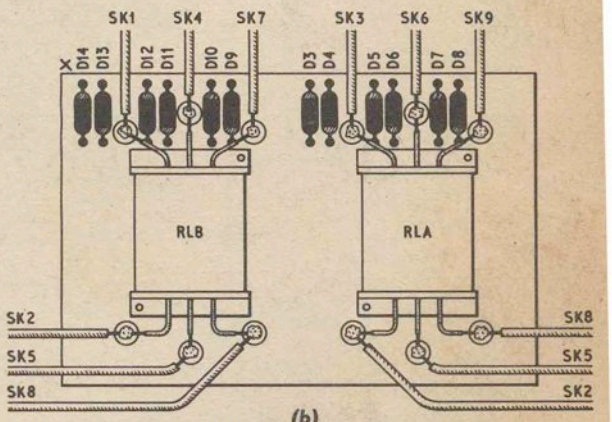


Fig. 7.1. UNIT "B" integrator switch circuit panel, (a) drilling template; (b) component arrangement; (c) underside wiring



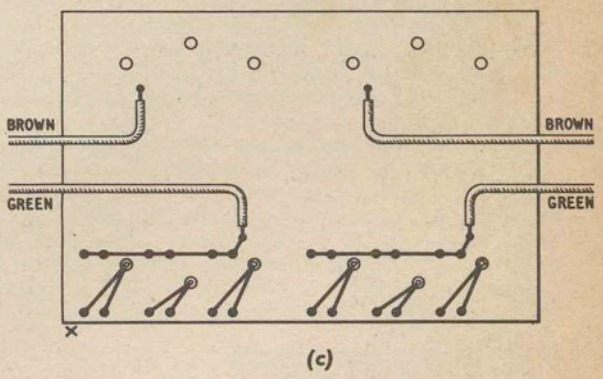
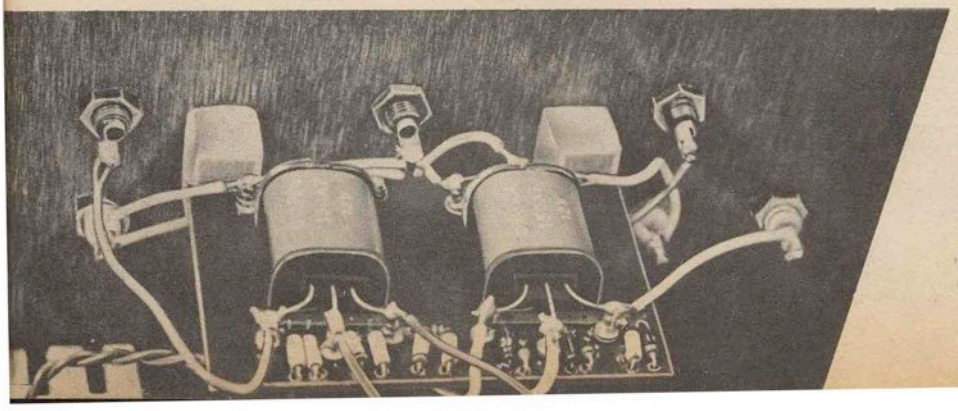


Fig. 7.2. UNIT "B" integrator switch relay panel. (a) drilling template; (b) component arrangement; (c) underside wiring

Build up the value of C8 timing capacitor by adding more capacitors in parallel, until the +9V output is obtained when S7 is pressed.

To check the "fast" end of VR19 scale, set VS1 for −9V and rotate VR19 fully anti-clockwise. Adjust VR2 on the integrator switch panel to obtain the desired amplifier output of +9V for a compute interval of 0·1s.



(c)

Section of UNIT "B" panel (viewed from rear) showing integrator switch relay assembly

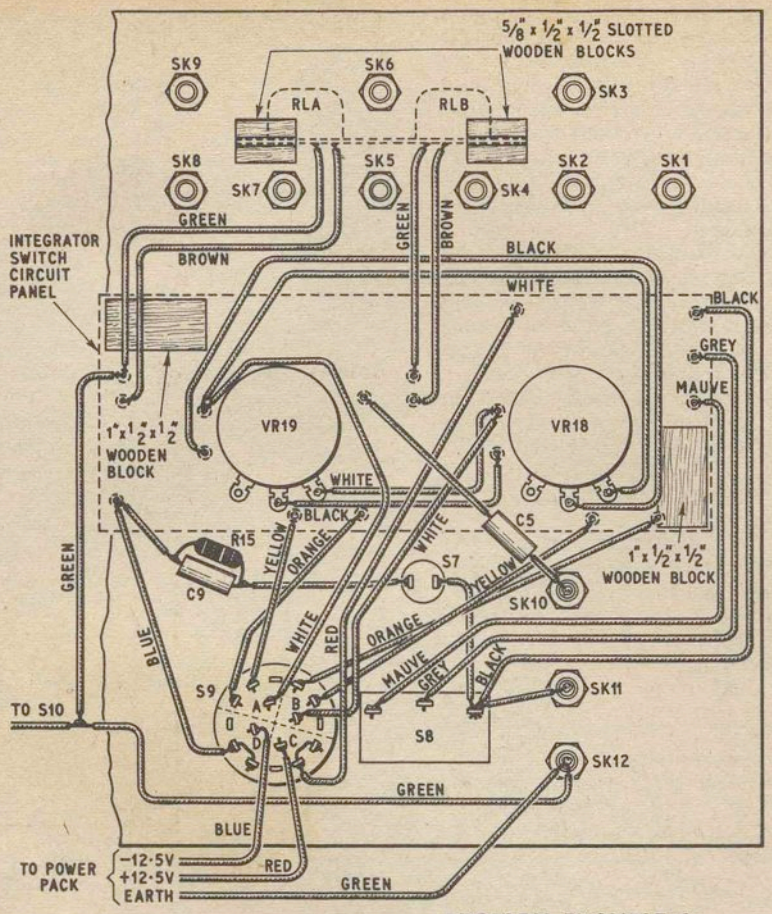


Fig. 7.3. Rear view of UNIT "B" front panel showing integrator switch wiring

CALIBRATING THE SECOND RANGE

To calibrate the 10–100ms S9 range, repeat the above procedures in just the same way, but this time use a 0·1μF capacitor for C_t in sockets OA3/SK11 and SK12, and adjust the value of timing capacitor C7 for correct compute intervals.

1st monostable timing capacitors C3 and C4 need not be precise, as VR18 has no effect on the accuracy of computations, and is mainly used to control the switch cycle frequency when integrator output waveforms are displayed by oscilloscope. Therefore, and merely for the sake of conformity, build up C3 and C4 capacitor values until the coverage of VR18 is approximately as indicated by the reset interval dial calibration.

CIRCUIT ADJUSTMENTS

The Fig 6.10 circuit should operate reliably at all switch and dial settings, with no noticeable relay bounce or overlap between the closure of reset and compute switches. However, it may be found that the integrator switch will stop running during repetitive operation, when reset and compute intervals approach 10ms, despite the fact that VR1 has already been trimmed for optimum performance. If so, try reducing the value of R8.

At the opposite extreme, if the integrator switch suddenly goes into repetitive operation when S8 is at "Hold", and VR18 and VR19 settings are near 1s, increase R8, and also try the effect of doubling the value of C1 to improve decoupling.

PROBLEM EXAMPLE 4

STRAIGHT PATH MOTION OF AN OBJECT

Problem Example 4 is primarily intended as a comprehensive introduction to the use of integrator mode switching, but the programme is sufficiently flexible to allow many experiments in dynamics to be performed.

Several factors can combine to influence the overall motion of an object, and some are shown in the ball problem of Fig. 7.4. A ball thrown vertically into the air will be subject to an initial upward velocity *iv*, retardation or negative acceleration due to gravity $-a$, and air resistance. The situation is further complicated if the ball is projected upwards from an initial height *is*, and is arrested at some height other than zero.

Ignoring for the moment air resistance, the equations which govern the motion of the ball are,

$$v = \int_0^t a\,dt + iv \qquad \text{(Eq. 7.1)}$$

and

$$s = \int_0^t v\,dt + is \qquad \text{(Eq. 7.2)}$$

Clearly, integration of a yields v, and a further integration of v will give s.

The formulae used to calculate velocity or distance when acceleration is constant are,

$$v = iv + at \qquad \text{(Eq. 7.3)}$$

and

$$s = ivt + \tfrac{1}{2}at^2 + is \qquad \text{(Eq. 7.4)}$$

Eq. 7.3 and 7.4 will not apply if, for example, acceleration is proportional to time. A discussion of the implications of variable acceleration lies outside the

scope of this series, but time varying voltage analogues of acceleration are fairly easy to generate on the computer.

The drag on a body moving through air or a fluid conforms to an exponential law, and is proportional to velocity when there is little or no turbulence. Viscous friction should not be confused with the friction resulting from solid surfaces in contact, as the latter is independent of velocity except at very low speeds. A general solution to an equation which describes the motion of an object through a viscous medium—where composite velocities are involved—is often unwieldy and can demand extensive calculations.

However, an exponential decay can be set-up on the computer to simulate true viscous friction, in terms of a coefficient value μ which remains constant for all velocities. Nevertheless, as μ will be dependent on such factors as the surface area, shape, and relative smoothness of an object, it can only be determined by practical experiment, or by comparison between the computer solution and the timed motion of an actual object.

Looking at the symbolised diagram of Fig 7.5, OA1 is employed to integrate a known voltage against time, so that t can be conveniently and accurately displayed as a meter reading. OA2 integrates a to give an output v, and at the same time handles the initial velocity iv. The exponential decay $e^{-(\mu/m)t}$ is introduced by CP1. Resulting velocity v is then integrated by OA3 and initial distance is is included to give distance or height s at any time t.

Routine. Set-up the problem according to the simplified patching circuit of Fig. 7.5 but omit for the time being all C_f capacitors. The integrator switch is linked to the three operational amplifiers by connecting IS/SK1 to OA1/SK9, IS/SK2 to OA1/SK10, IS/SK3 to OA1/SK4, IS/SK4 to OA2/SK9, IS/SK5 to OA2/SK10, IS/SK6 to OA2/SK4, IS/SK7 to OA3/SK9, IS/SK8 to OA3/SK10, and IS/SK9 to OA3/SK4.

Allow the computer to warm up before zero-setting the amplifiers, also make sure that S6 is off. Using the readout meter on its 10V range, zero-set amplifier outputs (OA1/SK13, S3/I5/SK2, and OA3/SK13) by means of VR1 on each amplifier panel, from the back of the UNIT "A" box.

Next insert the C_f computing capacitors into amplifier feedback loop sockets (SK11 and SK12) and set the integrator switching controls to give reset and compute

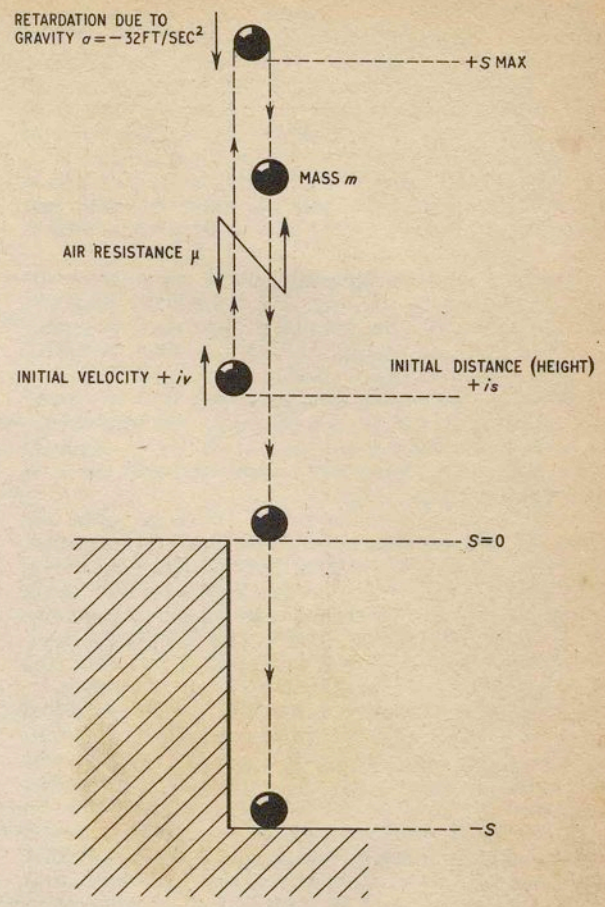
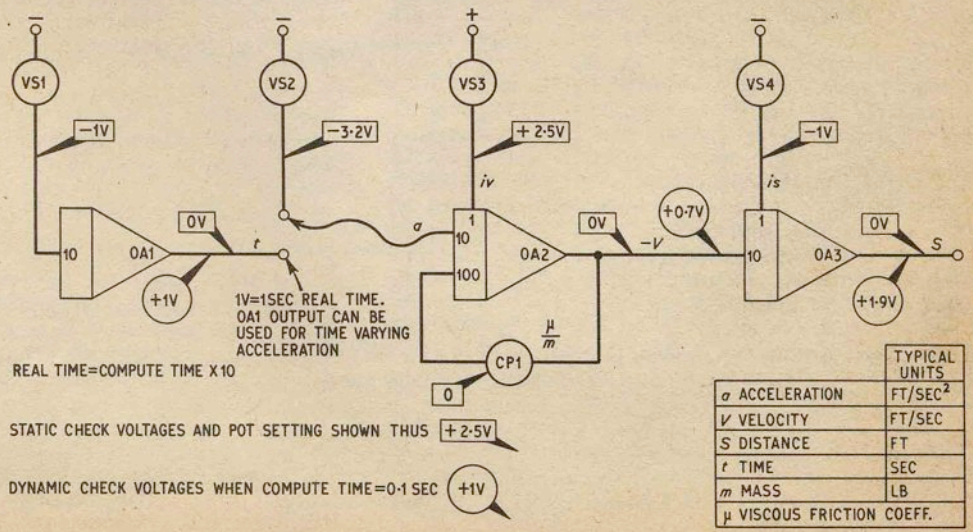


Fig. 7.4. An experiment in dynamics with a ball

times of approximately 0·1 second. Put S8 in the "hold" position. With the readout meter on its 1V range, applied to the output of OA1, press S7 and adjust VR15 for a zero voltage reading. Repeat for OA2 output and VR16, and OA3 output and VR17, in that order. The amplifiers should now be balanced for near zero input offset voltage.



	TYPICAL UNITS
a ACCELERATION	FT/SEC^2
V VELOCITY	FT/SEC
S DISTANCE	FT
t TIME	SEC
m MASS	LB
μ VISCOUS FRICTION COEFF.	

Fig. 7.5. Symbolised diagram of the ball problem illustrated in Fig. 7.4.

To enable static and dynamic checks to be made, trial values are given to the ball problem of Fig. 7.4, as follows: $t_{real} = 1$ sec, $a = -32$ft/sec^2, $iv = 25$ft/sec, $is = 10$ft, $v = -7$ft/sec, $s = 19$ft, and $\mu/m = 0$. The problem scaling is such that 1 computer volt = 10 units in all cases. For example, 1V = 1 sec for t at the output of OA1 (10 × compute time), and 1·9V = 19ft for s at OA3 output. Calculation from the formula Eq. 7.4 shows that the ball will have travelled just beyond s_{max} after a time of 1 sec, when air resistance is zero.

The next stage is to establish all computer static voltages shown in the Fig. 7.5 symbolised diagram, starting with VS1. Set the dial of the master potentiometer to "10" and patch MP/SK1 to SK4, MP/SK2 to SK3, and MP/SK5 to SK8. Connect RM/SK2 to S1/I1/SK2. Switch on S6, set switch S10 to "null" and adjust VS1 dial for a null meter reading, corresponding to a voltage source output of − 1V. Remove the null input patching lead completely, and use it to link RM/SK1 to OA1/SK13.

With the readout meter on its 1V range, press S7, and trim compute time control VR19 for an integrator output of 1V; this will ensure that the compute interval is exactly 0·1 sec. Set up VS2, VS3, and VS4 check voltages, preferably by nulling with the master potentiometer to avoid loading, and rotate CP1 fully anticlockwise. Switch off S6 and press S7 to reset the amplifiers. Check that amplifier outputs are zero.

To obtain dynamic check voltages, switch on S6 and press S7, while applying the readout meter to the outputs of OA1, OA2, and OA3 in turn. For greater convenience, three separate voltmeters can be left connected as shown in the patching circuit of Fig. 7.5 to give simultaneous readouts of t, v, and s. Before altering other problem variables, introduce air resistance by means of CP1 and arrest the travel of the ball at selected positions along its path by adjusting the compute time. It is instructive to compare the velocity and distance of the ball when $a = -32$ft/sec^2 and friction is present, with a ball projected upwards under moon gravity conditions (approximately $a = -5{\cdot}3$ft/sec^2) in a vacuum.

The existing scaling of layout Fig. 7.5 will provide the following coverage: VR2 0–±100ft/sec^2, VR3 0–±100ft/sec, VR4 0–±100ft, with amplifier outputs of OA1 0·1–10sec, OA2 0–±100ft/sec, and OA3 0–±100ft. The coefficient of CP1 covers the range 0–10 for μ/m.

If at any instant during a computer run velocity exceeds 100ft/sec, or distance is greater than 100ft, this will result in amplifier overloading, and a false problem solution. Spot checks of velocity or distance voltage trends can be made at selected compute times, using the single shot facility, and s_{max} will correspond with $v = 0$ at a particular time t. Alternatively, during repetitive integrator switching, an oscilloscope will serve to show amplifier overloads as a flattening or clipping of an output waveform, but this should not be confused with the short "hold" interval which separates the opening and closing of reset and compute switches.

RESCALING PROBLEM EXAMPLE 4

The programme of Problem Example 4 need not be confined to the vertical motion of an object in air, but could equally well apply to movement up and down an inclined plane in water, or else the horizontal progress of a fast wheeled vehicle being decelerated by braking forces, for example.

There are several ways of rescaling Problem Example 4, the most obvious being the adoption of other unit systems, such as miles/hour, centimetres/sec, or even inches/year. Providing that compatible units are employed, and computer voltages are correctly interpreted, there are no serious barriers to unit system rescaling. Probably the most straightforward way of verifying a new problem scaling is to set up a simple check problem, where known values of t, a, v, and s are computed for an object in a vacuum, to establish the relationships between static and dynamic voltages.

Where it is desired to extend the range of an existing unit system, increasing the value of computing capacitors by a factor of ten will reduce real time by ten. Similarly, a tenfold increase in real time is achieved when C_f values are divided by ten.

When employing large computing capacitors at short compute times, always ensure that the reset resistor R_r is small enough to completely discharge C_f during the reset interval. It is also possible to alter the computer voltage scaling so that, for example, 1 computer volt will equal 100 units instead of 10 units, but care should be taken to make sure that *all* voltages and potentiometer settings conform to the new scaling.

Finally, a word or two about variable acceleration. If the input to OA2 is transferred from the VS2 source to the output of OA1, acceleration will then be zero

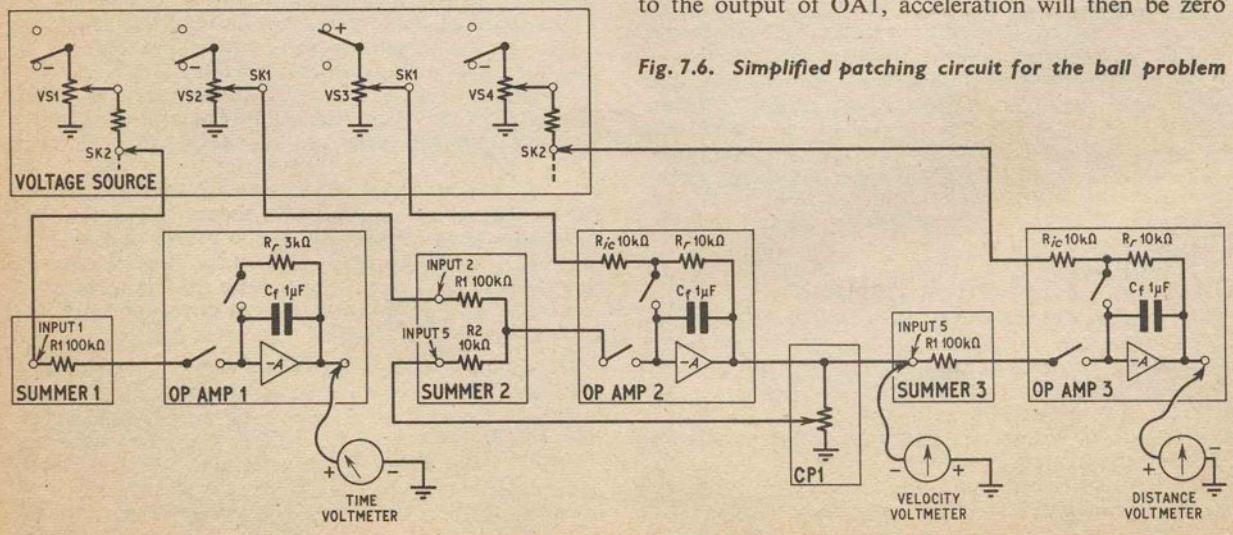


Fig. 7.6. Simplified patching circuit for the ball problem

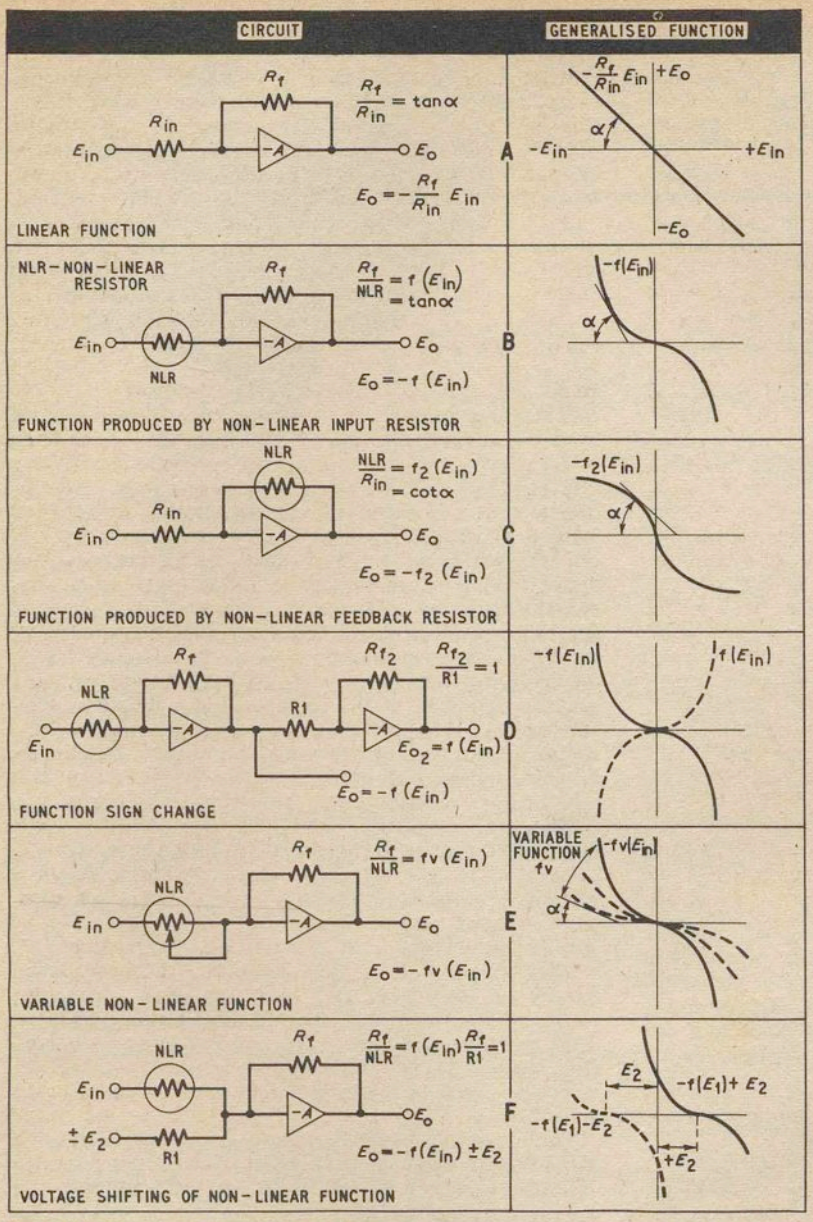


Fig. 7.7. Generating non-linear functions with a voltage dependent resistor

when $t = 0$, and increases linearly to 10ft/sec² when $t = 1$ sec real time. VS1 can be used to adjust the magnitude of a when $t > 0$. Also, if OA1 initial conditions are inserted, in a similar manner to OA2 and OA3, many other time functions of a can be generated.

UNIT "C" FUNCTION GENERATOR

UNIT "C" contains two diode-resistor networks, one for positive input voltages, and the other for negative inputs. The characteristics of each network can be adjusted separately by means of miniature pre-set potentiometers to give a wide range of possible functions, and optimum accuracy. The function generator is designed to be used in place of a normal computing resistor, at the input or in the feedback loop of an operational amplifier.

When employed for squaring an input voltage, with both networks operating in parallel, the function generator will accept input voltages of 0–±10V, and yields amplifier outputs of up to ±10V. Accuracy can be within 2 per cent of the indicated value, depending on the care taken in setting up a function, for input voltages between 0·2V and 9V.

NON-LINEAR FUNCTIONS

Quite often some non-linear function of an applied voltage is needed in analogue computer work, two simple instances being the square or square root of a number. An arbitrary function may also be encountered, perhaps arising from experimental data for which no analytic expression is available.

Servo driven potentiometers and circuits consisting of biased diodes are widely used for generating non-linear functions, but the latter is deservedly popular because it can be adjusted to cater for a range of functions, and does not suffer from a severely limited frequency response.

To show how a diode function generator can give rise to non-linear functions, when allied to operational amplifiers, use is made here of the parallel which exists between the discontinuous behaviour of a biased diode network, and the smooth response of a voltage dependent resistor. Both can display a fall in resistance with an increase in applied voltage.

Consider first of all the circuit and generalised curve of Fig. 7.7a. Input and feedback resistors R_{in} and R_f are not influenced by applied voltage, therefore a straight line function is generated, while amplifier gain and $\tan\alpha$ remains constant. However, if some form of non-linear resistor, or biased diode network, is substituted for R_{in} (NLR in Fig. 7.7b) the gain of the amplifier tends to grow with an increase of E_{in}, and the tangent to the curve will vary according to some function $f(E_{in})$, arising from the characteristic of NLR. A related function $f_2(E_{in})$ results when NLR is exchanged for R_f, as in Fig. 7.7c, but here the amplifier gain falls off with an increase of E_{in}. The curves of Fig. 7.7b and Fig. 7.7c only occupy two of four possible quadrants, but four quadrant operation can be achieved if the function is inverted by a sign changing amplifier, depicted in Fig. 7.7d.

Fig. 7.7e shows how curves, of widely differing slope and magnitude, may be generated if the characteristic of NLR is alterable. Finally, any fixed function will find wider application if its $E_{in} = 0$ datum is shifted, as in Fig. 7.7f. Moreover, as a voltage shift can also be applied to the E_0 axis, it becomes a simple matter to locate any portion of a curve in any quadrant.

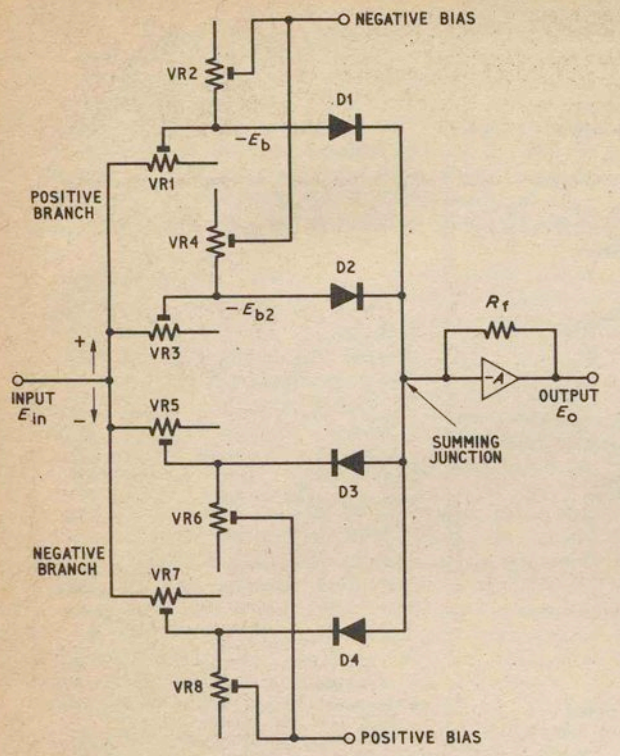


Fig. 7.8a. Circuit of a simple function generator

BIASED DIODE NETWORK

The next step is to see how biased diode networks are used to achieve an increase of resistance with applied voltage, and thus imitate the behaviour of an *ideal* voltage dependent resistor. Unfortunately, currently available silicon carbide, selenium, and copper oxide resistors are far from ideal in many respects, and are not sufficiently accurate for serious use with operational amplifiers.

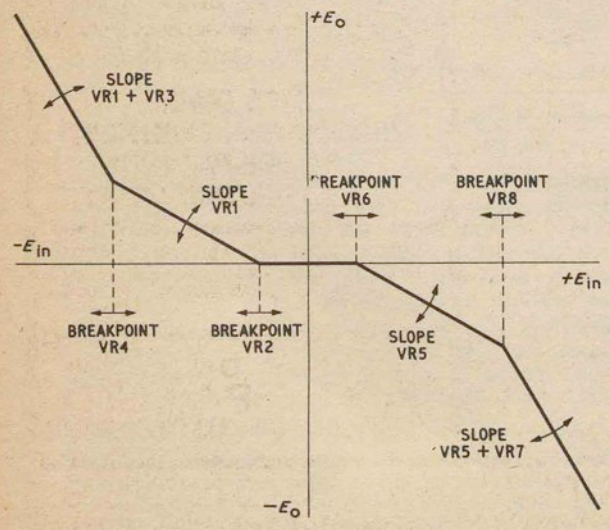
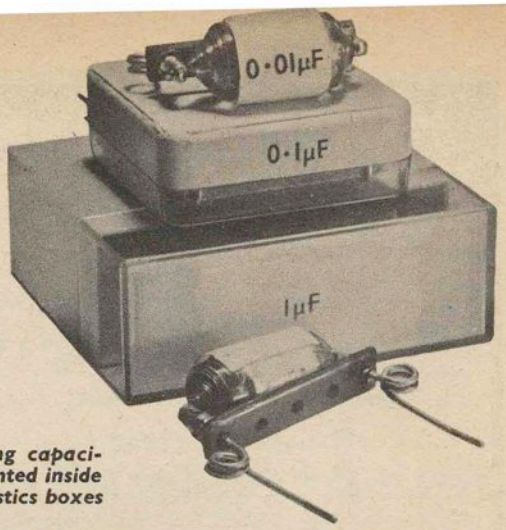


Fig. 7.8b. Adjustable characteristic of simple function generator



Computing capacitors mounted inside small plastics boxes

The UNIT "C" function generator is based on the simple circuit of Fig. 7.8a. In the absence of an input voltage all diodes are biased off, and the network can be represented by a very high value of resistance in series with the operational amplifier input, giving an amplifier gain of almost zero. If a positive voltage is gradually applied to the input terminal, there will be virtually no output until a point is reached where E_{in} is slightly larger than $-E_b$, whereupon D1 conducts and connects VR1 to the operational amplifier summing junction. Further increase of E_{in}, beyond $-E_b$, will produce a straight line output of slope determined by the amplifier gain R_f/VR1.

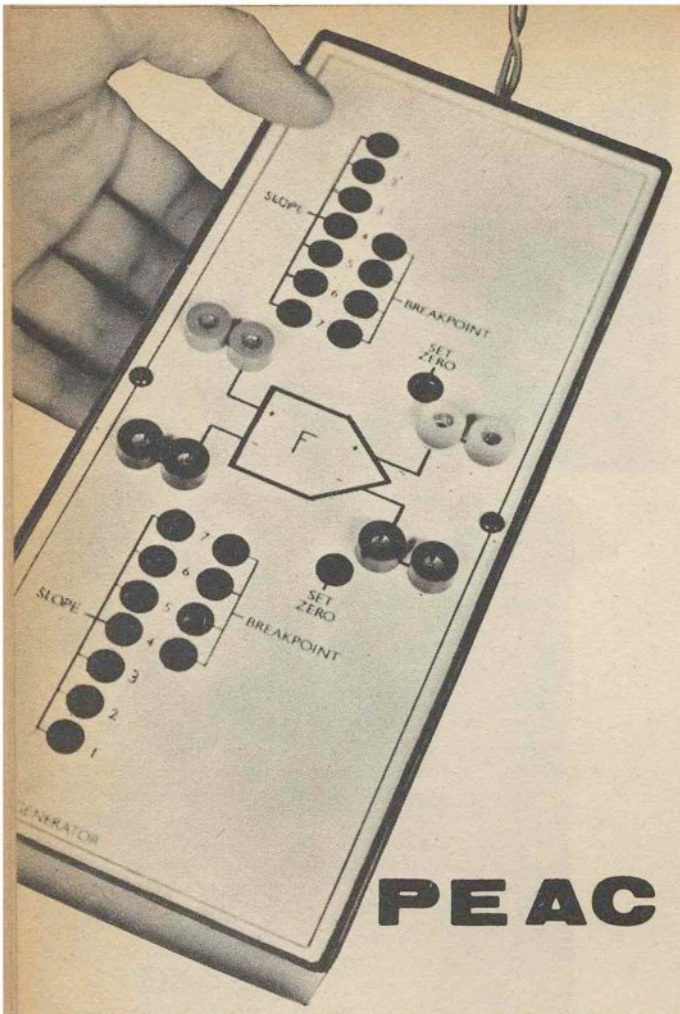
When E_{in} reaches approximately the level of $-E_{b_2}$, D2 conducts and places VR3 in parallel with VR1, thus reducing even more the effective resistance of the network. It can be easily imagined that where a number of diodes and variable resistances are cascaded, the resistance of the network will continue to fall as E_{in} becomes larger still.

Bias voltage $-E_b$ is determined by the relative resistances of VR1 and VR2, and the same applies to $-E_{b_2}$, VR3 and VR4. Furthermore, the setting of VR1 will obviously affect the combined slope of VR1 and VR3 (see Fig. 7.8b), and it follows that all the resistance settings associated with D1 and D2 must be interrelated.

Considerations applying to the positive branch of circuit Fig. 7.8a are also pertinent to the negative branch formed by D3 and D4, and VR5–VR8, except that input and bias voltage polarities are reversed. There is no interaction between the resistance settings of the positive branch and the negative branch, and the two can be separated when required for independent use.

The output characteristic curve of Fig. 7.8b identifies slopes and breakpoints with VR1–VR8. As there are only two diodes in each branch, the result is a very rough approximation to a smooth curve. Generally speaking, the accuracy of a diode function generator is proportional to the number of diodes employed, but a natural rounding at the junction of straight lines does occur at low input voltage levels, due to the dynamic resistance of the diodes (not shown in Fig. 7.8b), so the deviation from a smooth curve is not as great as might be expected. Commercial diode function generators sometimes use more than 20 diodes to achieve accuracies of better than 1 per cent.

Next month: Construction of UNIT "C" and some practical applications of this Function Generator.



ANALOGUE COMPUTER

By D. BOLLEN

LAST month the Function Generator UNIT "C" was introduced. The principle of operation and some of the uses of the function generator were explained. We are continuing with a description of the practical circuit, constructional details, and application information.

FUNCTION GENERATOR CIRCUIT

The function generator circuit of Fig. 8.1 is designed to display a nominal resistance of 100 kilohm when the input voltage is ± 1V. A typical resistance variation with applied voltage is from 500 kilohms at 0·2V to 10 kilohms at 10V. In the Fig. 8.1 circuit, components forming the positive branch are identified by the letter A after a component number, and the letter B is appended to negative branch numbering. As both branches are identical, except for diode and bias polarities, it is not necessary to describe them separately.

D1 is a gold-bonded diode, for a low voltage drop with small input voltages. All other diodes (D2–D7) are of silicon construction to keep reverse leakage low. The natural forward voltage drop of D1 and D2 furnishes self-bias, and bias conditions for D3 are satisfied by a fixed resistor R1. The values of slope adjusters VR1, VR2, VR3, VR4, VR6, VR8 and VR10 were selected to give a parabolic function approximating to $E_0 = E_{in}^2$ when all sliders are at mid-track, and appropriate bias values for that function are provided by mid-track settings of breakpoint adjusters VR5, VR7, VR9 and VR11. The combination VR12 and R3 serves to eliminate offset voltages resulting from diode leakage currents, and VR12 is therefore used for zero-setting.

With so many possible adjustments, including amplifier closed-loop gains determined by R_f or R_{in} computing resistors, it is obviously impossible to catalogue the coverage of the Fig. 8.1 circuit. As a rough indication though, powers of E_{in} ranging from about $E_{in}^{1.1}$ to beyond E_{in}^3 are available. If both branches are cascaded in series with operational amplifiers, the upper limit will extend beyond E_{in}^6. Corresponding root functions $^{1.1}\sqrt{E_{in}}$ to $^6\sqrt{E_{in}}$ may also be generated. It is sometimes possible to use the UNIT "C" function generator for certain trigonometrical functions, and logs to the base 10 or e.

UNIT "C" BOX

A wood and plastics laminate box, of small dimensions compared with other PEAC units, will serve to house the two function generator circuit panels. The suggested form of construction is shown in Fig. 8.2. Softwood blocks are glued to a 9½in × 4in × ¼in plywood frame, which has its centre cut out, and white plastics laminate side pieces are then glued to the blocks. The front panel sits on the wooden blocks and is recessed.

UNIT "C" FRONT PANEL

The only items to be mounted on the 9½in × 4in plastics laminate front panel are eight coloured sockets; the layout is given in Fig. 8.3. A series of ¼in holes are drilled in the front panel to allow screwdriver access to slope, breakpoint, and set-zero controls. Panel markings are similar to previous PEAC units.

FUNCTION GENERATOR CONSTRUCTION

Two 3¾in × 3¾in s.r.b.p. panels are drilled and shaped according to the Fig. 8.4a diagram. Before inserting turret tags, lay the prepared panels out as shown in Fig. 8.5, so that one panel is turned over in relation to the other, and components are clearly seen to be mounted on opposite sides. The underside wiring of the positive branch panel is shown in Fig. 8.4b, and the wiring of the negative branch is in Fig. 8.4c.

All diodes are mounted on turret tags to allow them to be disconnected for special purposes, where for

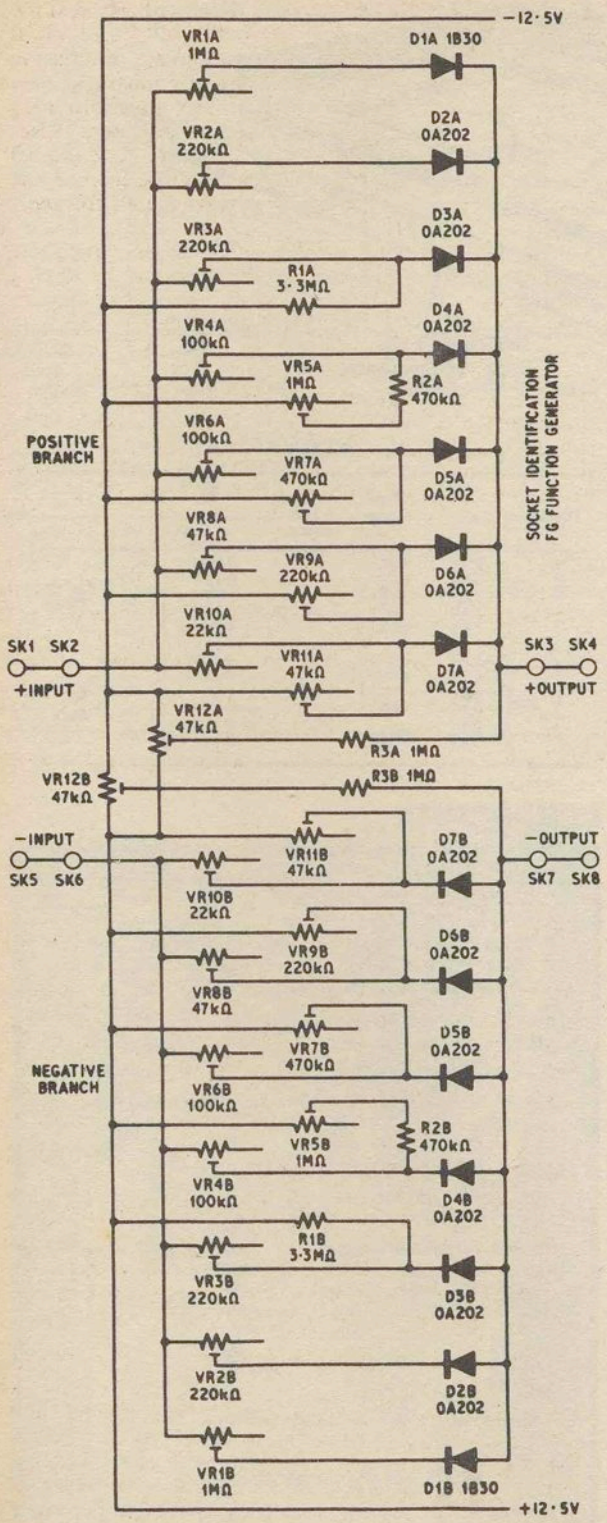
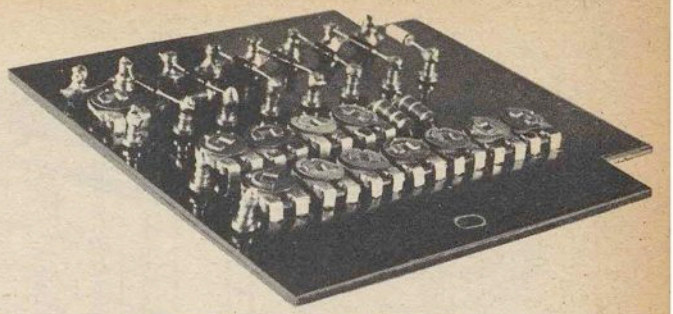


Fig. 8.1. UNIT "C" function generator circuit diagram



Function generator circuit panel

example it is desired to reduce the number of breakpoints, or combine a curved and straight line function. It is advisable to check the polarity of all diodes with a meter before mounting them on the circuit panels.

After completing the underside wiring, bolt the two circuit panels on the plywood frame, as in Fig. 8.5, and make sure that the front panel holes are aligned with the pre-set miniature potentiometer slots.

SETTING UP THE FUNCTION GENERATOR

Patching leads for the function generator should preferably be terminated at one end by miniature plugs, to permit connection to the UNIT "A" computing component sockets. As the generation of powers and roots is the main area of interest, functions related to the square or cube of a number are used in the following setting-up instructions.

To patch the function generator to OA1, join FG/SK5 to S1/I1/SK3, FG/SK8 to S1/I1/SK4, S1/SK5 to OA1/SK8, and link together OA1/SK9, SK10, and SK4. Insert a 100 kilohm computing resistor into OA1/SK11 and SK12. Take a patching lead from S1/I1/SK1 to VS1/SK2, and ensure that S6 is off.

The task of setting up the function generator is made easier if two voltmeters are used, one for E_{in} connected to S1/I1/SK2, and the other for E_0 to OA1/SK13. The Unit "B" readout meter is ideal for monitoring E_0 because it can indicate voltages down to 0·01V. Switch on the computer power supply and zero OA1 by means of its balance control VR15. Set all function generator slope and breakpoint potentiometer sliders to mid-track, and connect the red and blue wires from the function generator to the power supply terminals on the side of the UNIT "A" box (TL1 and TL2). Adjust VR12B (zero-set) for zero output from OA1.

Because of the interdependence of slope and breakpoint adjustments, a systematic approach is called for when setting up a function. Start with the lowest E_{in} and VR1 and proceed in an orderly fashion towards VR11 and the maximum E_{in} value. It is a help to tabulate specific input and output voltages and relate them to particular slope or breakpoint controls. To assist the reader, two tables have been prepared covering square and cube functions, Table 8.1 and Table 8.2.

If a square function is to be set up on the function generator, switch on S6 (Voltage Source) and set VS1 for an output of −0·2V, then adjust VR1B for an OA1 output of 0·04V. Next set VS1 for −0·5V and adjust VR2B for an output of 0·25V, and so on, according to Table 8.1. After application of $E_{in} = -2{\cdot}0V$, and adjustment of VR4, change the 100 kilohm computing resistor in the feedback loop of OA1 to 10 kilohm, to prevent the amplifier overloading when E_{in} exceeds $\sqrt{10}$.

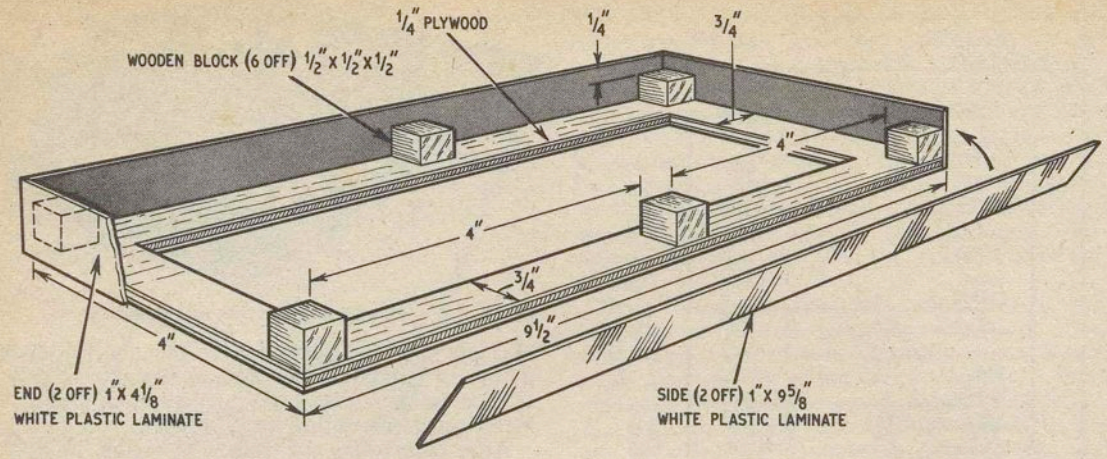


Fig. 8.2. Details and measurements of UNIT "C" function generator case

TABLE 8.1

Diode	E_{in}	Adjust slope	Adjust break-point	E_o	
1	−0·2V	VR1	—	+ 0·04V	$E_o = E_{in}^3$ $R_f = 100k\Omega$
2	−0·5V	VR2	—	+ 0·25V	
3	−1·0V	VR3	—	+ 1·0V	
4	−1·5V	—	VR5	+ 2·25V	
	−2·0V	VR4	—	+ 4·0V	
5	−2·5V	—	VR7	+ 0·625V	$E_o = \frac{E_{in}^3}{10}$ $R_f = 10k\Omega$
	−3·5V	VR6	—	+ 1·225V	
6	−4·0V	—	VR9	+ 1·6V	
	−6·0V	VR8	—	+ 3·6V	
7	−6·5V	—	VR11	+ 4·225V	
	−9·0V	VR10	—	+ 8·1V	

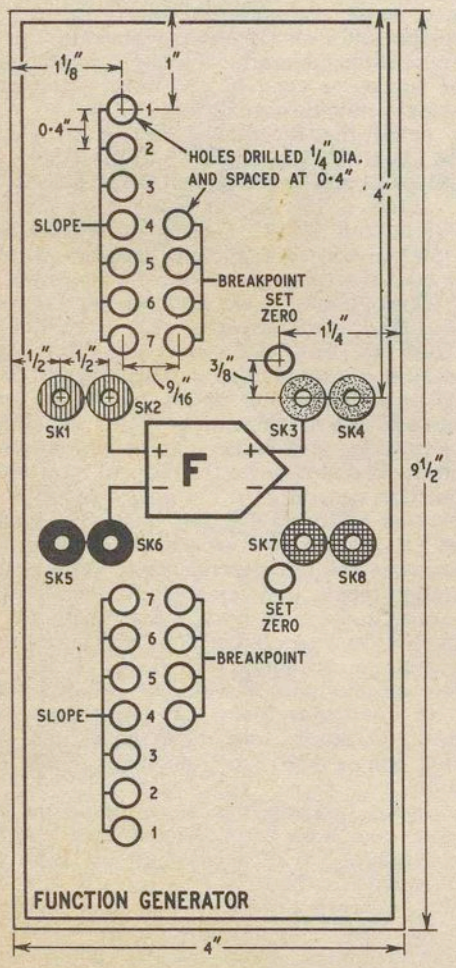


Fig. 8.3. Front panel layout of UNIT "C" function generator

COMPONENTS . . .

UNIT "C" BOX
Plywood 9½in × 4in × ¼in
Softwood ½in × ½in × 3½in
White plastics laminate 9⅝in × 1in (2 off), 4⅛in × 1in (2 off)
Rubber grommet ¼in × $\frac{5}{32}$in

UNIT "C" Front Panel
White plastics laminate 9½in × 4in. Sockets: 2 red, 2 yellow, 2 black, 2 blue.

UNIT "C" Function Generator Components

Resistors
R1 3·3MΩ (2 off)
R2 470kΩ (2 off)
R3 1MΩ (2 off)
All 10%, ½W carbon composition

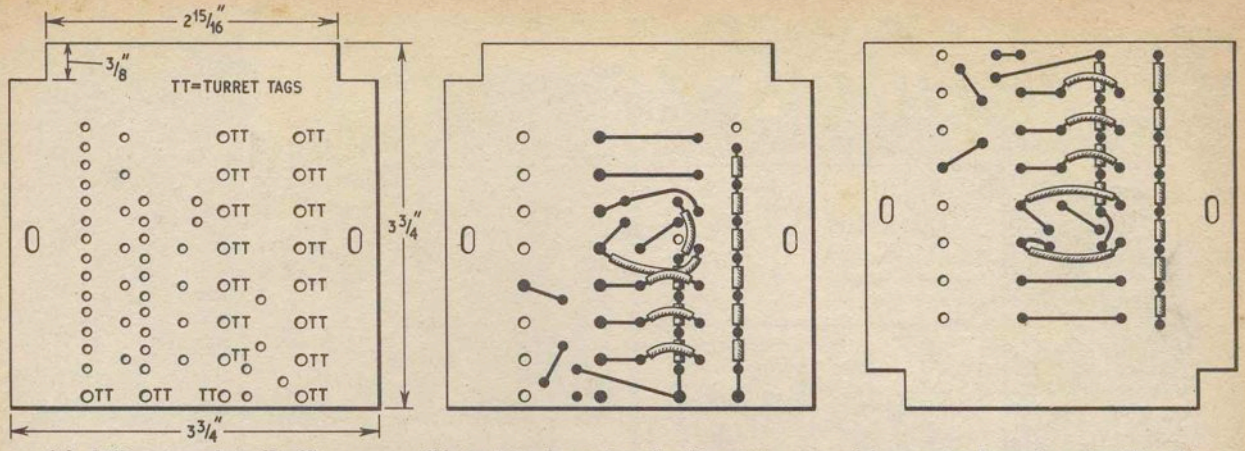
Pre-set Potentiometers

VR1, VR5	1MΩ	(4 off)
VR2, VR3, VR9	220kΩ	(6 off)
VR4, VR6	100kΩ	(4 off)
VR7	470kΩ	(2 off)
VR8	47kΩ	(2 off)
VR10	22kΩ	(2 off)
VR11, VR12	47kΩ	(4 off)

All miniature horizontal mounting

Diodes
D1 1B30 (2 off) (Radiospares)
D2–D7 OA202 (12 off)

Miscellaneous
S.R.B.P. 3¾in × 3¾in (2 off). Small turret tags 4mm stackable plugs, one red, one blue (Radiospares)

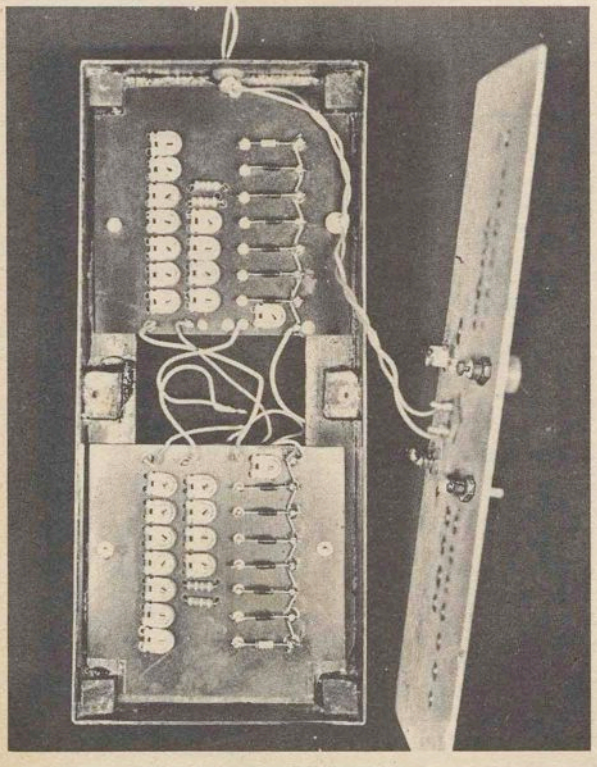


(a) drilling template (2 off) (b) positive branch underside wiring (c) negative branch underside wiring

Fig. 8.4. Function generator circuit panels (2 off)

TABLE 8.2

Diode	E_{in}	Adjust slope	Adjust break-point	E_o	
1	−0·3V	VR1	—	+ 0·027V	$E_o = E_{in}^3$
2	−0·5V	VR2	—	+ 0·125V	R_t = 100kΩ
3	−0·75V	VR3	—	+ 0·421V	
4	−1·0V	—	VR5	+ 1·0V	
	−1·25V	VR4	—	+ 1·953V	
5	−1·5V	—	VR7	+ 3·375V	
	−2·0V	VR6	—	+ 8·0V	
6	−2·5V	—	VR9	+ 1·56V	$E_o = \frac{E_{in}^3}{10}$
	−3·0V	VR8	—	+ 2·7V	R_t = 10kΩ
7	−3·5V	—	VR11	+ 4·287V	
	−4·64V	VR10	—	+ 10·0V	



Interior view of UNIT "C" function generator

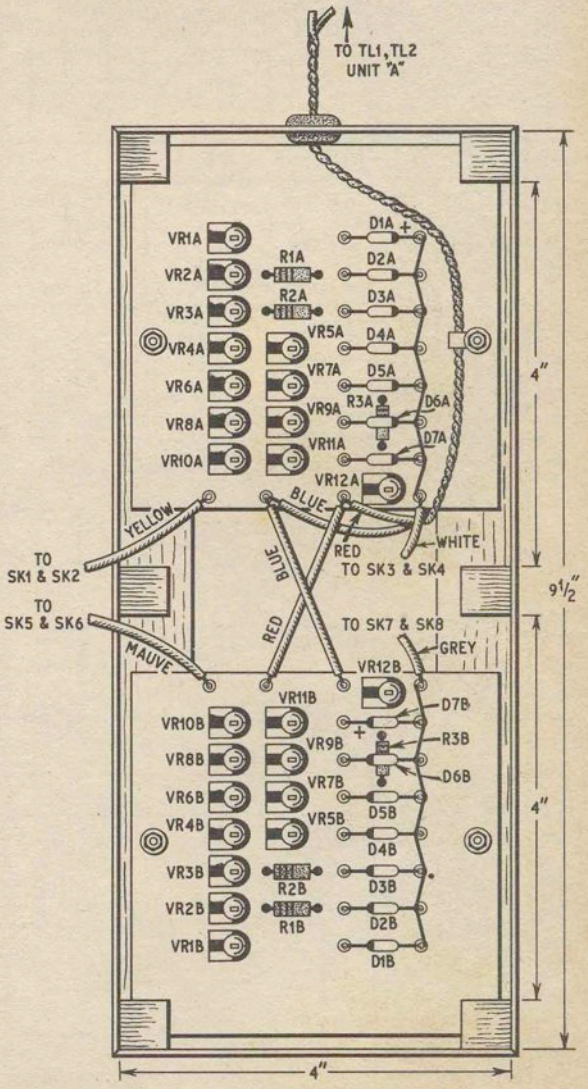


Fig. 8.5. Topside and interconnecting wiring of function generator panels. The circuit boards are shown in position inside the UNIT "C" case

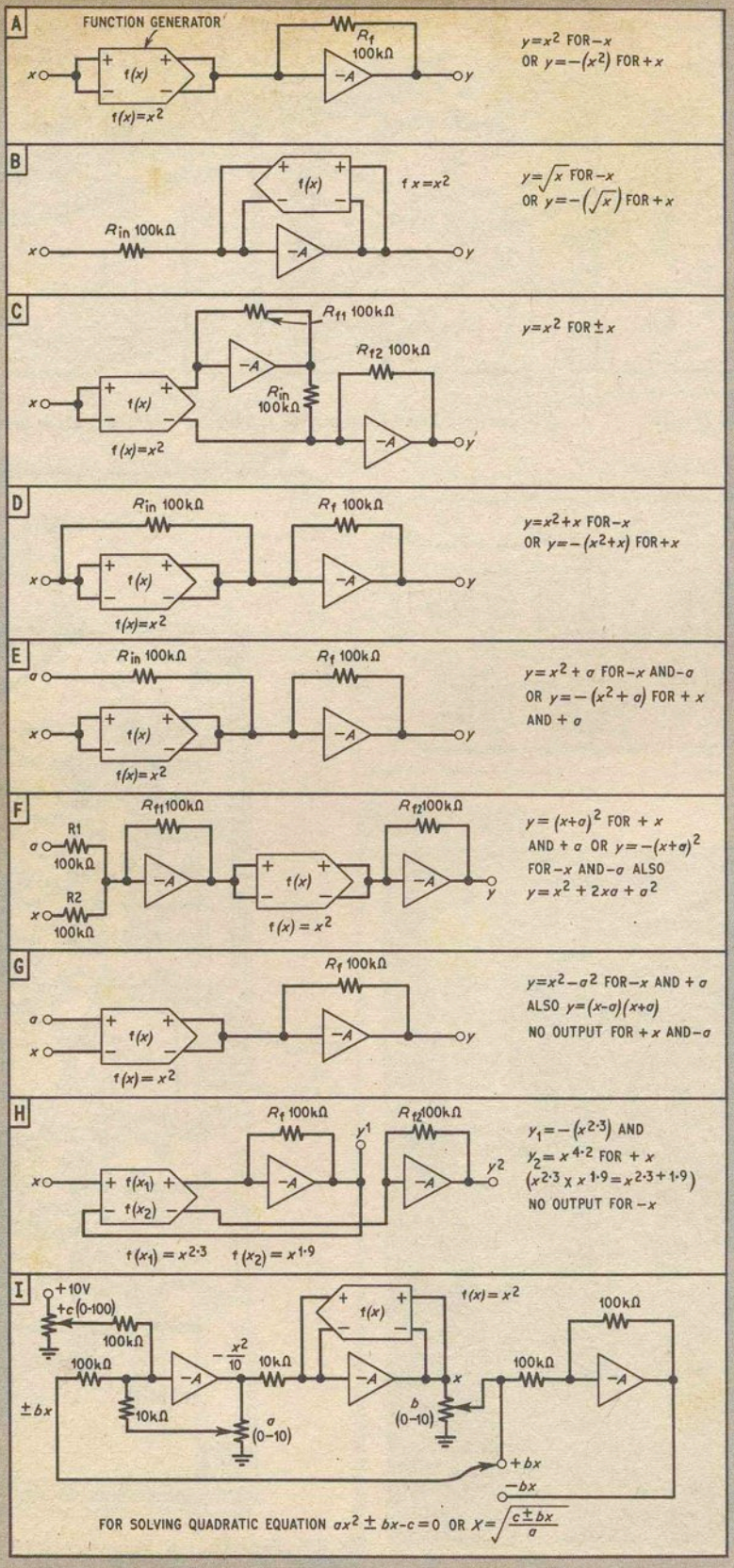
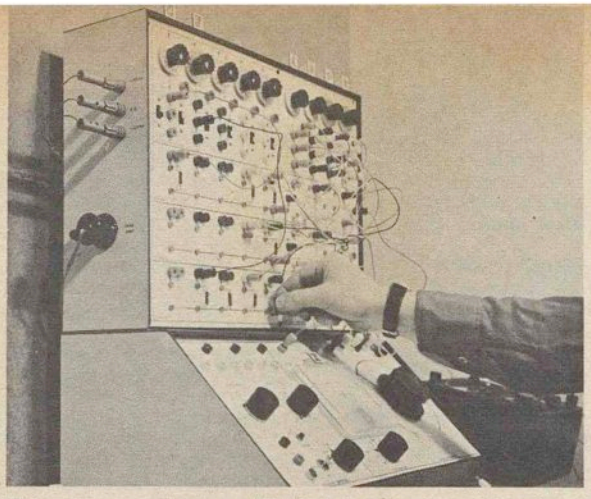


Fig. 8.6. The function generator used for equation solving



This photograph shows PEAC being used to solve simultaneous equations

After the entire range of input voltages listed in Table 8.1 has been covered, return to $E_{in} = -0{\cdot}2V$ and go through the procedure again, to achieve optimum accuracy. The positive branch can be set up for the same function as the negative branch by transferring patching leads from FG/SK5 to SK1, and FG/SK8 to SK4, but this time trim VR12A for zero-set, and apply positive values of E_{in}. It may be necessary to slightly re-adjust slope controls VR1–VR3 when the two branches are connected in parallel, if there is some small bias voltage imbalance.

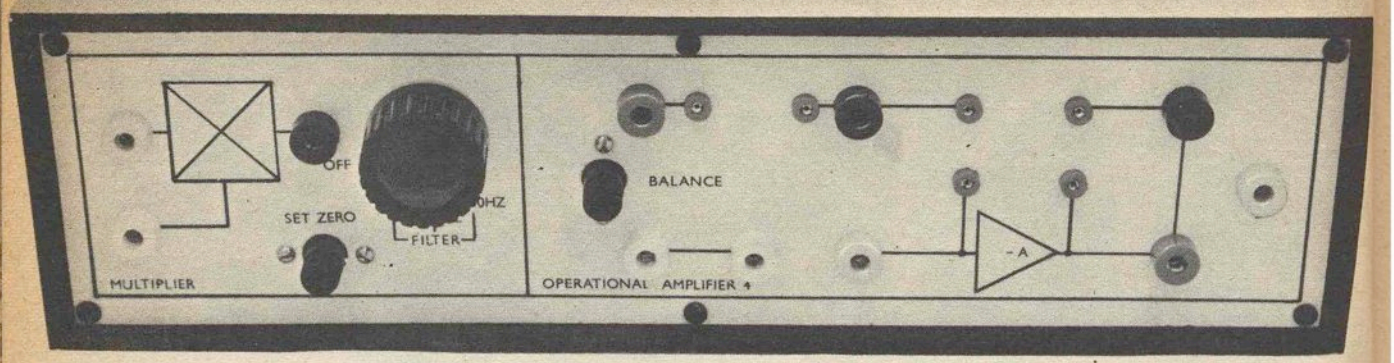
THE FUNCTION GENERATOR IN EQUATION SOLVING

The fact that an analogue computer can produce and handle imaginary numbers will be particularly evident when the function generator is applied to equation solving, see Fig. 8.6. One type of function generator circuit configuration will produce consistant outputs for, say, the cube of a number, but not for its square, or vice versa, because $\pm x^2 = +y$, but $+x^3 = +y$, and $-x^3 = -y$. The computer operator must therefore choose, or devise, the appropriate circuit for a given task.

Output y in Fig. 8.6a will be of the required sign when the input is $-x$, but the sign of y with an input of $+x$ cannot be reconciled with mathematical convention. However, the circuit of Fig. 8.6a does provide a consistant output when the function is x^3, with inputs of $\pm x$. Much the same applies to the Fig. 8.6b circuit, which shows the function generator arranged for square root operations. Circuit Fig. 8.6c reverses the above situation and gives consistent outputs for a square function, but not for a cube function, by employing an extra sign reversing amplifier.

Getting away now from the complexities of square roots of negative numbers and other mathematical anomalies, Fig. 8.6d can be made to give outputs of $y = x^2 + x$, or some other combination such as $y = x^{2.5} - 3x$, depending on the choice of function, voltage polarities, and computing resistor values. The purpose of other circuits E–H will be self-evident in Fig. 8.6. Fig. 8.6i gives the symbolised layout for solving a quadratic equation, where x is unknown and a, b, and c are constants. The function generator can also be introduced into problem set-ups where integrating amplifiers are used, as its frequency response is well in excess of any frequency likely to be encountered.

Next month: The final item of the PEAC equipment, UNIT "D", will be described.



ANALOGUE COMPUTER PEAC

By D. BOLLEN

THIS month's article deals with UNIT "D"—the multiplier, which is the final piece of PEAC equipment. After a technical description, details of the construction and setting up are given.

The servo driven potentiometer has been widely employed in the past for multiplication of one variable voltage by another, but its frequency response, in most cases, is seldom better than 0–5Hz. Modern analogue computers now tend to use all solid-state multiplier circuits, which have a frequency response extending into the kHz region, but they are both complex and expensive. Taking the quarter-square multiplier as an example, it needs five operational amplifiers and two diode function generators to produce an accurate product voltage from two inputs. It follows, therefore, that analogue multiplier circuit design can be expected to present considerable difficulties when cost is an important consideration.

UNIT "D"—THE MULTIPLIER

Working on the premise that even a multiplier of restricted performance can make a worthwhile contribution to an analogue computer which lacks such a facility, an accuracy of $\pm 2{\cdot}5$ per cent and a frequency response of 50Hz under the most favourable conditions was considered to be an acceptable specification for the UNIT "D" multiplier. Although 0–50Hz seems rather limited by ordinary electronic standards, in the context of "parallel" computer circuit operation it represents a useful compute time which compares favourably with the servo multiplier.

UNIT "D" contains three distinct circuits, two operational amplifiers and a bistable reed relay driver. One of the amplifiers is identical to those used with UNIT "A", and is available as a multi-purpose operational amplifier when the multiplier is not in service.

TIME DIVISION

With the time division multiplier, a square wave is modulated in such a way that the mark/space ratio is proportional to one input voltage, while the amplitude of the waveform is proportional to another input voltage. The mean value of the resulting waveform is then proportional to the product of the two input voltages.

Looking at Fig. 9.1, which sets out the simplified multiplier circuit with associated waveforms, a voltage E_2 is compared with a fixed voltage E_3 at the input of the integrating amplifier. A bistable relay is arranged to switch S1 and S2 when the integrator output reaches a pre-determined value, conveniently about two thirds of the maximum available amplifier output swing. If the sign of E_3 at the S1 contacts is correct, the feedback will be positive, and a self-sustained oscillation at a frequency determined mainly by E_2 and C_1 will result. When $E_2 = 0$ the output from the integrator will consist of a sawtooth or symmetrical ramp waveform, with identical rising and falling slopes, which is generated by E_3.

Assume now that a voltage E_2 is applied; this will be added to, or subtracted from E_3, depending on the position of the S1 switch. The ramp waveform is therefore modified to an asymmetric form where the rising and falling slopes become dependent on the level and sign of E_2.

Waveform (a) in Fig. 9.1 depicts the asymmetric ramp for $+E_2$ and $-E_2$, while waveform (b) shows the square wave generated by the switch, of mark/space dependent on the magnitude of E_2. As S2 is synchronised with S1, so the input resistor R1 will be alternately switched to the inverting and non-inverting inputs of the product amplifier, and will remain at each contact for a time dependent on the frequency and mark/space of the switching waveform.

The amplitude of the product amplifier output is

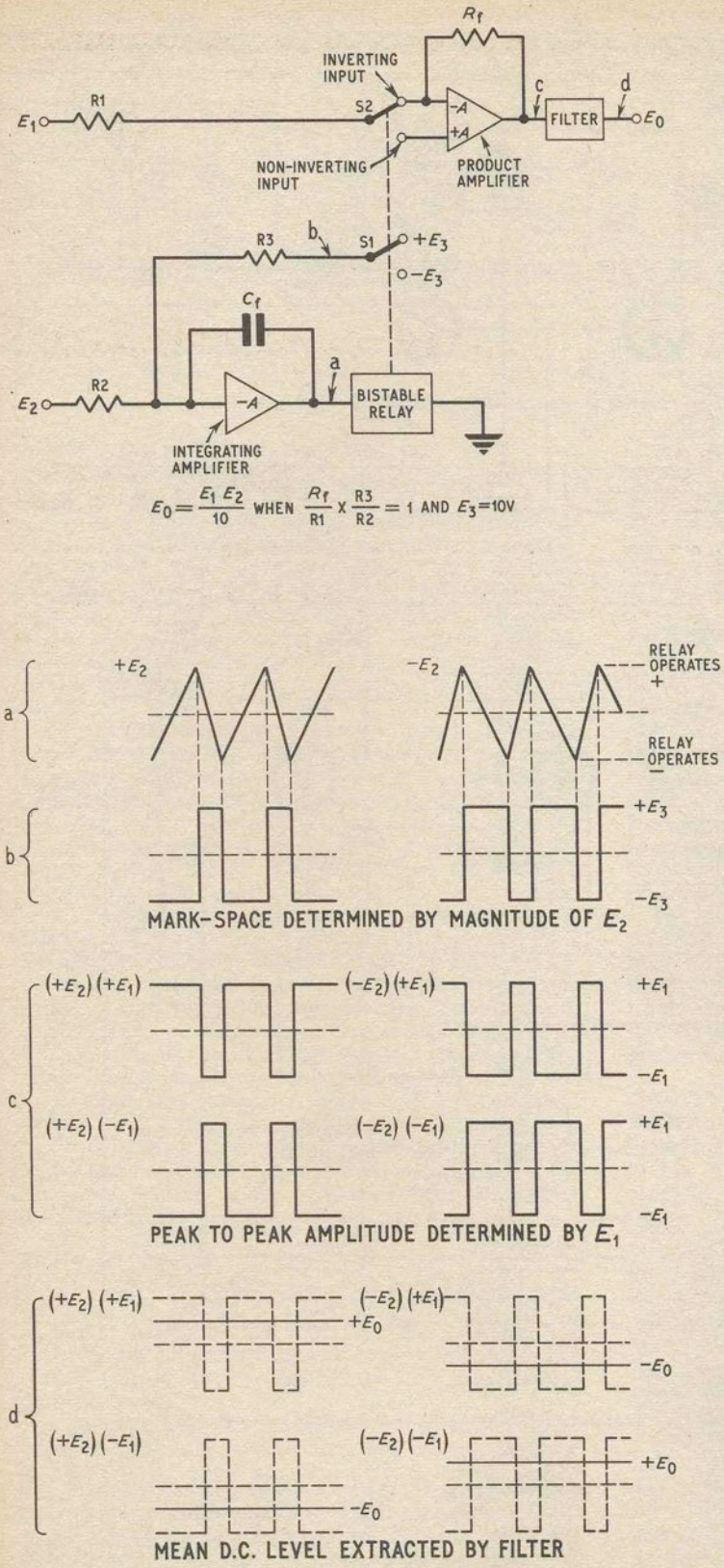


Fig. 9.1. Time division multiplier with associated waveforms

COMPONENTS . . .

UNIT "D" FRONT PANEL AND BOX

Potentiometers
VR25 100Ω wirewound
VR26 50Ω wirewound
(both panel mounting type)

Switches
S11 3 pole, 4 way rotary
S12 Double-pole slide switch (c/o contacts)

Sockets
2 red, 2 blue, 1 black, 2 yellow, 3 white, 1 green, and 6 miniature sockets

Miscellaneous
Material for front panel and box. Hardboard, 2 off 12⅜in × 4½in, 2 off 4½in × 3 3/16in. White plastic laminate, 2 off 12⅜in × 4½in, 2 off 3½in × 4½in, 1 off 12in × 3⅛in. Softwood, 25in × ½in × ½in. Knob, one Radiospares 1⅛in type PK with pointer.

UNIT "D" BISTABLE RELAY AND PRODUCT AMPLIFIER

Resistors

R1	1kΩ	*R14	10kΩ 1%
R2	4·3kΩ	R15	1kΩ
R3	4·3kΩ	R16	820Ω
R4	4·3kΩ	R17	820Ω
R5	1kΩ	R18	1kΩ
R6	100Ω	R19	8·2kΩ
*R7	11kΩ 1%	R20	22kΩ
R8	10kΩ	R21	22kΩ
R9	27kΩ	R22	8·2kΩ
R10	2·2kΩ	*R23	200Ω 2%
R11	100Ω	*R24	1kΩ 2%
*R12	10kΩ 1%	*R25	1·2kΩ 1%
*R13	9·1kΩ 1%	*R26	300Ω 1%

(All 10% ½ watt carbon composition except * = 1W metal oxide)

Potentiometers
VR1 100kΩ vertical skeleton pre-set
VR2 220Ω miniature horizontal pre-set

Capacitors
C1 1μF polyester 250V d.c.
C2 0·25μF polyester 250V d.c.
C3 1μF elect. 15V
C4 8μF elect. 15V
C5 100μF elect. 15V

Transistors
TR1, TR2 2N2926 (orange) *or* 2N3904 (2 off)
TR3 2N3906
TR4 2N3904
TR5, TR6 ACY28 *or* AC126 (2 off)

Diodes
D1–D4 OA202 (4 off)

Choke
L1 5H (Radiospares "Midget" type)

Reed coils
RLA, RLB Miniature triple 12V Osmor type MT12V (2 off)

Reed switches
RLA1, RLA2 Hamlin MRG2 20-40AT (4 off)
RLB1, RLB2

Miscellaneous
S.R.B.P., 1 off 3in × 3¼in, 1 off 3in × 4½in. Small turret tags. Baseboard 12 in × 4in s.r.b.p. or plastic laminate

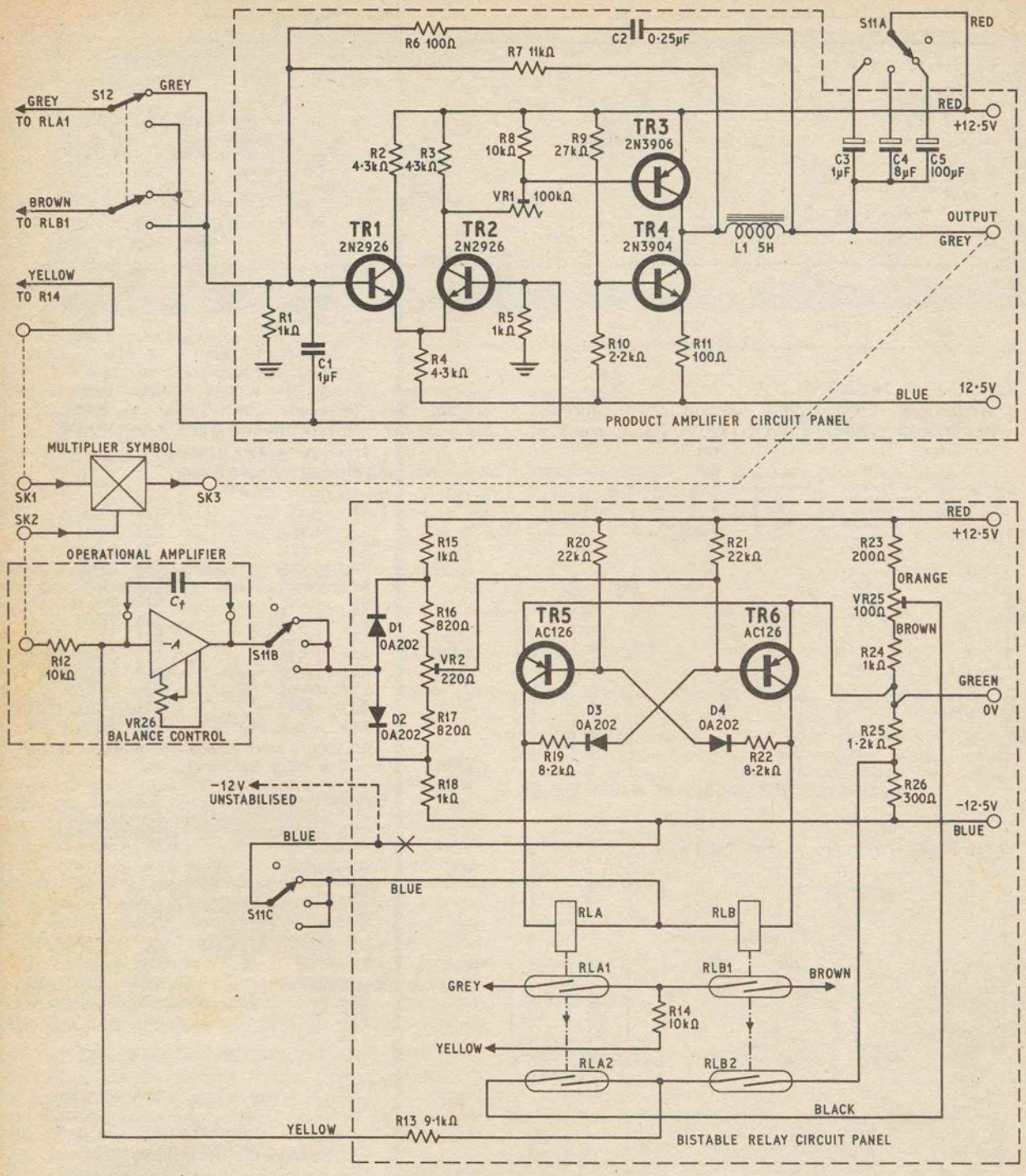


Fig. 9.2. Multiplier circuit, comprising product amplifier panel and bistable relay panel

wholly dependent on E_1, but whatever the value of E_1 it will be divided by $10/E_2$ (time division), which is the same thing as $(E_1 \times E_2)/10$, assuming of course that appropriate values for R1–R3, R_f and E_3 are chosen.

Waveforms (c) shows what happens to different signs of E_1 and E_2, in terms of the square wave. If now the mean voltage level of the output from the product amplifier is extracted by a suitable filter (see waveform (d)) it can be seen that four quadrant multiplication has been achieved. When E_1 and E_2 are both positive, or both negative, the product voltage will be positive, but when E_1 and E_2 are of opposite sign, the product becomes negative.

The multiplier circuit will now be described.

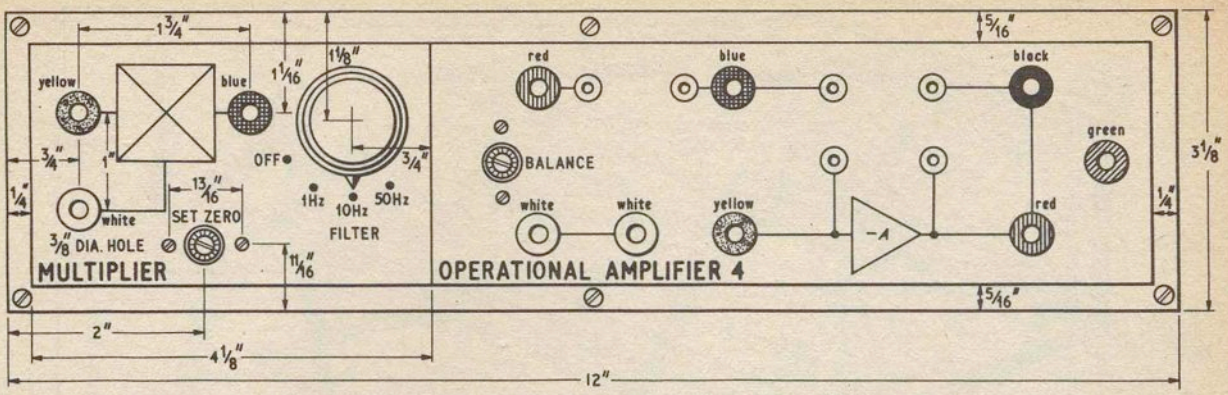


Fig. 9.3. Dimensions and engraving details for UNIT "D" front panel

UNIT "D" MULTIPLIER CIRCUIT

As the operational amplifier circuit has already been given in connection with UNIT "A", it appears in symbolised form only in the multiplier circuit of Fig. 9.2, with VR26 as the front panel balance control, and a fixed value of input resistor R12 provided internally for use with the multiplier. As the feedback capacitor C_f only affects the integrator waveform frequency, without altering other multiplier characteristics, it is useful to leave it as a plug-in component, so that the multiplier carrier frequency can be adjusted easily.

The output from the integrator, which it will be remembered from Fig. 9.1 carries information as to the magnitude and sign of input E_2, is fed via S11B to a diode resistor network composed of D1, D2, R15–R18, and VR2, the purpose of which is to allow the following bistable relay driver to be switched at precisely determined voltage levels. VR2 establishes the working point of the diode resistor network.

A conventional cross-coupled multivibrator is utilised as a relay driver, with reed coils RLA and RLB forming the respective collector loads of TR5 and TR6. D3 and D4 are used to ensure a "cleaner" switching action at high repetition rates, and the bistable circuit will function satisfactorily at frequencies in excess of 100Hz without undue relay contact bounce. The reference voltage, which was shown as $\pm E_3$ in Fig. 9.1, is extracted from a resistor network R23–R26 and VR25 in Fig. 9.2. VR25 allows positive and negative values of E_3 to be made equal. E_3 voltages are then fed, via RLA2 and RLB2 switches, and resistor R13, back to the summing junction of the integrator, thus completing the closed-loop to maintain oscillation.

SIGN CHANGE

The square wave switching cycle is presented to the input of the product amplifier by RLA1 and RLB1, with R14 acting as the input resistor. Changeover switch S12 is included to allow the sign of the multiplier output voltage to be changed to suit a particular problem set-up.

A product amplifier open-loop gain of about 1,000, which is the gain of the Fig. 9.2 circuit, is quite satisfactory for good accuracy when working with a fixed, closed-loop gain close to unity. Long-tailed pair TR1 and TR2 provide inverting and non-inverting inputs, while TR3 is the output transistor, and TR4 forms a constant current load for TR3, in place of a fixed resistor, thus enabling larger loads to be driven without excessive dissipation. VR1 serves to zero the amplifier output.

The ratio of resistors R7 and R14 gives a product amplifier gain (closed-loop) of 1·1, while R13/R12 yields an equivalent gain for the integrating amplifier of 0·91. The lower value of gain for the integrator enables E_2 to equal E_3 without stopping the integration cycle, and yet the overall gain of the multiplier is still unity because $1{\cdot}1 \times 0{\cdot}91 = 1$.

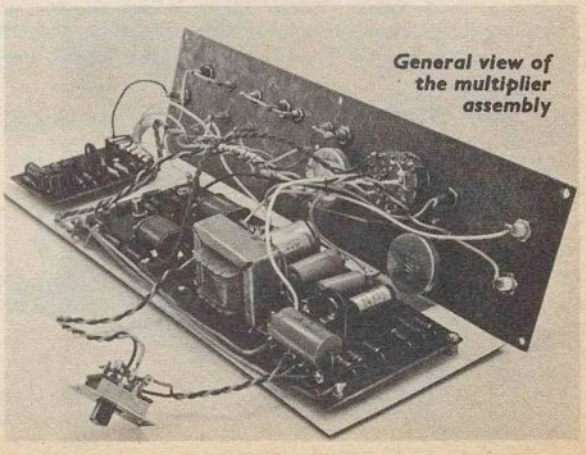
FILTER CIRCUIT

The purpose of the filter circuit L1, C2–C5, R6, and S11A, is to remove the square wave carrier without distorting the product waveform when input voltages are time varying. Bearing in mind that computer waveforms are extremely diverse, it is almost impossible to achieve near perfect results with one filter circuit, especially when the carrier frequency is not far removed from input frequencies. To allow compromise, therefore, the cut-off frequency of the Fig. 9.2 filter can be set by switch S11A to suit the circumstances of a particular problem set-up.

The three switch positions, 1Hz, 10Hz, and 50Hz, represent approximately the roll-off points given by the filter, and the bandwidth handled by the multiplier. In the 1Hz position the filter will virtually eliminate carrier ripple when input voltages are of very low frequency, but the 50Hz setting is used with fast integrator waveform inputs, where ripple may be less objectionable.

CONSTRUCTION OF UNIT "D" FRONT PANEL AND BOX

Details of the UNIT "D" front panel and box appear in Fig. 9.3 and Fig. 9.4. Note that the operational amplifier (OA4) socket positions and panel markings



General view of the multiplier assembly

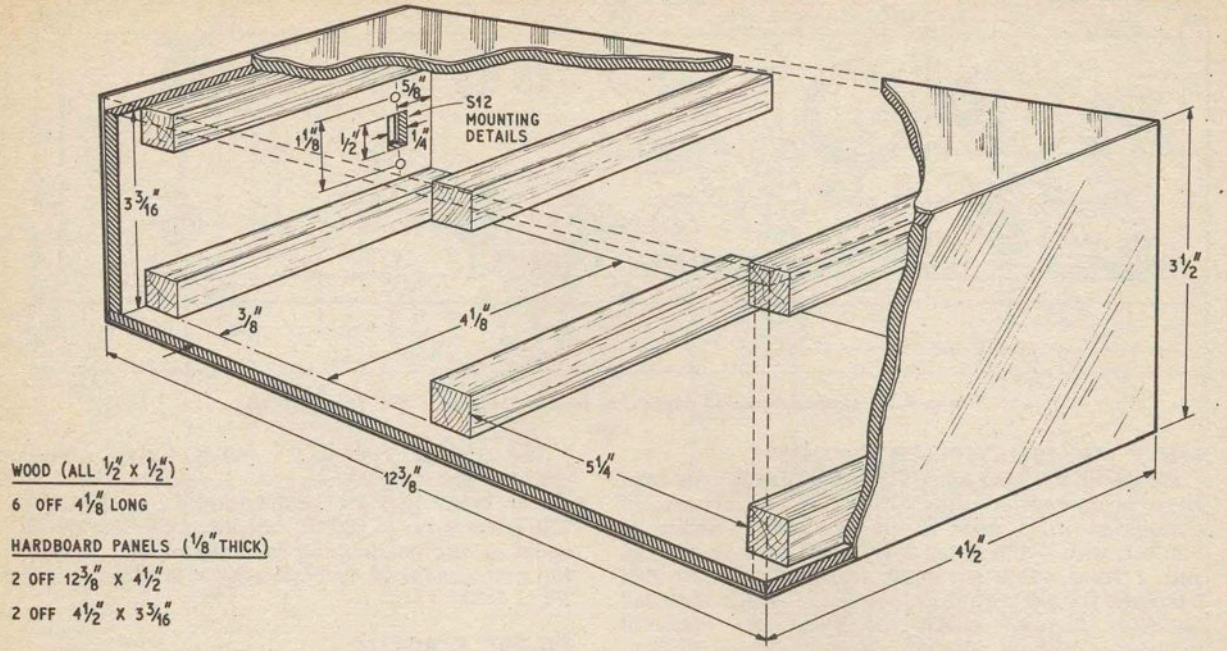


Fig. 9.4. Construction of the box for UNIT "D"

are the same as for UNIT "A" operational amplifiers. S11, VR25, VR26, and all sockets may be mounted after the front panel has been marked and drilled.

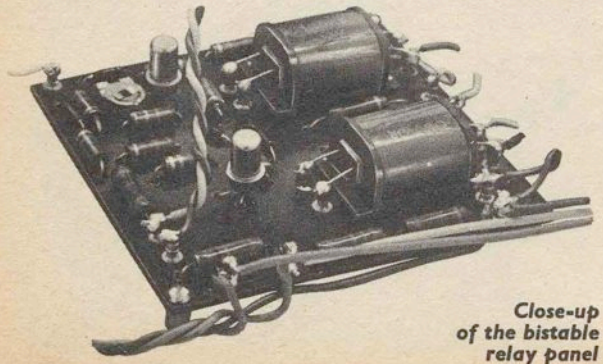
INTERNAL LAYOUT OF THE MULTIPLIER

The internal layout and interconnecting wiring of the multiplier are shown in Fig. 9.5. Operational amplifier, bistable relay driver, and product amplifier circuit panels are bolted with stand-off spacers to a 12in × 4in s.r.b.p. or plastics laminate baseboard, which rests on the wooden bearers at the base of the UNIT "D" box.

Component placement positions for the bistable relay circuit panel, and the product amplifier panel, also appear in Fig. 9.5, together with a rear view of the front panel assembly. The operational amplifier (OA4) is made up in accordance with instructions given in the May issue of PRACTICAL ELECTRONICS (pages 209–210).

BISTABLE RELAY CIRCUIT CONSTRUCTION

Drill the bistable relay circuit panel according to Fig. 9.6, and insert turret tags. Then mount all components and complete underside wiring, leaving the reed switches RLA1, RLA2, RLB1, and RLB2 until last. A triple reed coil is specified for the Fig. 9.2 circuit, to allow the addition of an extra pair of reed switches if the multiplier is to be enlarged to cater for three input voltages; this modification will, of course, also involve the construction of another product amplifier.



Close-up of the bistable relay panel

PRODUCT AMPLIFIER CIRCUIT CONSTRUCTION

Drilling details and underside wiring of the product amplifier panel appear in Fig. 9.7. Accurate matching of input transistors TR1 and TR2 may not be necessary with this low gain circuit. A 2N2926 transistor should not be employed in the TR4 position, in place of the 2N3904, as its maximum V_{ce} will be exceeded.

After inserting turret tags, mount resistors and transistors first, then follow with L1, and capacitors C2–C5. C1 is soldered into position last of all, across the amplifier input turret tags, as shown in Fig. 9.5.

FINAL ASSEMBLY AND SETTING UP OF UNIT "D"

Mount the three circuit panels on the baseboard and complete all interconnecting wiring between the circuit panels and the front panel, including S12 which can be left floating for the time being. The resulting assembly can be set-up and tested out of its box.

Connect red, green, and blue flexible wires from the bistable relay panel to the UNIT "A" power supply solder tags, or alternatively to TL1, TL2, and TL3 with stackable plugs.

Place S11 in the "off" position and zero-set the operational amplifier (OA4) following instructions given earlier for UNIT "A" amplifiers, after allowing the usual warm-up period. When adjusting the VR26 balance control connect M/SK2 to any earth socket with a patching lead. Next, attach a sensitive d.c. voltmeter (0–1V) to M/SK3 and zero-set the multiplier output by adjustment of VR1 on the product amplifier circuit panel.

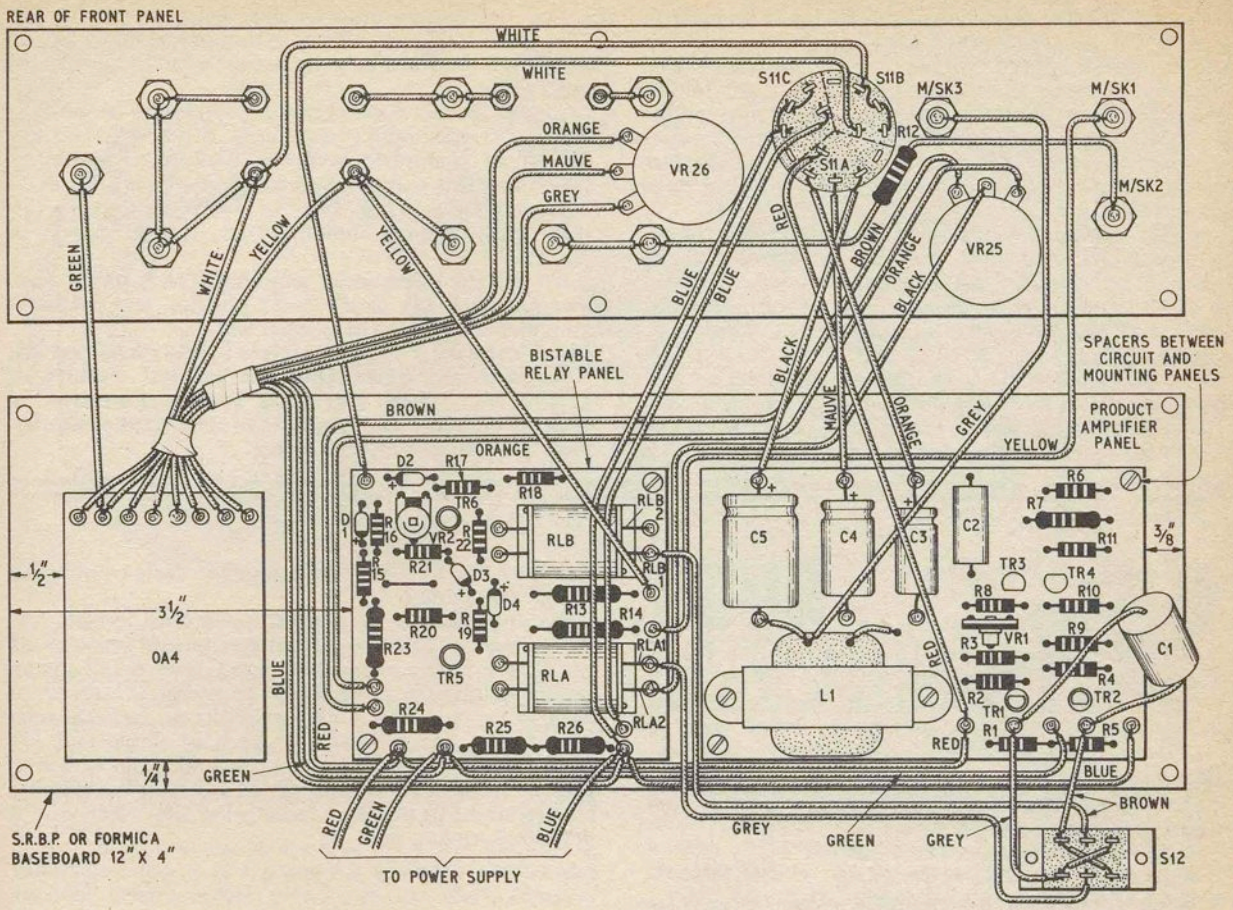


Fig. 9.5. Internal layout and wiring of UNIT "D" multiplier

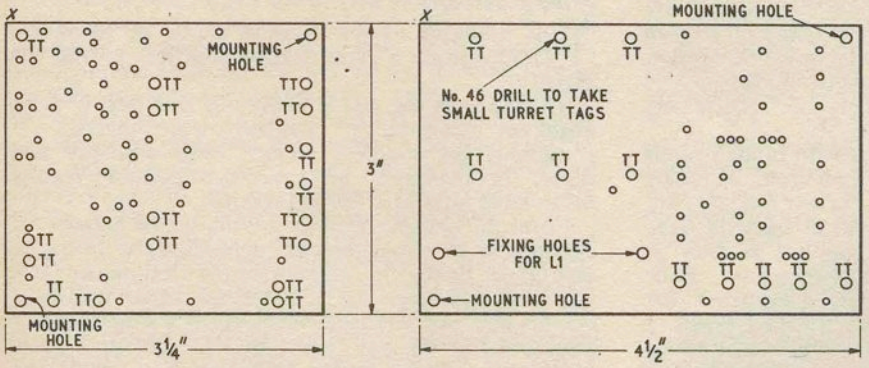


Fig. 9.6 (far left). Top and underside views of bistable relay panel

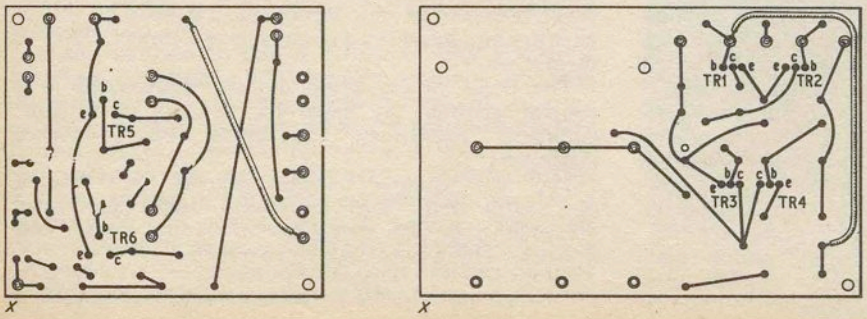


Fig. 9.7 (left). Top and underside views of product amplifier circuit panel

Insert a 0·25μF capacitor into OA4/SK11 and SK12, and switch S11 to 10Hz. A "buzz" from the relays should now be heard, which may or may not sound erratic. Transfer the d.c. voltmeter to OA4 output while the relays are still working and adjust VR2 on the bistable relay panel for zero volts; this should produce an even note from the relays. Return the voltmeter lead to the multiplier output M/SK3 and this time zero-set with VR25.

Apply an input of +5V to M/SK2; the relay "buzz" will drop in frequency, but no output should be observed at M/SK3. Transfer the +5V patching lead to M/SK1 and again no output should be seen. Finally, apply +5V to both inputs, M/SK1 and SK2, to produce a multiplier output of $5^2/10$ or 2·5V.

Throw switch S12 to change output polarity and experiment with inputs of differing sign. If all is well, the product voltage should retain its value of 2·5 for any sign combination of input voltages and S12.

For best accuracy it is advisable to go over all adjustments again to obtain optimum settings, and also verify that the multiplier will handle a full range of input voltages.

Due to the fact that the power supply may be working close to its maximum current limit, there could be some fall-off in multiplier accuracy because of switching transients, this can be checked by employing the extra current facility, S1 in Fig. 3.1. The optional −12V relay power supply should obviate the difficulty if it occurs.

To use the operational amplifier (OA4) on its own, merely switch S11 to the "off" position and patch the amplifier sockets in the normal way.

Next month: The final article in the PEAC series. This will complete the operational details of UNIT "D", and will give some examples of special circuits to represent mechanical phenomena, and some general notes.

We now consider the use of the multiplier UNIT "D" in solving equations.

THE MULTIPLIER IN EQUATION SOLVING

Fig. 10.1 sets out four multiplier configurations to show how equation terms may be handled. As a self-contained computing element, UNIT "D" will multiply input voltages X and Y to give a product $XY/10$, see Fig. 10.1a. Note that arrows are normally used with the multiplier symbol to identify input and output terminals.

Division of two variable voltages is achieved, in Fig. 10.1b, by placing the multiplier in the feedback loop of an operational amplifier. However, with division, certain limitations are imposed. The Y input must be of single polarity, which rules out a.c. waveforms unless they are d.c. biased above or below $Y = 0$, but ramp or step functions will be accepted if they do not change their sign. With the X input, voltages can be 0 to ± 10V d.c., or a.c. peak.

Because an extra filter capacitor (shown dotted in Fig. 10.1b) is needed to prevent amplification of low-level carrier ripple by the open-loop, high gain amplifier, frequency response is restricted to 10Hz for the division operation, when switch S11 is in the 50Hz position. It is sometimes possible to arrange a problem so that the reciprocal is multiplied, and thus avoid the limitations of Fig. 10.1b division. A related configuration in Fig. 10.1c gives an output $XY/(1 + X)$, for inputs of $\pm X$ and $\pm Y$.

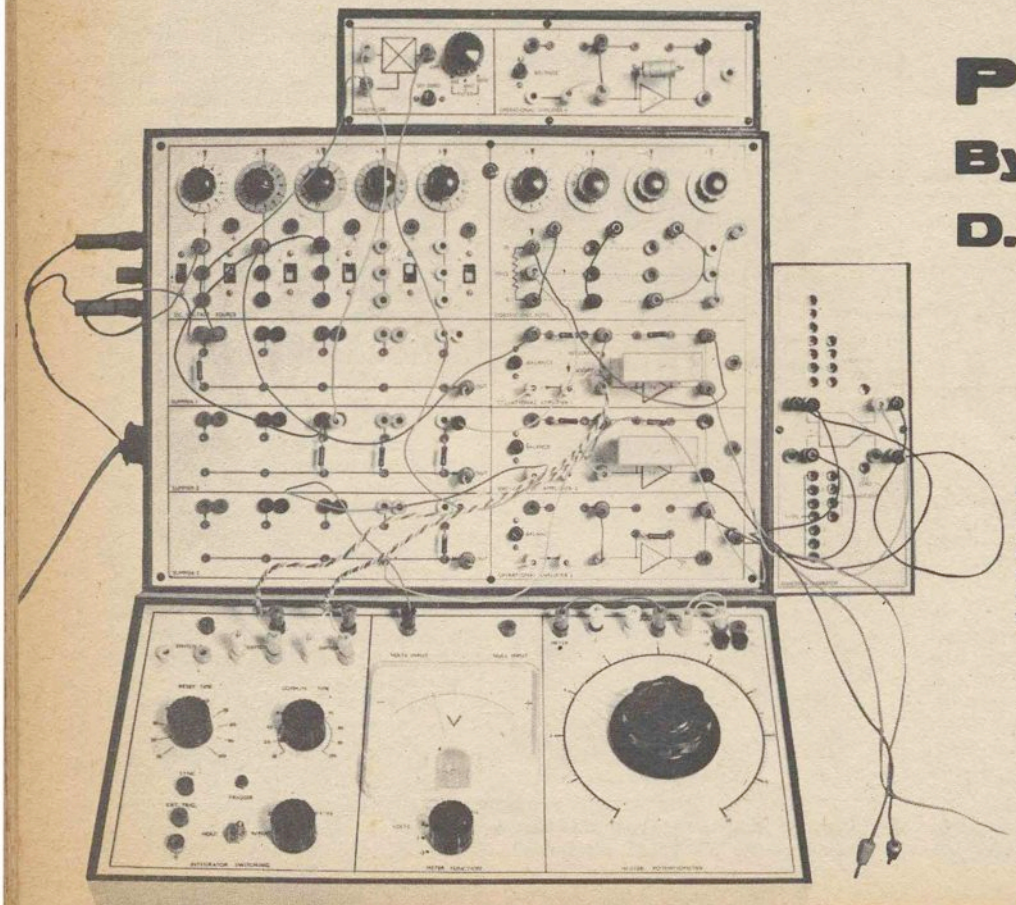
In the final example of Fig. 10.1d, the multiplier is combined with integrators, and therefore handles time varying voltages. By solving the equation $dA/dt = 2\pi R \times dR/dt$, which describes the rate at which the area of a circle changes with a growth of radius, the layout of Fig. 10.1d can be used to investigate,

ANALOGUE COMPUTER

PEAC

By

D. BOLLEN



The Practical Electronics Analogue Computer in its complete and comprehensive form. The whole of this equipment has been fully described in this series of articles which is concluded this month

say, the build-up of tape on a spool, the expansion or contraction of metal discs and cylinders when heated, or the surface area of a liquid in a conical reservoir.

SPECIAL ANALOGUE COMPUTER CIRCUITS

Apart from the analogue computing elements already covered are a few specialised diode circuits which are used for simulating various mechanical phenomena. Ordinary silicon diodes, such as the OA202, can be employed with the circuits of Fig. 10.2, and are inserted into the computing component sockets of UNIT "A".

Dead Zone. Amplifier gain in Fig. 10.2a is zero until the limits

$$E_{in} = -\frac{R1}{RB_1} \times 10$$

or

$$E_{in} = \frac{R2}{RB_2} \times 10$$

are reached, thereafter gain will depend on the slope given by R_f/R1 and R_f/R2.

Limiter. In Fig. 10.2b, amplifier gain is constant between the limits set by

$$E_o = \frac{R1}{RB_1} \times 10$$

and

$$E_o = -\frac{R2}{RB_2} \times 10$$

When the limits are exceeded, the gain falls to zero.

Friction. A frictional force generated by moving surfaces in contact is virtually constant for all values of

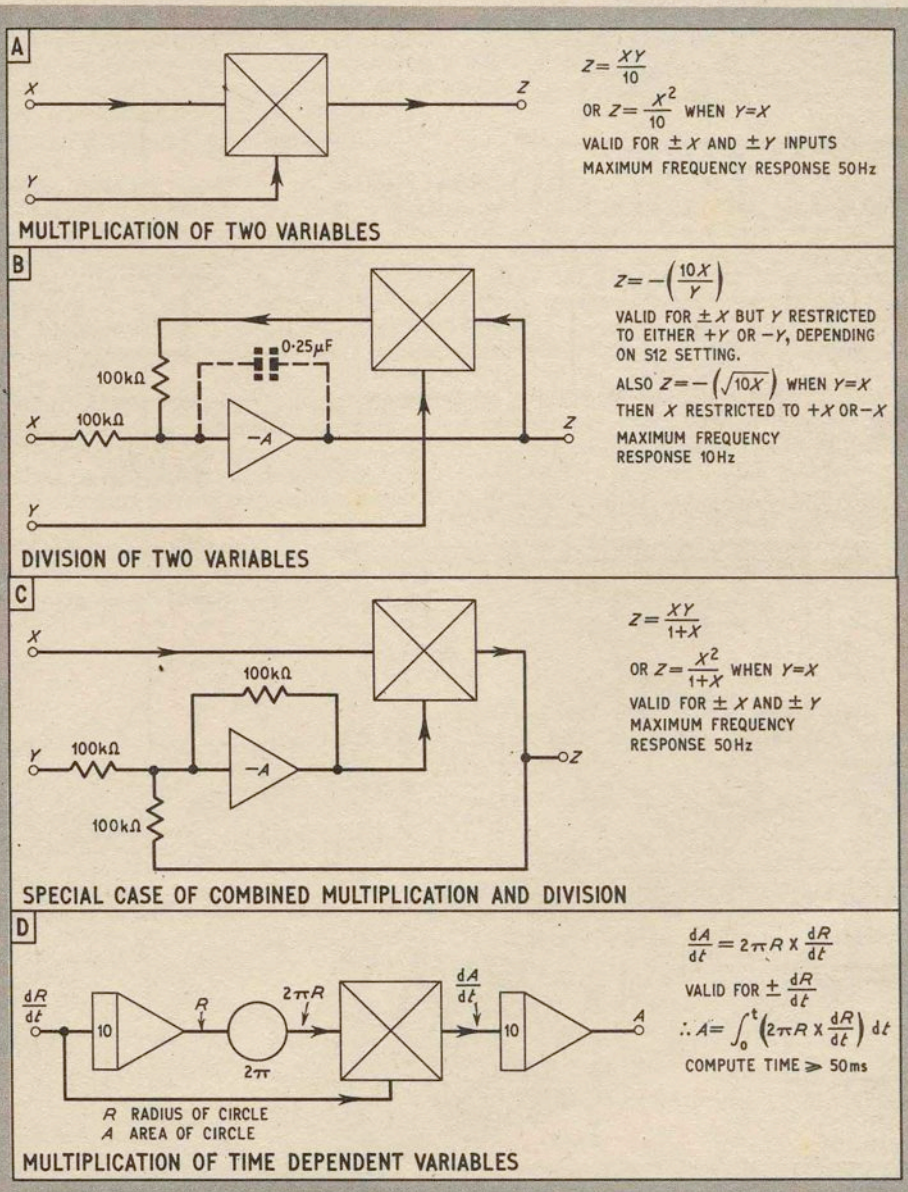


Fig. 10.1. The multiplier used for equation solving

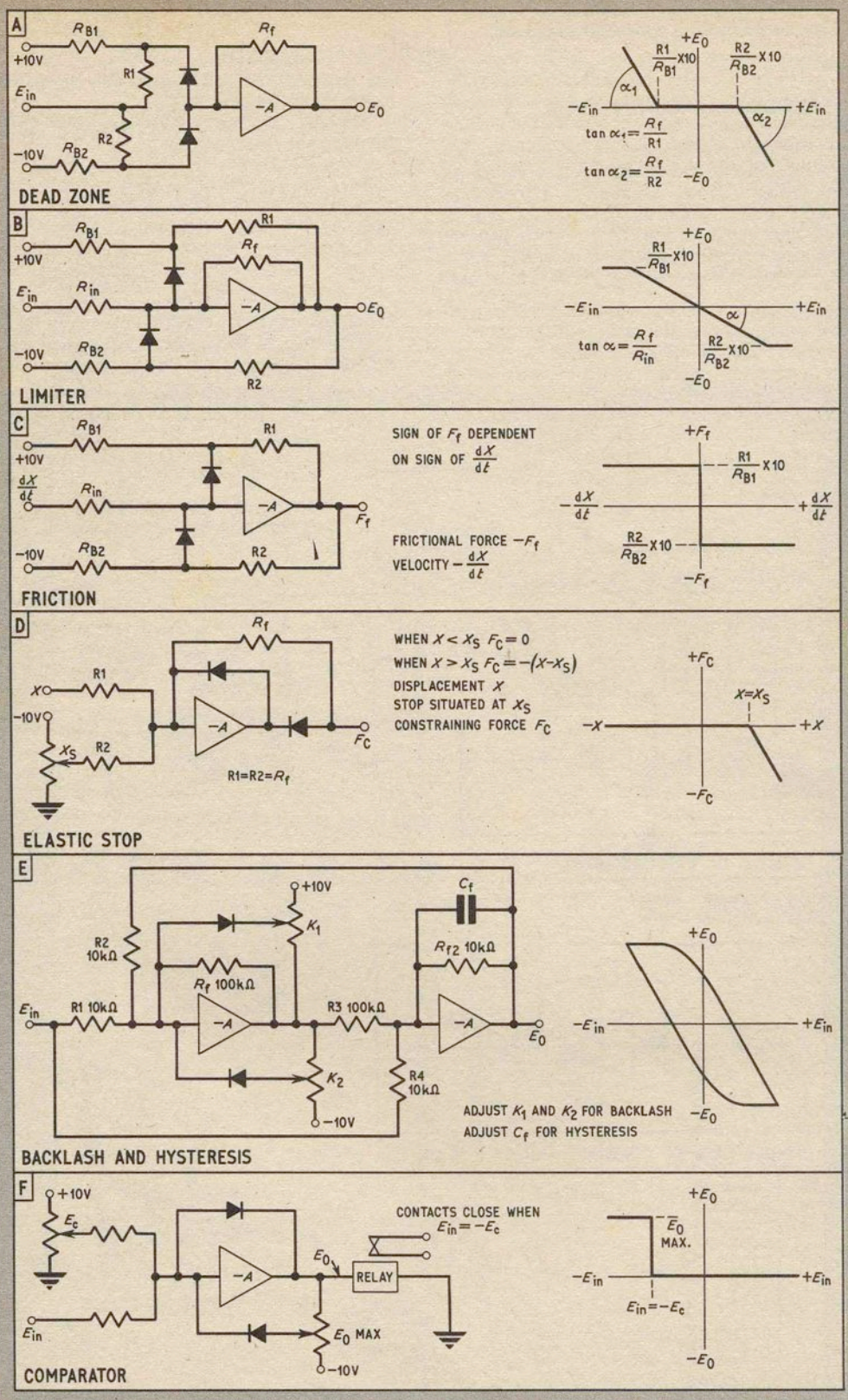


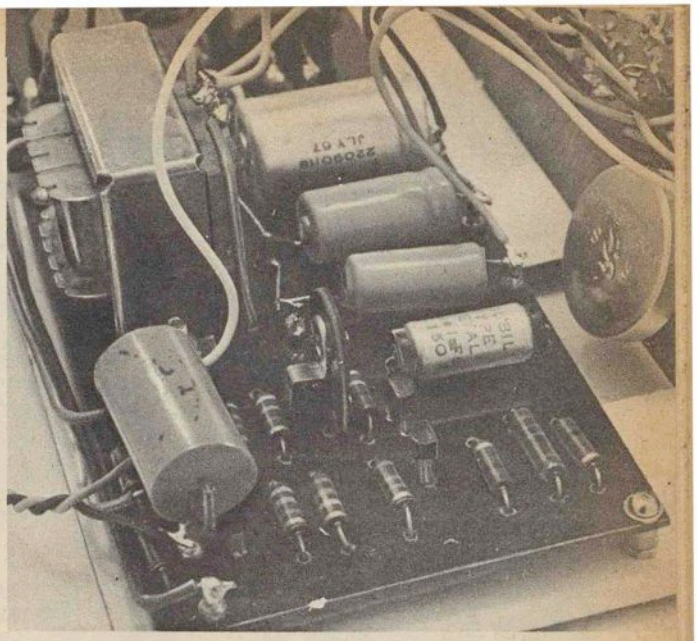
Fig. 10.2. Special circuits for simulating mechanical phenomena

velocity, but will change sign when the direction of the velocity is reversed. Circuit Fig. 10.2c satisfies the above conditions and generates a voltage proportional to a frictional force F_f.

Elastic stop. When an object makes contact with an elastic stop, the resulting constraining force is proportional to the penetration of the object into the stop. In Fig. 10.2d, term X_s represents the position of the elastic stop, while X is the displacement of the object. When $X \geqslant X_s$, the amplifier provides an output F_c which represents the constraining force.

Backlash and hysteresis. Mechanical linkages, gear trains, and some electrical circuits will often exhibit backlash and hysteresis, which are simulated by the circuit of Fig. 10.2e, using a dead zone and an integrator. Apart from K_1, K_2, and C_f, adjustments to R2, R3, and R4 will allow a wide range of characteristics.

Comparator. As its name suggests, the comparator of Fig. 10.2f compares one voltage with another, and enables some action to be taken at a pre-arranged input level. The comparator can be applied to the simulation of impact forces, where the constraining force is proportional to the *rate* of penetration; when $E_{in} = -E_c$, the relay contacts will close and insert a voltage representing velocity into an equation.



Product amplifier circuit panel

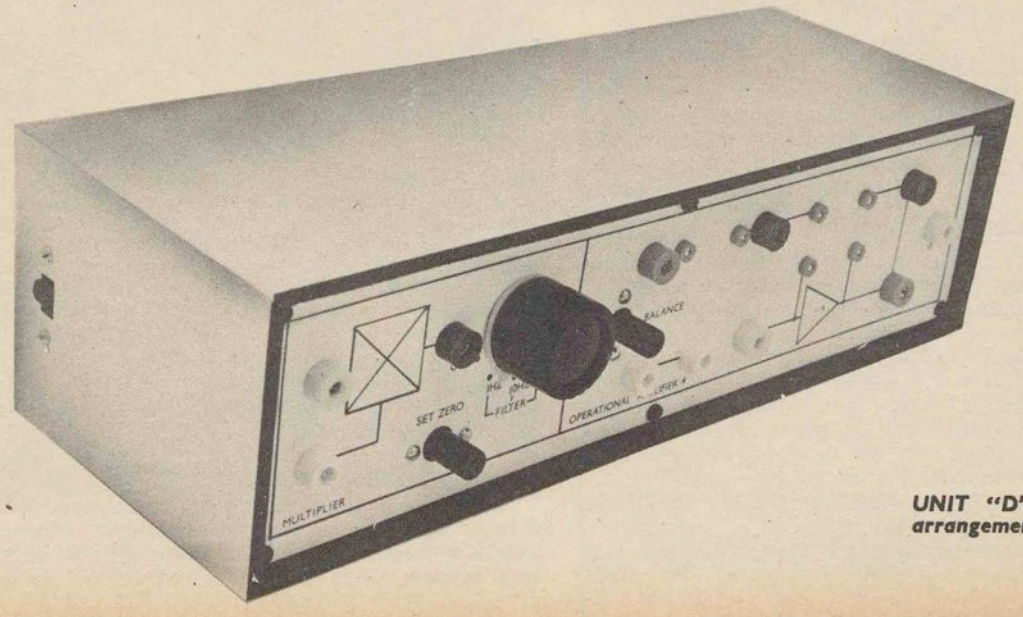
CONCLUDING NOTES

A brief mention should be made of those aspects of analogue computer usage which were considered to be beyond the scope of the present series. It would have been difficult to include the more complex Calculus problems which PEAC is capable of solving, and also transfer function techniques were avoided because they would have demanded some knowledge of Laplace transforms and the like.

A very important field is the use of analogue computers in controlling processes and evaluating data, so called "In-plant" applications, but here fairly elaborate sensing equipment and servomechanisms are called for, to act as intermediaries between the external process and the computer.

An important omission, brought to light by a reader's letter, concerns the use of a temporary feedback resistor when checking the coefficient of a potentiometer which is employed for division (Fig. 4.1f). If the feedback resistor is not present, the operational amplifier summing junction will no longer be at virtual earth when the potentiometer is disconnected for measurement purposes, and this can lead to serious errors. Therefore, when checking a division potentiometer coefficient, always insert a 10 kilohm feedback resistor into OA/SK11 and SK12.

If difficulty is experienced in zero-setting a UNIT "A" operational amplifier after construction, by adjustment of VR1 on the amplifier panel, it may be that transistor "spreads" are greater than has been allowed for in the design. The simple cure is to increase R1 (Fig. 3.7) to 4·7 megohm if the amplifier output is fixed close to the negative supply rail voltage, or, when the output remains clamped near to the positive rail, decrease R1 to 3·3 megohm. ★



UNIT "D" front panel arrangement and cabinet