808 ANALOG SIGNAL PROCESSOR

The 808 Analog Signal Processor is an analog computer that can function as a stand-alone unit or operate with external accessories to meet a variety of instrumentation and simulation applications. Features internal to the 808 are described below. The following is a list of external accessories that expand computing capabilities and operator functions.

MODEL 785 CONTROL UNIT- Combines multiple 808 units into a single operating system. Includes a 3 1/2 digit digital voltmeter and central address for setting attenuators and readout of amplifier outputs. Includes a push button slow time and repetitive operation mode control to operate combined 808's as a general purpose analog simulation system. Rack mountable in a full width, 3 1/2" high panel space.

MODEL 731 ATTENUATOR GROUP- Adds seven attenuators each having a push button coefficient setting switch. Rack mountable in a half width, 3 1/2" high panel space.

MODEL 709 VDFG- An eleven segment, variable slope, variable breakpoint diode function generator. Rack mountable in a half width, 3 1/2" high panel space.

MODEL 717 THREE MODE CONTROLLER- Provides the proportional, rate and reset control function for simulation and on-line applications. Rack mountable in a half width, 3 1/2" high panel space.

BANANA PLUG MODULES- A variety of switch and non-linear functions are available. Modules plug directly into the 808 patch panel jacks.

DESCRIPTION OF 808 INTERNAL FEATURES

1.0 AMP/POT ADDRESS

The Amp/Pot Address switch is an 11 position, 2 pole rotary switch. One section selects amplifier outputs for external readout; the other section selects coefficient potentiometer outputs for setting attenuator constants. The amplifier selector wiper is connected to the Amplifier Readout Bus; the potentiometer selector is connected to the Potentiometer Readout Bus.

1.1 MODE SELECTOR

The Mode Selector switch is a 2 position, 12 pole rotary switch. It provides a number of functions that distinguish the computer's Pot Set and Operate modes.

1.1.1 Setting of Coefficient Potentiometers

The top end input to each coefficient potentiometer is connected to one of six poles. In the OPR position the poles are switched to the patch panel input; in the POT SET position the poles are switched to positive reference. Thus in the Pot Set mode the inputs to all potentiometers are replaced by positive reference and the potentiometer output values are measurements of voltage divider ratios.

1.1.2 Integrator Mode Control

One pole is connected to the Mode Control switch pole. In the POT SET position the pole is switched to ground; in the OPR position the pole is switched to the OP patch panel jacks. Thus in the Pot Set mode all integrators are placed into an initial condition; in the Operate mode integrators are controlled by the OP mode control logic.

1.1.3 External Readout Meter

One pole is connected to the Readout Meter Bus. In the POT SET position the pole is switched to the Potentiometer Readout Bus; in the OPR position the pole is switched to the Amplifier Readout Bus.

1.1.4 Hold Inhibit

In the normal integrator initial condition mode the hold switch is shut off, thereby isolating the input resistor network. It is necessary, however, to set potentiometers with their resistor loads connected. Therefore, during the Pot Set mode each integrator hold switch is inhibited; it is held in an "on" condition and the resistor network summing junction is ground potential. A separate hold inhibit logic circuit is found on the quad amplifier assembly. A positive logic input enables the hold switch to operate normally; a negative input inhibits the switch. Thus one pole of the Mode Selector switch is connected to the Hold Inhibit Bus. In the POT SET position the pole is connected to negative 10 volts; In the OPR the pole is switched to positive reference.

1.2 MODE CONTROL

The Mode Control switch is a single pole, double throw, center off toggle switch that produces logic levels to operate the 808 integrator mode switches. When the Mode Selector switch is in the OPR position the pole is connected to the patch panel OP Bus. The OP Bus has three states. Ground or a positive voltage places integrators into the Initial Condition mode. A -5 or more negative voltage places integrators into the Operate mode. A voltage level between -1.5 and -3.5 volts places integrators into the Hold mode.

In the "IC" position the pole is switched to ground. In the "OP" position the pole is switched to the Mode Control Bus. (The bus is pulled to the Operate mode level by a 22K resistor connected to -10 volts. For external mode control the Mode Control switch is placed into the "OP" position and the Mode Control Bus is pulled to ground and/or the Hold mode level.) In the "HD" position the Mode Control Bus is pulled to the Hold mode level through a 1K resistor that is connected from the pole to ground.

1.3 COEFFICIENT POTENTIOMETERS

The coefficient potentiometers are ten turn, 5K ohm variable resistors arranged as attenuators with their bottom ends grounded. Procedures for setting coefficients are listed as follows:

1. Coefficients are set after all patching is completed.
2. Position the Mode Selector switch to POT SET.
3. Position the Amp/Pot Address switch to the number of the potentiometer to be set.
4. Connect a digital voltmeter to the Readout Meter Bus found in the rear Trunk and Readout connector.
5. Adjust the potentiometer until the desired setting is observed.

1.4 OVERLOAD INDICATOR

The "OVLD" lamp is a light alarm that indicates when one or more of the eight patch panel amplifier outputs exceed either positive or negative 10 volts reference.

1.5 POWER

Power is on when the POWER toggle switch is in the up position.

1.6 PATCH PANEL

Patch panel operations are described in a separate patching section.

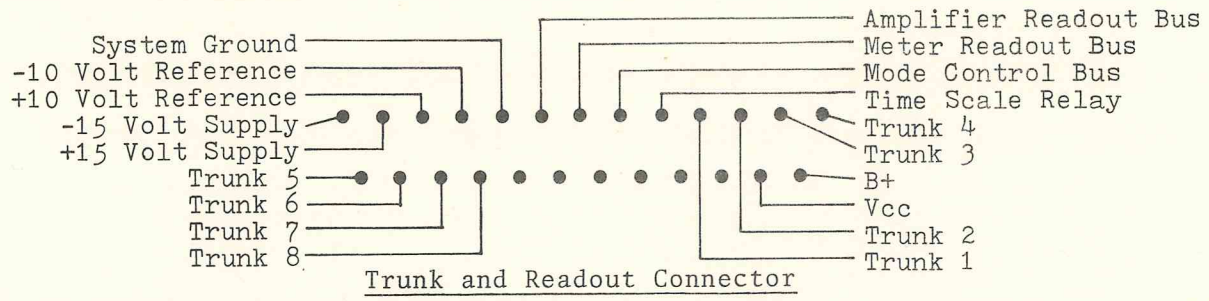
1.7 TRUNK AND READOUT CONNECTOR

A twenty-five pin rack and panel connector found at the rear on the 808 unit provides convenient input/output connections. The following is a description of pin connections. (Numbers are left to right, top to bottom facing the unit's rear.)

No.	Description	No.	Description
1.	Trunk 4 (patch panel jack)	14.	B+ Neon display power (160 volts) *
2.	Trunk 3 (patch panel jack)	15.	Vcc Logic power (+5 volts) *
3.	Trunk 2 (patch panel jack)	16.	NC
4.	Trunk 1 (patch panel jack)	17.	NC
5.	Time Scale Relay #	18.	NC
6.	Mode Control Bus, see para. 1.2	19.	NC
7.	Meter Readout Bus, see para. 1.1.3	20.	NC
8.	Amplifier Readout Bus, see para 1.0	21.	NC
9.	System Ground	22.	Trunk 8 (patch panel jack)
10.	-10 Volts Reference	23.	Trunk 7 (patch panel jack)
11.	+10 Volts Reference	24.	Trunk 6 (patch panel jack)
12.	-15 Volts	25.	Trunk 5 (patch panel jack)
13.	+15 Volts		

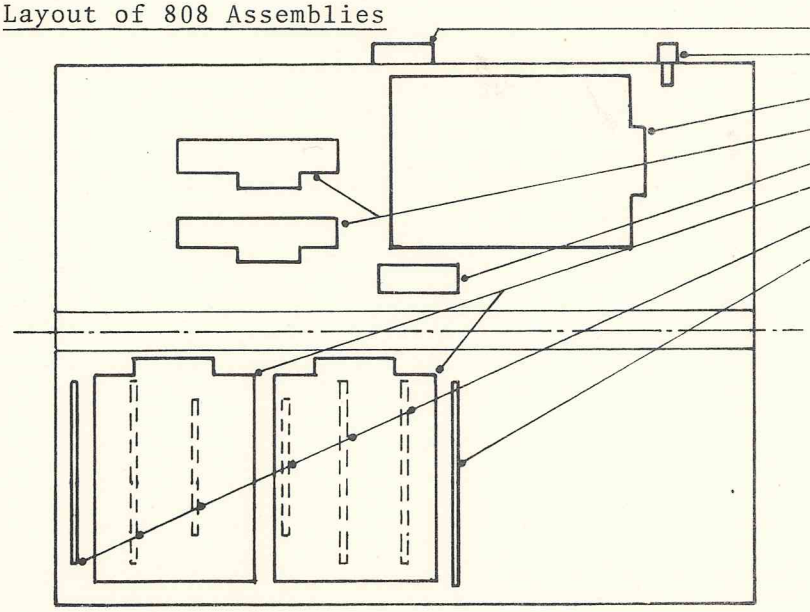
* Included only when a Comdyna digital voltmeter is supplied.
\# When the quad amplifier boards have the time scale relay provision, -15 volts connected to the Time Scale Relay termination will energize the relay. In the energized state integrators are in a slow time condition; in the de-energized state integrators are in a high speed condition.

808 SYSTEM SCHEMATIC



Trunk and Readout Connector

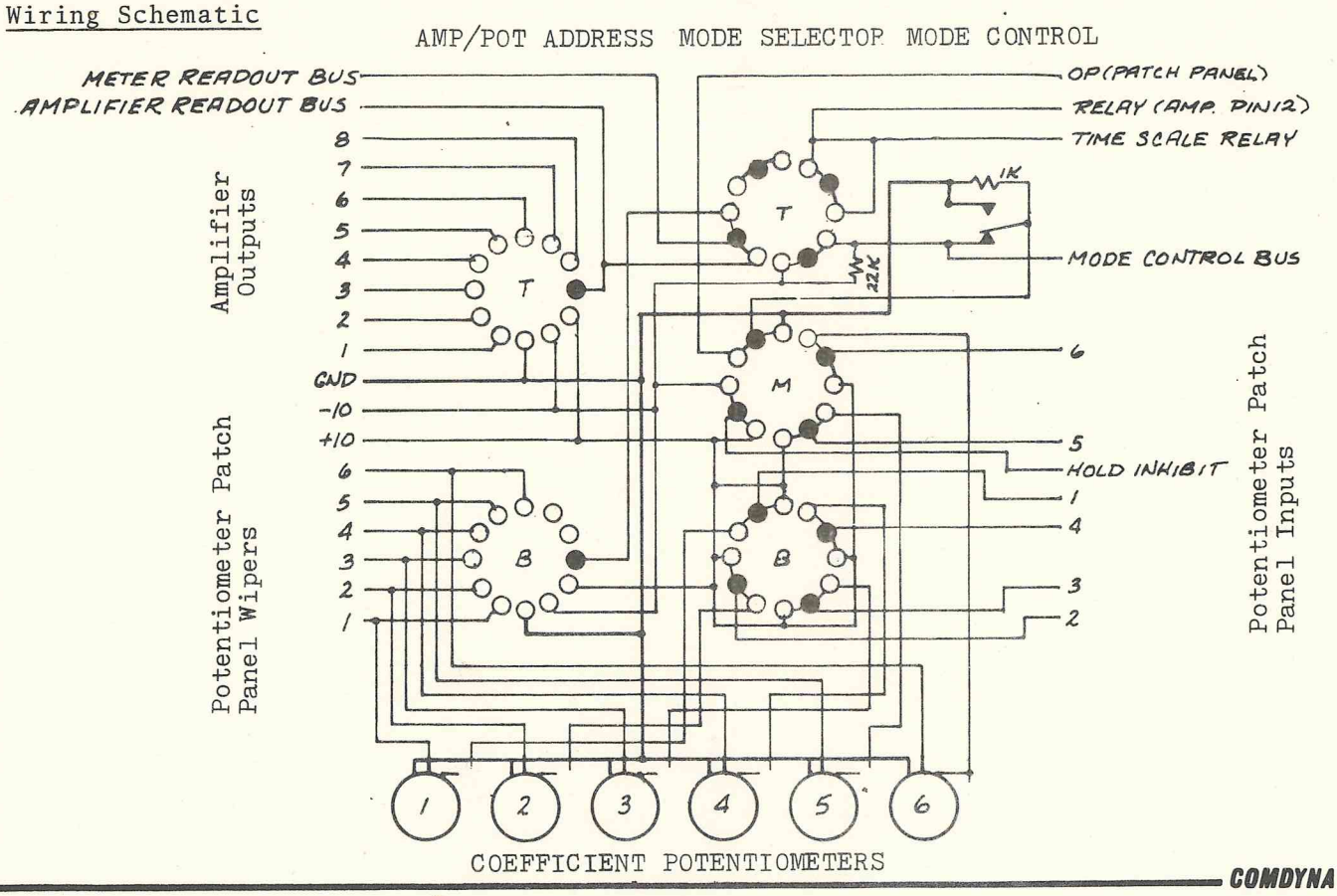
Layout of 808 Assemblies



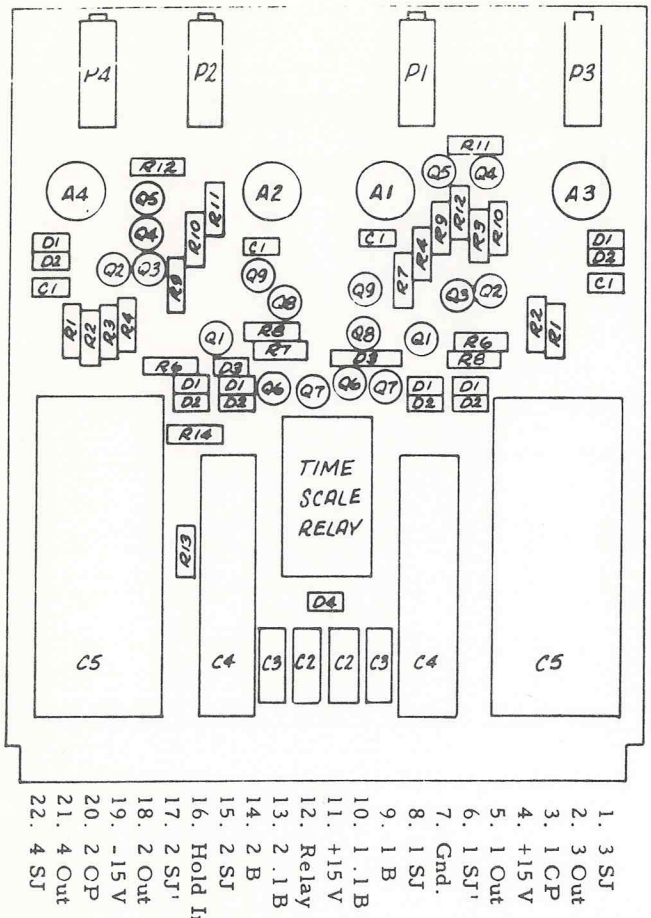
Input summing resistors for integrator and summer amplifiers are located on the Resistor Network Boards. Resistors are 5.00K and 50.0K ohms, metal film, 0.1%.

Color coding of power wiring is:
+15V -Red; -15V -White;
-10V -Yellow; +10V -Orange;
Ground -Black.

Wiring Schematic



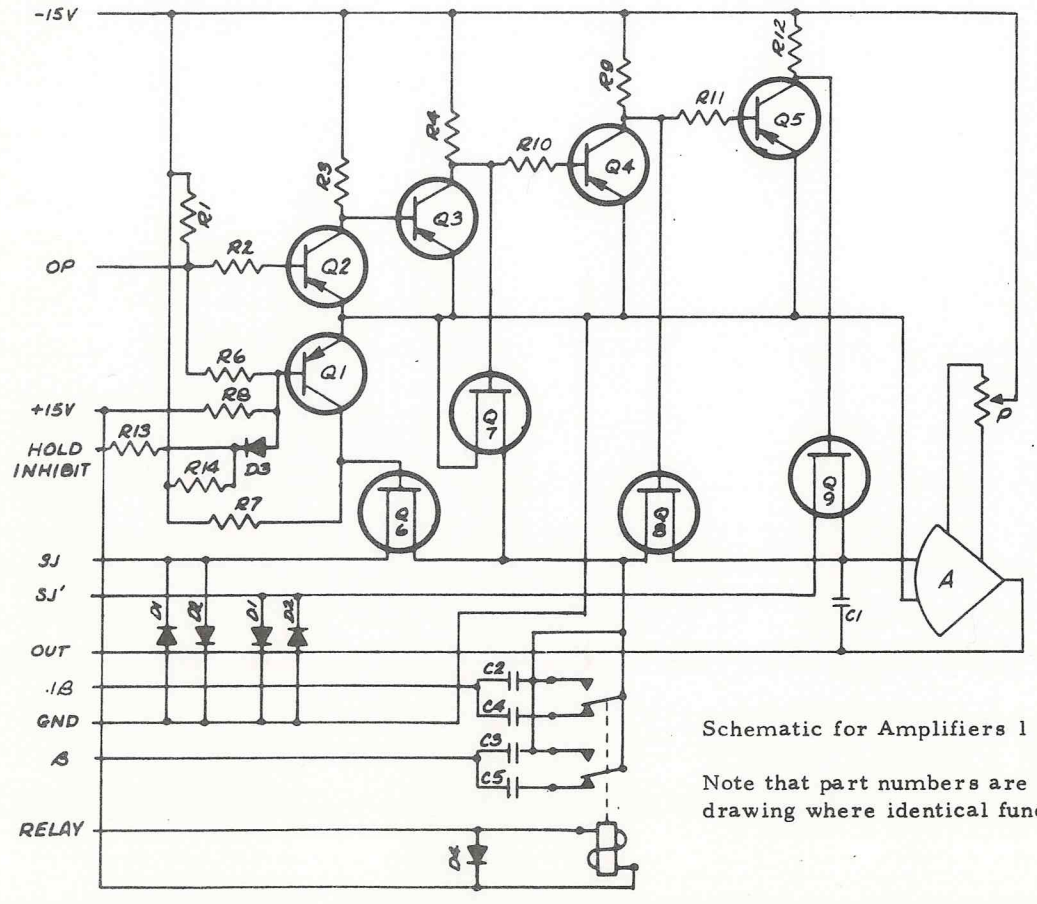
Assembly Drawing



Dwg. 911-1, QUAD AMPLIFIER ASSEMBLY

The 911 board provides four single ended, high gain operational amplifiers. Amplifiers 1 & 2 have electronic switch circuits. Ground or plus voltage at the OP input closes the SJ' summing junction (Q9 and shunt Q7) and opens the SJ summing junction (Q8.) A -5 volt or less input or absence of an input closes the SJ and opens the SJ' summing junction. Amplifiers 1 & 2 may include up to four integrating capacitors which are connected to the SJ summing junction. For integrator operation, either the B or .1 B input is externally connected to the amplifier output. The time scale relay, when energized, parallels capacitors C2 and C3 with C4 and C5. A hold mode switch (Q6) shuts off the SJ input with -2 to -3 volts at the OP input. The capacitor remains as the feedback. The hold switch may be held closed with a negative voltage at the Hold Inhibit input. Such a condition is required when setting coefficient potentiometers.

Amplifiers may be balanced as summers. With a zero input, adjust the balance potentiometer (P1 - P4) until a zero output is observed. Amplifiers 1 & 2 may be balanced as integrators. With a zero input, adjust the balance potentiometer until a zero integration rate is observed.



Schematic for Amplifiers 1 & 2

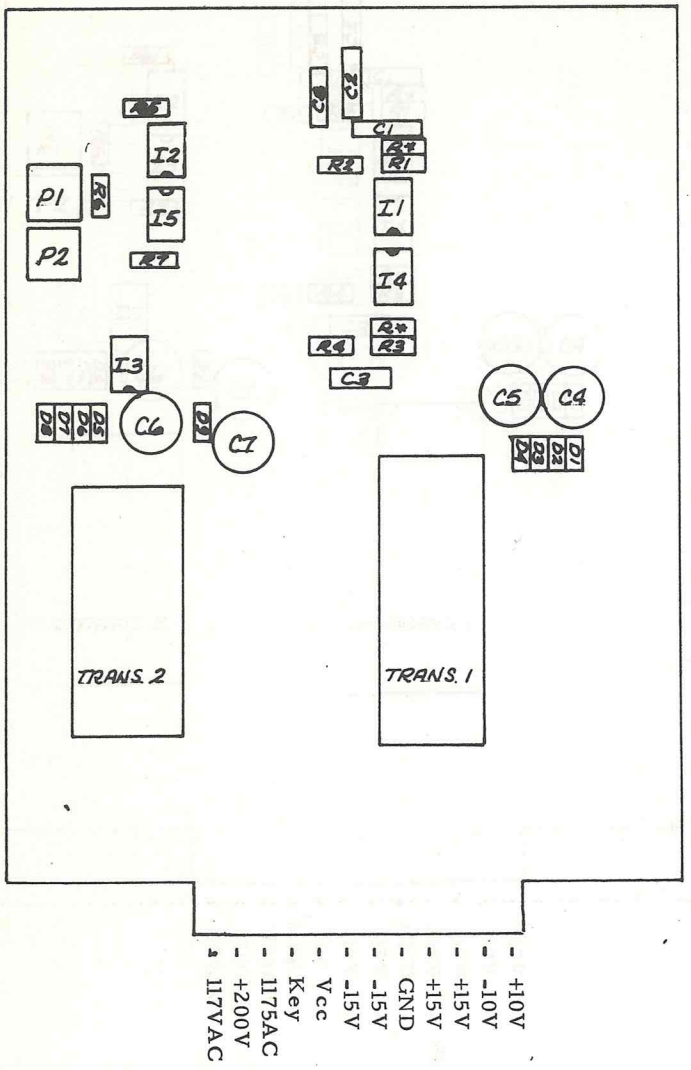
Note that part numbers are repeated in the assembly drawing where identical functions or circuits occur.

Parts List

R1	27K
R2-R4, R9-R12, R7	15K
R6	47K
R8	330K
R13	2.2K
R14	27K
C1	15 uuf
C2	.005 uf*
C3	.05 uf*
C4	2 uf*
C5	20 uf*
Q1-Q5	2N5138
Q6-Q9	2N5163
P1-P4	10K
A1 & A2	1421
A3 & A4	741
Relay	4A, 24V

*Precision integrating capacitors

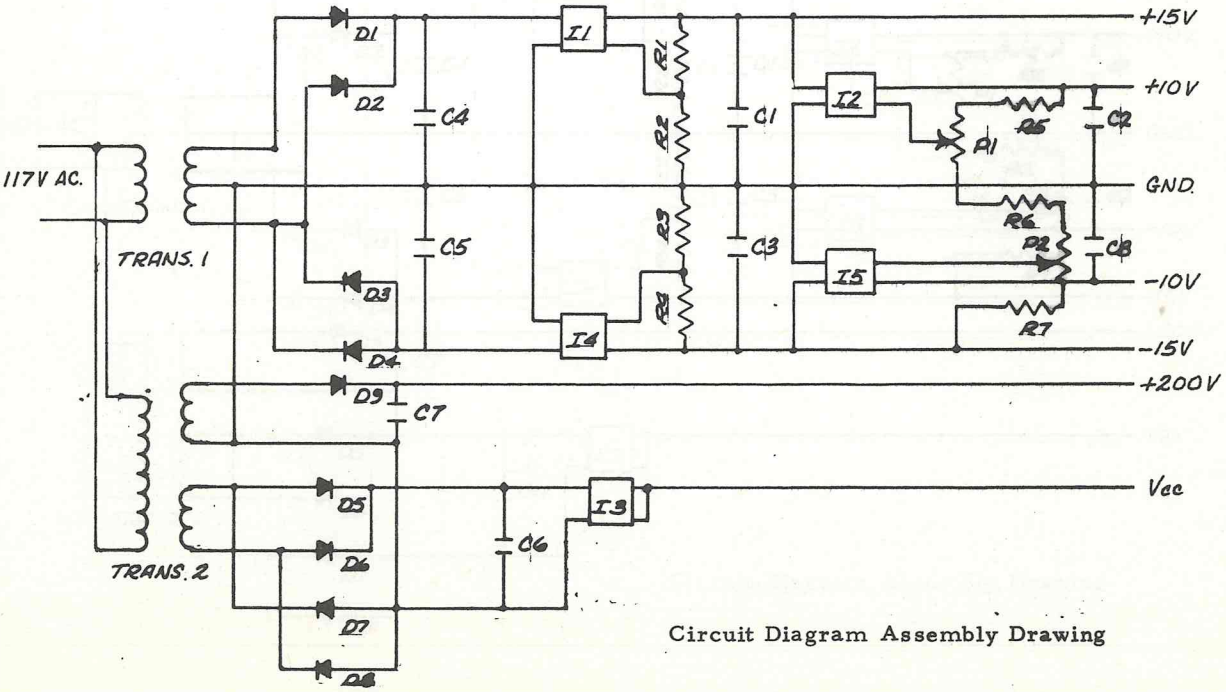
DWG 116-2 POWER SUPPLY



The 116-2 Power Supply uses the 78MGT/79MGT programmable regulators to generate +15, -15, +10, -10 and +5 volts. The +200 V neon display drive is unregulated. The +15/-15 volt outputs are fixed within a range of 14.75 to 15.25 volts. The +10/-10 are arranged in a tracking configuration with adjustments for the absolute value and tracking error. Potentiometer P2 adjusts the absolute value of -10 volts. P1 adjusts +10 to track -10.

Parts List

R1, R3	12K
R2	4.7K
R4	2.2K
R5	4.99K
R6	6.98K
R7	7.05K
R*	Trimming Resistors
C1, C2	.1 uf
C3, C8	.47 uf
C4, C5, C6	500 uf
C7	12 uf, 250V
D1 thru D8	IN4001
D9	IN4007
P1	50 ohm
P2	500 ohm
I1, I2, I3	78 MGT
I4, I5	79 MGT
TRANS 1	28V CT/300 Ma
TRANS 2	125V/15Ma, 6.3V/600Ma



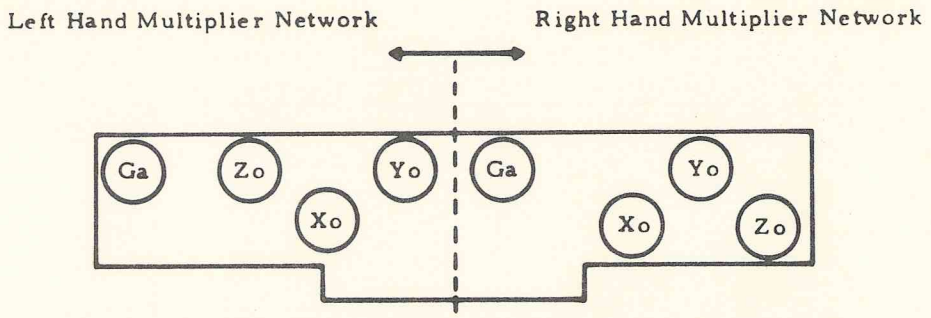
Circuit Diagram Assembly Drawing

C. 2-B MODEL 982 DUAL MULTIPLIER ADJUSTMENT (For Serial Nos. 114-)

For GP-6 computers of serial numbers greater than 114, the Model 982 Dual Multiplier Network is located directly under the Amplifier Mother Board on the back side of the patch panel. A layout of the 982 assembly is shown in Fig. C. 2-B-1.

The 982 network is originally adjusted at the factory. It should, however, be checked and readjusted, if necessary, during the computer's initial checkout. Thereafter, the network should be periodically checked to assure its most accurate operation. About 10 - 20 minutes should be allowed for warm-up before adjusting or checking.

Figure C. 2-B-1



Adjustment consists of zero offset balancing and a trim for gain and linearity. The suggested procedure for adjustment is as follows:

1. With the patch panel terminations X and Y patched to ground, adjust potentiometer Zo (shown in Fig. C. 2-B-1) for a zero output.

2. Program an integrator to sweep from minus to plus reference. For convenience, place the GP-6 into the repetitive operation mode. Display the ramp vs. the multiplier output. Patch the ramp to the Y input; the X input should remain patched to ground. Adjust the Xo potentiometer until a best zero curve is obtained.

3. Reverse the X and Y input connections. Adjust the potentiometer Yo until a best zero curve is obtained.

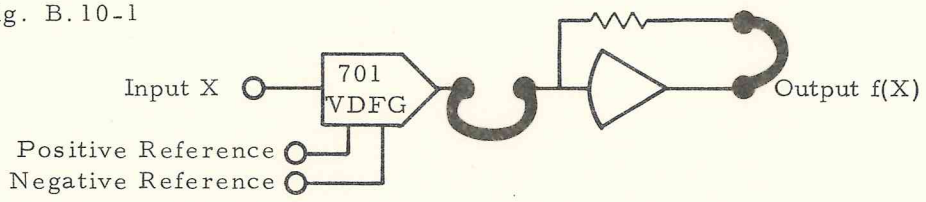
4. Readjust Zo, if necessary.

5. Patch Reference to the X input and the ramp to the Y input. Sum the multiplier output with the correct polarity of the ramp so that an error curve is obtained. Adjust the potentiometer Ga until the best error curve is obtained. Reverse the X and Y inputs and check the error curve. Check the error curve with the opposite reference under both combinations of inputs. Trim potentiometer Ga so that the best error curve for all four combinations is obtained.

B.10 THE MODEL 701 VARIABLE DIODE FUNCTION GENERATOR

The Model 701 VDFG is programmed as an input network. For operation, it must be connected to the summing junction of an operational amplifier. When the feedback of this amplifier is a resistor, such as shown in Fig. B.10-1, the VDFG function appears as its output. For a detailed discussion of diode function generation, see Chapter 12 of the "GP-6 Analog Simulation and Computation Programming Manual".

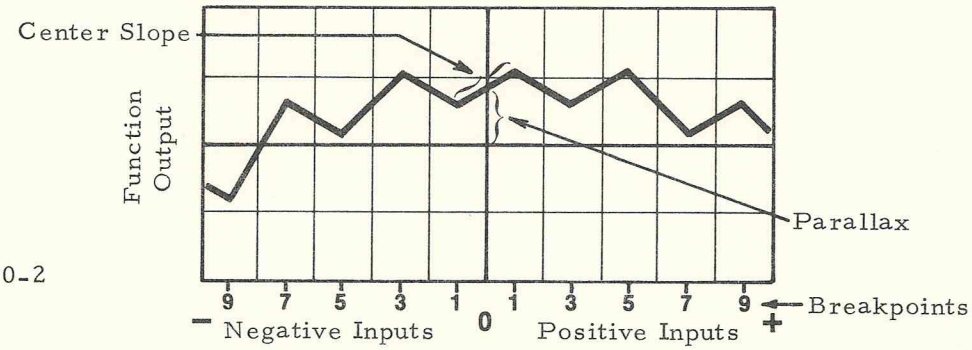
Fig. B.10-1



The following procedures may be used for setting functions:

1. Construct an output/input plot of the function to be set. The curve should be drawn on graph paper with full scale co-ordinates relating to computer reference.
2. Connect computer reference to the "+" and "-" jacks found on the VDFG panel.
3. Connect the VDFG to the summing junction as shown in Fig. B.10-1.
4. Connect a ramp that sweeps from negative reference to positive reference as the VDFG input. (The GP-6 computer time base may be used as this input ramp.)
5. Set up of the VDFG is easiest when the computer is in the repetitive operation mode and the function is displayed on an oscilloscope. Setting in the slow time mode may be desired, however, because of the increased accuracy offered by an XY plotter readout. In either case, display the VDFG amplifier output as a function of the input. The eleven segments will be presented in a manner similar to that shown in Fig. B.10-2.

Fig. B.10-2



6. To set a function, first vary the "Parallax" adjustment until the function intersects the Y axis at the desired position.
7. Next, set the "Slope" adjustment to the desired center slope. The center slope extends from -1 volt to + 1 volt input.
8. Adjust individual slopes until the desired function is displayed. Individual breakpoint slope adjustments should be set in a numeric sequence from the origin.
9. Replace the ramp with the desired program input.

It is noted that an overload condition of the output amplifier will affect set up. If this amplifier overloads during a repetitive operation set up, it will be necessary to readjust the function when the overload condition is removed.

The output amplifier feedback resistor controls the gain of function adjustments. The range of individual slopes may be increased by raising the resistor value. Slopes may also be increased by placing a co-efficient potentiometer in series with the amplifier output and the feedback resistor. In this case, adjustment gains are increased by the reciprocal of the potentiometer setting.