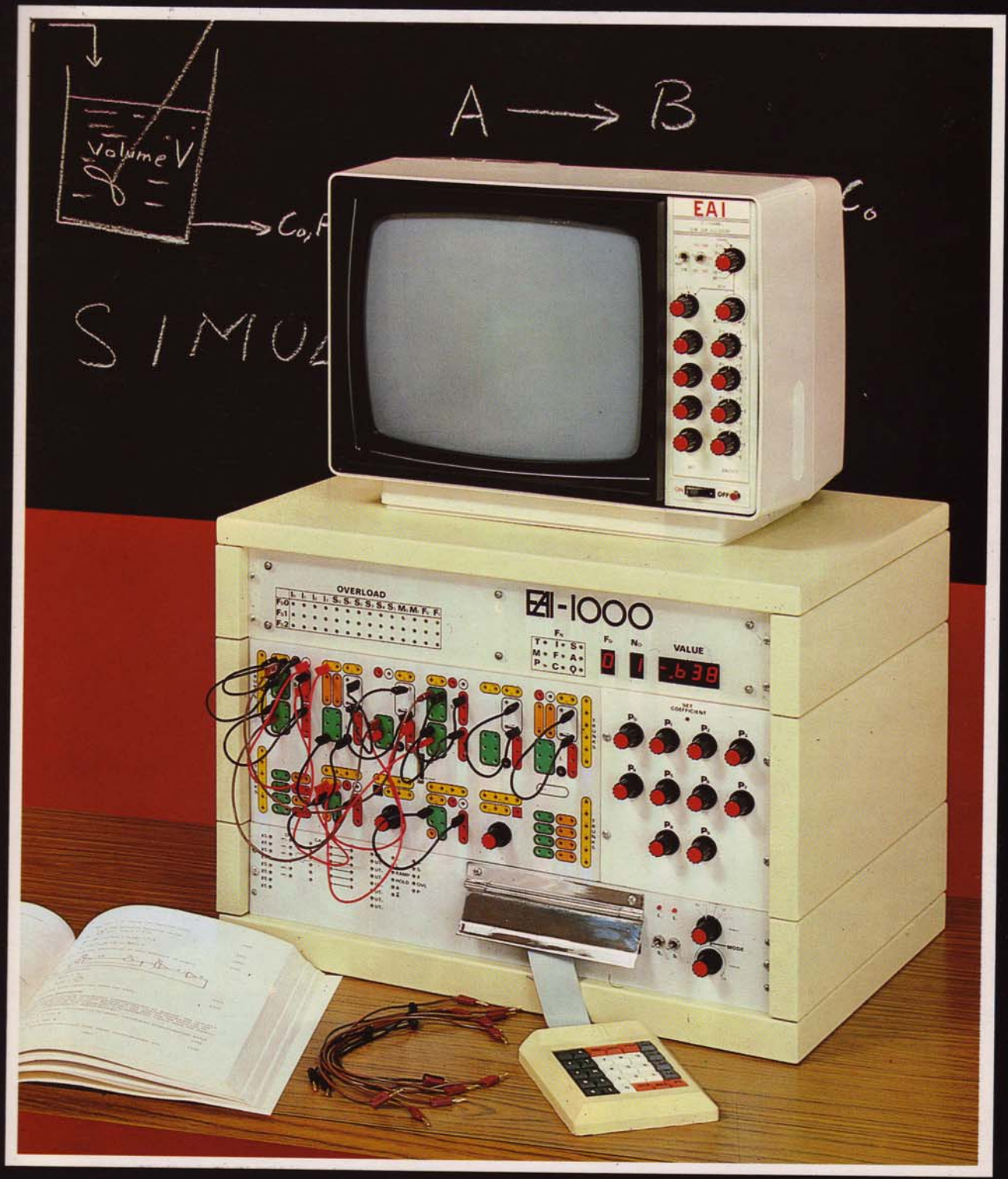
EAI-1000

Micro Processor Controlled ANALOG HYBRID COMPUTER SYSTEMS



REFERENCE AND MAINTENANCE MANUAL

EAI-Electronic Associates Pty. Limited
48 Atchison Street, St. Leonards, N.S.W., Australia 2065
Telephone: 439 7522 • Telex: 21130 • Cables: 'Paceaus' Sydney
P.O. Box 170, Crows Nest 2065

E A I

EDUCATION SYSTEMS

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REFERENCE MANUAL ONLY

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Melbourne Office: Suite 1, 182 Albert Road, South Melbourne, Vic. 3205 • Telephone: 699 7100

NOTICE

When ordering or enquiring about spare parts and replacement units for your EAI-1000 Computer, we request that you use the following procedure.

1. Supply the Drawing Number and Circuit Reference which is listed in the parts listing at the back of this manual and the model and serial number of the computer. Without this information we cannot process your request.

2. If the item is a mechanical part or assembly which does not have the above reference, please supply a full description and the model and serial number of the computer.
   If possible, include the purchase order or the EAI project number under which the equipment was originally purchased.

Your co-operation in supplying the required information will speed the processing of your requests and aid in assuring that the correct items are supplied.

It is the policy of EAI-Electronic Associates to supply equipment patterned as closely as possible to the requirements of the individual customer. This is accomplished, without incurring the prohibitive costs of custom design, by substituting new components, modifying standard components, etc., wherever necessary to expedite conformance with requirements. As a result, this instruction manual, which has been written to cover standard equipment, may not entirely cover modified equipment. It is felt, however, that a technically qualified person will find the manual a fully adequate guide in understanding, operating, and maintaining the equipment supplied.

EAI-Electronic Associates Pty. Limited reserves the right to make changes in design, or to make additions to or improvements in its product without imposing any obligation upon itself to install them on products previously manufactured.

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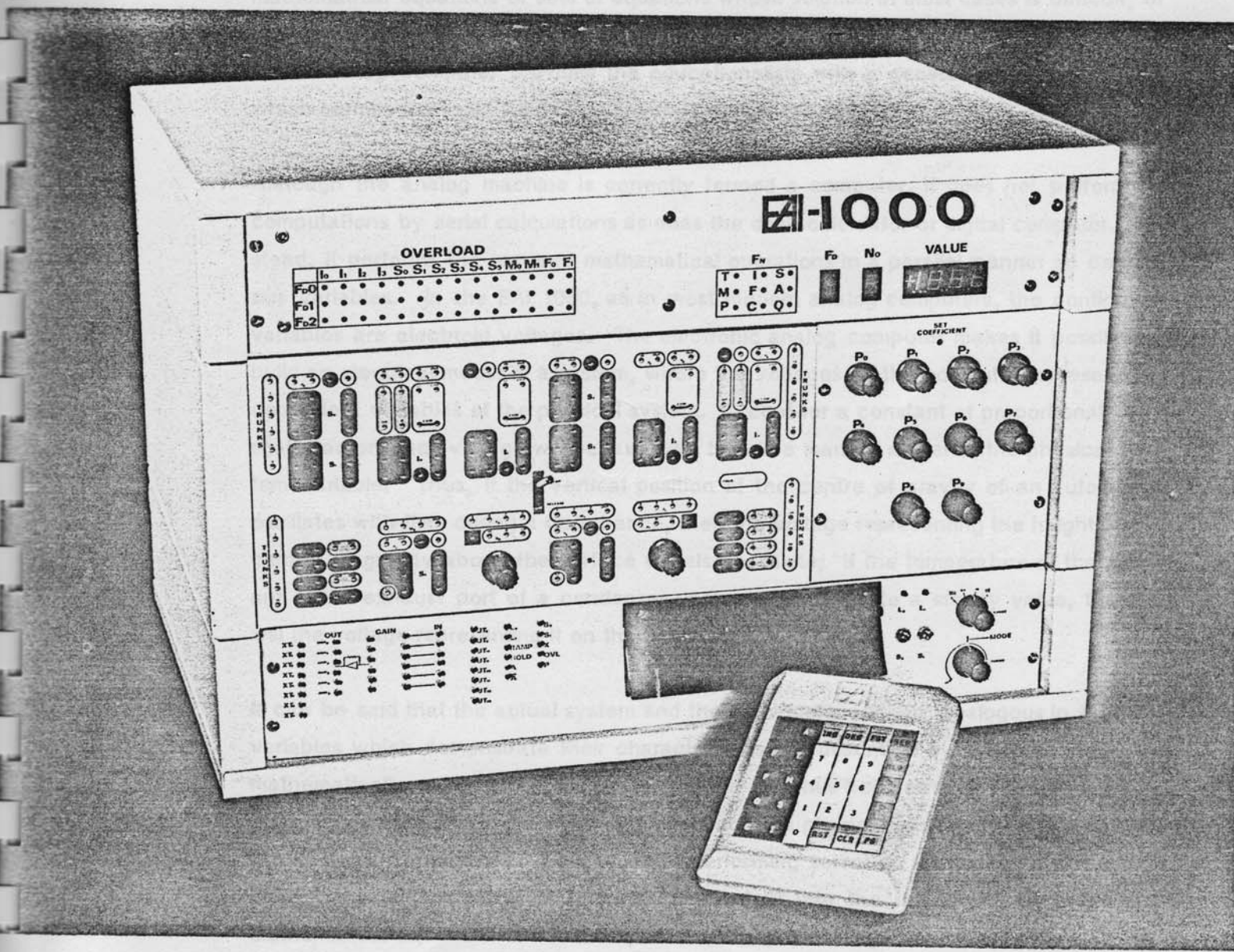


FIGURE 1

EAI - 1000 ANALOG COMPUTER

CHAPTER 1

1.1 INTRODUCTION

Many problems encountered in scientific, engineering and educational work involve mathematical equations or sets of equations whose solution in most cases is difficult, or practically impossible to obtain by the classical approach to equation solution. The EAI 1000 Analog Computer provides the educationalists with a general purpose computer which permits the rapid solution of linear or non-linear equations.

Although the analog machine is correctly termed a computer, it does not perform its computations by serial calculations as does the desk calculator or digital computer. Instead, it performs the required mathematical operations in a parallel manner on continous variables. In the EAI 1000, as in most modern analog computers, the continuous variables are electrical voltages. The electronic analog computer makes it possible to build an electrical model of a system, where the voltages on the computer represent the dependent variables of the physical system. Except for a constant of proportionality, or scale factor, each voltage will behave with time in a manner similar to the physical system variable. Thus, if the vertical position of the centre of gravity of an automobile oscillates with time during a disturbance, then the voltage representing the height of the centre of gravity above the surface will also oscillate; if the temperature of the coolant at the exhaust port of a condenser rises exponentially to a steady value, then so will the voltage representing it on the computer.

It can be said that the actual system and the electrical model are analogous in that the variables which demonstrate their characteristics are described by relations which are mathematically equivalent. The actual system has thus been simulated because of the similarity of operation of the electrical model and the physical system. This capability of the analog computer is of great value in performing scientific research of engineering design calculations because it permits an insight into the relationship between the mathematical equations and the response of the physical system. Once the electrical model is completed, well-controlled experiments can be performed quickly, inexpensively, and with great flexibility to predict the behaviour of the primary physical system.

Although the analog computer utilizes electronic components in its operation, it is not essential that the user has an extensive knowledge of electrical circuits. The EAI 1000 is basically a set of mathematical operations on direct voltages and capable of being easily interconnected. By appropriately interconnecting these building blocks, an electrical model is produced in which the voltages at the outputs of the blocks obey the relations given in the mathematical description of a physical problem.

Since the area of interest is frequently in the dynamic behaviour of physical systems, the mathematical equations are usually differential equations having time as the independent variable. In order to solve such equations, the standard components of the computer must perform the following operations; inversion, algebraic summation, integration with respect to time, multiplication and division, and function generation.

The sequence of steps for constructing a dynamic model on an analog computer requires first a mathematical description of the physical system, usually in equation form. From this description, the operator derives the information necessary to set up a computer program for interconnecting the computing components and determines the required initial conditions and forcing functions. The computing components are interconnected with wires called patch cords. The input and output terminations of the computing components are brought out to a patch panel. The physical system is simulated or modelled on the computer by interconnecting the various computing element patch points on the removable patch panel to correspond with the patching diagram. The patch panel is then fitted to the computer and the initial problem parameters are set by adjusting the coefficient potentiometers to their appropriate values.

Once the computing elements have been programmed, adjusted, and energised, the computer is switched into the operate mode. The voltages on the computer change with time in accordance with the equations that govern the physical sys tem variables. The behaviour of the computer model is viewed through an output device such as an X-Y plotter, oscilloscope, strip-chart recorder, or digital voltmeter.

This EAI 1000 Operator's Reference and Maintenance Handbook has been prepared to serve as a working guide to the analog programmer or computer operator. The information contained presupposes a knowledge of the analog computer, its basic principles of operation, and programming procedures. (Instructional information in these areas can be obtained from "Basics of Analog Computer Programming" and Seminar Handbooks by the EAI Education and Training Group). Readers interested in more detailed circuit information are referred to the Maintenance section of the manual.

1.2 GENERAL DESCRIPTION

The EAI 1000 (Figure 1) is a microprocessor controlled general purpose analog computer composed of solid-state computing components. The EAI 1000 is compact in size and is able to operate with stability and precision in a normal office or classroom environment. Reliable, with simplicity in functional design, the EAI 1000 is easy to use and can be a powerful aid to the individual engineer or student in the rapid solution of scientific and engineering problems.

The EAI 1000 is constructed with a modular housing system of two (2) sizes. These modules are fitted together and interconnections between trays are made with standard flat strip cables.

The models included in the basic system are:

Analog Module — Containing analog and digital computer elements. Up to three (3) analog modules may be accommodated in any one system.

Display Module — Containing all necessary displays for value readout, function addressing and overload.

Control Module — Containing power supplies, microprocessor control system multiplexer, mode control and keyboard. The control module can support up to three (3) analog modules.

Expansion Modules are:

Analog Modules — As previously described. Two expansion trays can be added to a basic system.

Digital Module — Containing additional digital computing elements plus facilities for hybridisation. One digital tray can be fitted to a basic system.

Expansion Elements are:

Summer Module)
Sin/Cosine Module)
Log/Antilog Module)
Vector Module) These elements are optional items housed in any analog tray
Multiplier Module)
Function Relay Module)

Buffer amplifier – Housed in the control modules. Six amplifiers are provided with patch selectable gain values of ½, unity and 2.

The EAI 1000 utilizes a building block concept, in which individual computing components may be easily interconnected to solve the required equations by forming electronic modules analogous to the system under study. Each building block, either individually or in combination with others, is capable of performing one or more mathematical operations. The computing components in the EAI 1000 are housed on P.C. cards behind removable patch panels.

The analog module, comprising a removable patch panel, potentiometer panel and analog component card contains:

4 Integrators
6 Summers (including 2 Summer/Stores)
2 Multipliers
2 Comparators
2 Analog Switches
10 Grounded Potentiometers
2 Ungrounded Potentiometers
2 Free Function Positions
2 Dual Input AND/NAND Gates
2 D Flip-Flops
24 Universal Trunk Lines
1 Free Diode

The Potentiometer or coefficient panel is mounted to the right-hand side of the analog removable patch panel. This unit couples ten (10) grounded potentiometers to the analog panel.

The digital module, comprising a digital removable patch panel, digital control panel and digital component card contains:

6 Dual Input and Gates
4 Triple Input NAND Gates
4 D Flip Flops
2 4-Stage Binary Counter
2 4-Stage BCD Counter
2 Variable Monostables
8 Logic Switches
8 Logic Lamps
24 Universal Trunks
2 Clocks, one fixed frequency, one variable frequency
1 Provision for Hybridisation.

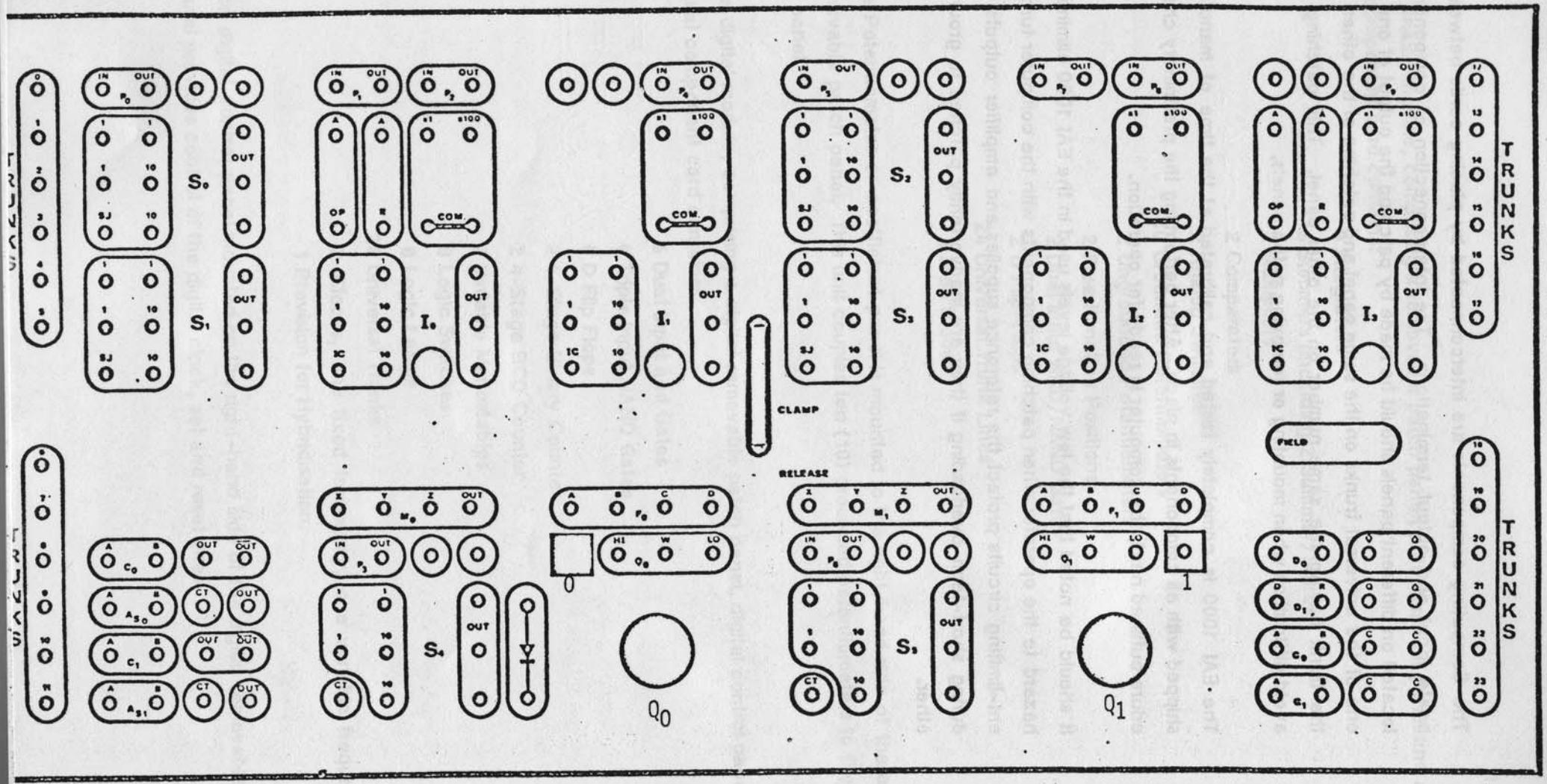
The digital control panel mounted on the right-hand side of the digital removable patch panel provides control of the digital clock, set and reset lines.

The Computing components are interconnected by placing cords between the appropriate input and output terminations. The interconnection of components which are located on different panels should be made by patching the output of one component to one of the universal trunks on the same panel and patching of the other component to the trunk having the same number on the other panel. This patching approach will avoid difficulties when mounting or removing patch panels.

The EAI 1000 is completely tested and calibrated at the time of manufacture and is shipped with all components in place. After performing the preliminary check-out procedure outlined next, the computer is ready for operation.

It should be noted that the low voltage levels used in the EAI 1000 eliminate any shock hazard to the operator when patching components with the computer turned on. Current-limiting circuits protect the reference supplies and amplifier outputs from damage during short-term overloading if they are inadvertently patched to ground or to each other.

ANALOG PATCH PANEL



CHAPTER 2

OPERATING PROCEDURES

2.1 INITIAL SET UP PROCEDURES

In order to ensure that the equipment will function correctly, it is advisable that the following initial set up procedures be followed before the equipment is switched on.

2.1.1 Rating

Check that the equipment is correctly rated for either 240V, 50Hz or 120V, 60Hz operation. This information is displayed on the rating plate located on the back of the CONTROL tray. Remove the transit cover for access to the rating plate.

2.1.2 Integrator Mode

Check that integrators Nos. 0 and 3 have patch plugs connecting control signals A and $\overline{A}$ to OP and R buses respectively. Integrators 1 and 2 are connected directly to the master mode control and therefore do not require external mode control.

2.1.3 Integrator Feedback

Check that all integrators have the X1 capacitor connection in the Feedback loop. A single patch plug may be used for this purpose, connecting to the input/output positions indicated by '1' (the integrator has provisions for operation at 1 and 100 volts per second respectively).

2.1.4 Summer Feedback

Check that all summers have a patch lead between output and a unity (1) input.

2.1.5 Keyboard

Check that keyboard connector is firmly and fully located and that all keys operate freely.

2.1.6 Slaving Plug

Check that a slaving connector is fitted to the slaving output at the back of the control module. If two computers are to be slaved together, then a slaving cable should be connected between the two slaving outputs.

2.1.7 Switch ON

Switch power ON and allow 10 minutes warm-up. Note for safety reasons, the power switch is located on the back of the unit so that no large voltages are connected to the front panel. Depress I.C. key which selects the initial condition mode of operation.

2.1.8 Overload

If any overload indicators are illuminated, check:

(a) I.C. key depressed and I.C. mode LED on keyboard illuminated.

(b) The element/module showing an overload is correctly patched.

Correction of these points should extinguish the overload indicator. Confirm this by redepressing the I.C. key.

2.1.9 Computer Addressing

To set the microcomputer program for correct operation, depress the RESET key. All displays in the Function, Field, Number and Value areas will extinguish except the decimal point (.). Depress any function key – the selected Function LED will illuminate.

NOTE: The 'C' key and unmarked keys will cause the function display to flash unless DCA's or a special modification is fitted. Select another key. Depress 'O' key twice – Field O LED plus function number 0 will illuminate. The value of the output of the selected module in machine units will also be displayed after the function number is entered.

2.1.10 Logic Circuits

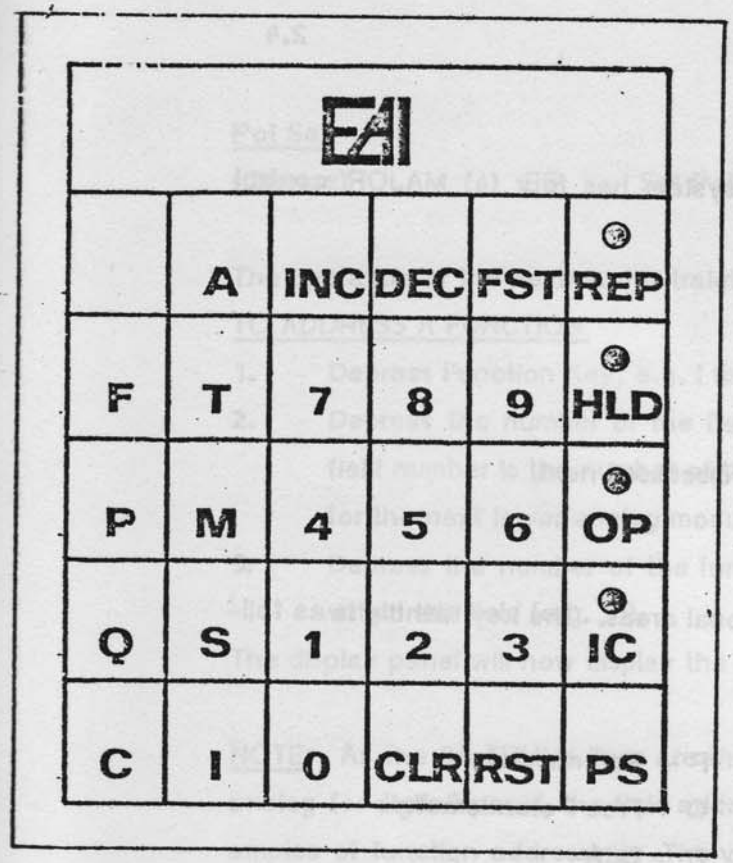
Connect Patch cord between L_1 and S_1, and L_2 and S_2 eyelets. The logic lamps will extinguish and indicate on depression of the appropriate logic switch.

2.1.11 Mode Control

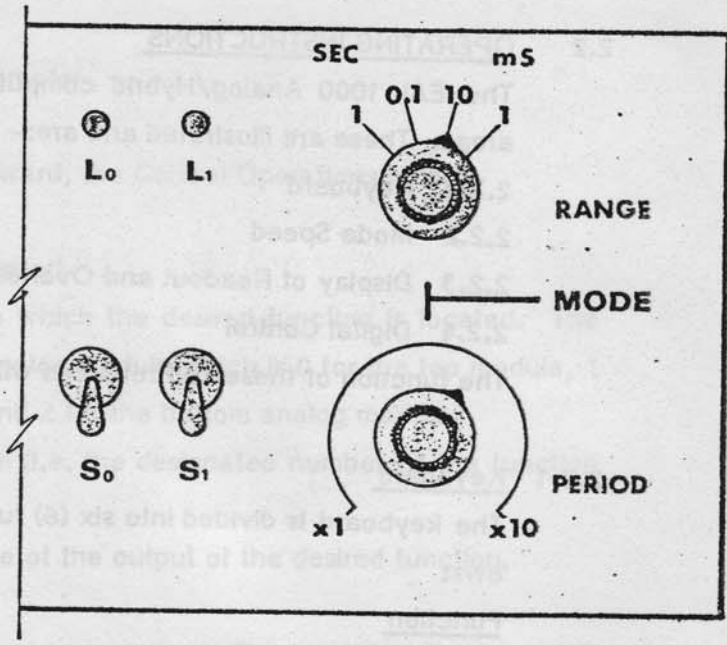
Set mode time switch to 1 SEC. Connect A and L_1, $\overline{A}$ and L_2 patch eyelets. Confirm operation according to table:

DEPRESSED KEY	LAMP INDICATION	
	$L_1(A)$	$L_2(\overline{A})$
I.C.	ON	OFF
HLD	ON	ON
OP	OFF	ON
REP	Alternating	Alternating

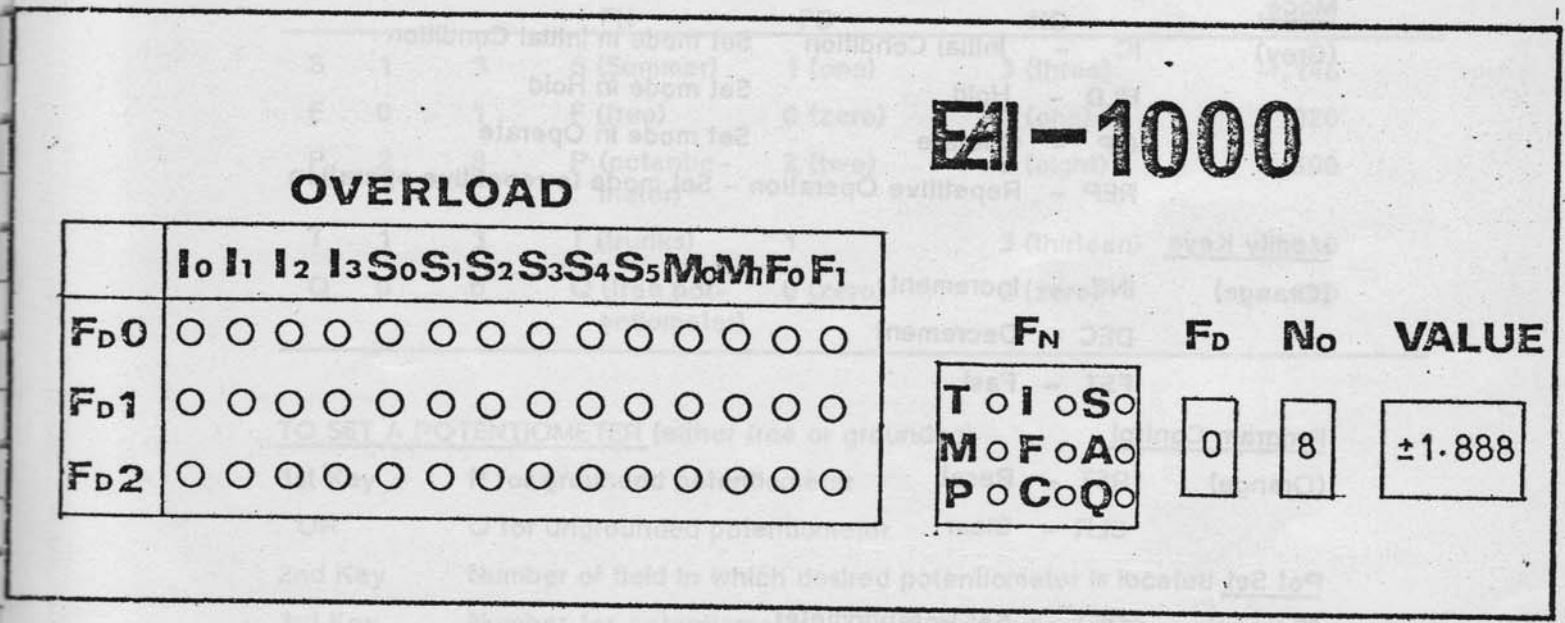
The EAI 1000 Analog Computer is now ready for operation.



KEYBOARD



MODE CONTROLS



DISPLAY PANEL

FIGURE 2.1 - EAI-1000 CONTROL AREAS

2.2 OPERATING INSTRUCTIONS

The EAI 1000 Analog/Hybrid computing system has four (4) MAJOR control areas. These are illustrated and are:-

2.2.1 Keyboard

2.2.2 Mode Speed

2.2.3 Display of Readout and Overload

2.2.4 Digital Control

The function of these control areas will be discussed next.

2.2.1 Keyboard

The keyboard is divided into six (6) functional areas. The key identity is as follows:

Function

(Green)	T - Trunks	P - Potentiometer
	I - Integrator	Q - Free Potentiometer
	S - Summer	C - DCA
	M - Multiplier	F - Free Function
	A - Analog Switch	Plain - Spare (unused)

Numbers

(White) 0 - 9

Mode

(Grey)	IC - Initial Condition	Set mode in Initial Condition
	HLD - Hold	Set mode in Hold
	OP - Operate	Set mode in Operate
	REP - Repetitive Operation	- Set mode to repetitive operation

Modify Keys

(Orange)	INC - Increment
	DEC - Decrement
	FST - Fast

Program Control

(Orange)	RST - Reset
	CLR - Clear

Pot Set

(Orange) PS - Set Potentiometer

Pot Set

(Orange) PS – Set Potentiometer

The operation of the keyboard is traightforward, the Control Operations being:

TO ADDRESS A FUNCTION

1. Depress Function Key, e.g. I (Integrator)
2. Depress the number of the field in which the desired function is located. The field number is the number of the analog module which is 0 for the top module, 1 for the next lower analog module and 2 for the bottom analog module.
3. Depress the number of the function (i.e. the designated number of the function within the field [e.g. 3]).

The display panel will now display the value of the output of the desired function.

NOTE: As the 23 TRUNK lines are Universal and appear in the same location on each analog (or digital) panel, the field address is not required. The following table gives examples of function addressing. The values shown are hypothetical and depend on the program under investigation.

Key Depression			Display			
1st	2nd	3rd	Function	Field	Number	Value in Machine
			FN	FD	NO	Units
S	1	3	S (Summer)	1 (one)	3 (three)	– .146
F	0	1	F (free)	0 (zero)	1 (one)	+ .020
P	2	8	P (potentio-meter)	2 (two)	8 (eight)	+ .600
T	1	3	T (trunks)	1	3 (thirteen)	– .810
Q	0	0	Q (free pot-entiometer)	0 (zero)	0 (zero)	+ .500

TO SET A POTENTIOMETER (either free or grounded)

1st Key P for grounded potentiometer

OR Q for ungrounded potentiometer

2nd Key Number of field in which desired potentiometer is located

3rd Key Number for potentiometer. The display indicates the value at the output of the potentiometers.

4th Key Pot Set – HOLD KEY DOWN – The display indicates the ratio or coefficient of the potentiometer when positive reference is applied. The value will be positive. Adjust to the required value. Release POT SET key.

TO CORRECT AN INCORRECT ENTRY

The Clear (CLR) Key, when depressed once, will delete the last instructions entered, enabling a correct or modified instruction to be entered. For example: Address required integrator, Field zero, Number 2, instead of number 1 entered. Depress CLR once, depress Number 2.

If the CLR key is pressed twice, the whole instruction is erased and addressing is re-repeated.

The Reset Key

Depression of the Reset Key will halt and restart the entire micro-processor program. All previously entered instructions are invalidated. The Reset Key may be depressed at any time. It has no effect on problem solution.

Mode Selection

The four Mode Select keys are independent of all other key groups and any desired mode state can be selected at any time. Selection of a mode state is by depression of the appropriate key. The mode control provides a means of controlling the solution of problems, once scaled and patched, ready to run on the computer.

Initial Condition (I.C.)

All integrators switched to the conditions required at the commencement of the problem solution. In this condition, signals connected to integration inputs are disconnected.

Operate (OP)

All integrators accept all inputs and integration starts, and continues until another condition is selected.

Hold (HLD)

All inputs of all integrators are removed. All programme variables are held at a constant value, enabling checking or listing for evaluation.

Repetitive Operation (REP)

In this state, I.C. and OP are alternatively selected at a rate determined by the Mode Range controls.

The Modify Keys

The keys INC and DEC (Increment and Decrement) enable the addressing of functions to be stepped forward or backwards one at a time. A single depression of the keys will move the addressing up or down by one position. If either of the keys are held down, stepping, either up or down, will continue through the total complement of the addressable machine functions. The Key FST (Fast) is a provision for planned future product enhancements. In present systems, no increase in increment or decrement rate will occur if FST is depressed.

The sequence of addressing of funtions when in the step (or modify) condition is:

Trunks	0	through to	23	followed by		
Integrators	0	"	"	3	"	"
Summers	0	"	"	5	"	"
Multipliers	0	"	"	1	"	"
Free Function	0	"	"	1	"	"
Analog Switches	0	"	"	1	"	"
Grounded Potentiometer	0	"	"	9	"	"
D.C.A.S. (if fitted)	0	"	"	9	"	"
Ungrounded Potentiometers	0	"	"	1		

NOTE: Where more than one field is fitted, address of each module type is completed for all fields followed by the next listed module type.

The Set Potentiometer Key

This key is also independent of all other keys. When depressed, it disconnects the inputs of all potentiometers (both P and Q) and connects the analog positive reference (+1 machine unit) to the potentiometer input. The potentiometers can then be addressed (as previously described) and the coefficient value displayed. Alternatively, the potentiometer may be adjusted to a desired coefficient setting.

2.2.2 Mode Speed

The mode speed controls are mounted in the R.H.S. of the control front panel. Two controls are provided:

a) A calibrated 4 position range switch providing four repetitive Operating Periods of 1 sec, 0.1 sec, 10ms and 1ms. The fixed I.C. period associated with each of the above ranges are 0.1sec, 10ms, 1ms, 0.1ms respectively.

b) A 10-1 variable control which is operative at all times and modifies the selected range by up to a factor of 10:1. Thus the maximum Operate Period in the REP-OP mode is 10 seconds.

NOTE

i) The mode control system generates a ramp for driving the X axis of a peripheral plotter or display oscilloscope. This ramp is generated irrespective of whether or not the REP-OP is selected. When the OPERATE mode is selected, the ramp will rise at a rate determined by the mode range setting. It will limit at its full voltage and remain at that voltage until I.C. is selected. At this time the ramp will decay to zero at a rate determined by the selected mode range position.

ii) It must be clearly understood that alteration of the Mode Range Switch in no way changes the RATE OF PROBLEM SOLUTION. This is determined by the equations and time scaling of the problem under investigation. The value of Mode Range is that it provides a range of time "windows" through which the problem solution can be evaluated.

2.2.3 The Display Panel

This panel has no controls but provides an information display for the computer. The panel is in two sections:-

a) Addressed Information

Any required information readout is displayed along with the relevant addressing details.

The FUNCTION (FN) is indicated by a LED alongside a mnemonic:-

I	-	Integrator
S	-	Summer
M	-	Multiplier
A	-	Analog Switch
P	-	Grounded Potentiometer
Q	-	Ungrounded Potentiometer
F	-	Free Function
T	-	Trunks
C	-	D.C.A.'s (if fitted)

The Field (FD) is indicated by a number 0 - 2. Maximum is 3 analog fields per console. The NUMBER of the function within its field is indicated by a number 0 - 9.

NOTE The Universal Trunks (T) are not limited to any field anddwhen addressed , the field display (FD) indicator is utilised to enable display of Trunks 00 - 23.

As each segment of addressing is completed (e.g. FN, FD, No.), this information is immediately displayed providing the operator with a check on the validity of the addressing.

b) Overload Information

Each analog field is provided with 14 overload indicators, These indicate when function modules are being operated near to their limits of linear operation. This level is set at 1.1 machine units (i.e. 10% above Reference level) and applies to both positive and negative values. Three rows of indicators are provided - one for each field position. The functions provided with overload indication are:-

Integrators - 4 per field

Summers - 6 per field, including two with store facilities.

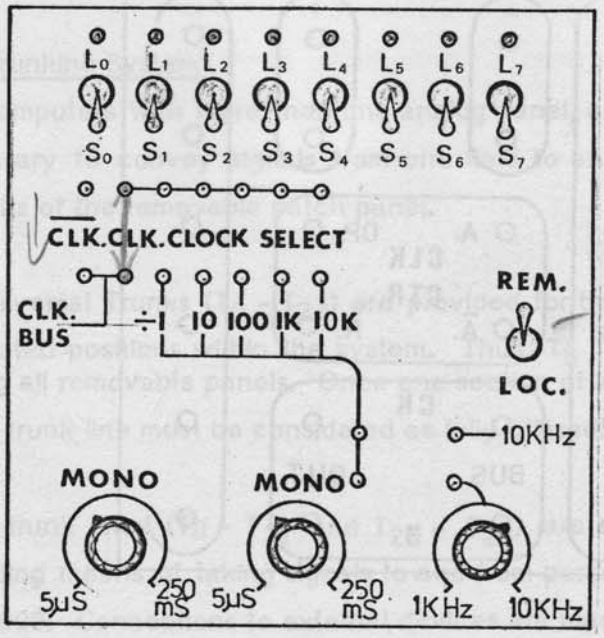
Multipliers – 2 per field

Free function – 2 per field

In normal operation, any other function modules overloading will, due to the programme patching, cause one or more of the above functions to overload. This will enable rapid location of the programme patching or scaling error.

2.2.4 DIGITAL CONTROL

The digital control panel supplies the control signals necessary for correct operation of the digital elements.



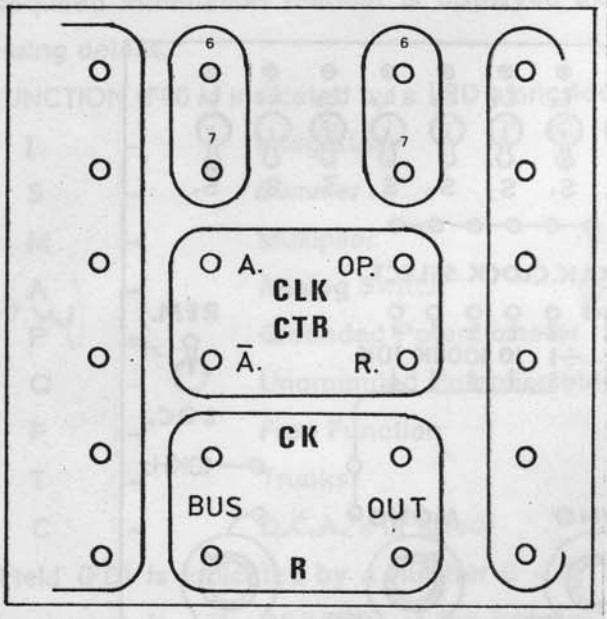
Prior to operation of the digital frame, patch the following with bottle plugs:

1) Select either fixed or variable oscillator and patch to divider.
2) Select and patch desired clock frequency/or range if variable clock has been selected.
3) Patch CLK to clock bus.
4) Put local/remote time switch to LOCAL.

On the Digital patch panel, patch:

1) On Clock Control area (CLK CTR):
   a) A to OP
   b) $\overline{A}$ to R

2) Patch the bus tines:
   a) Clock Line CK OUT to CLOCK BUS
   b) Reset Line R OUT to R BUS



The digital frame is now ready for normal operation with the clock controlled by the mode control circuits, which are controlling operation of the integrators on the analog frame(s).

2.3 Slave Mode

Two EAI 1000 computers can be slaved together to simulate larger problems. Slaving is carried out by removing the Dummy slaving plugs and linking the two computers with a slaving cable.

This procedure effectively transfers operation of the mode control of both computers to the unit to which the RED coded connector of the slaving cable is connected. In this condition the keyboard addressing of the two computers remains independent.

2.4 The Trunking System

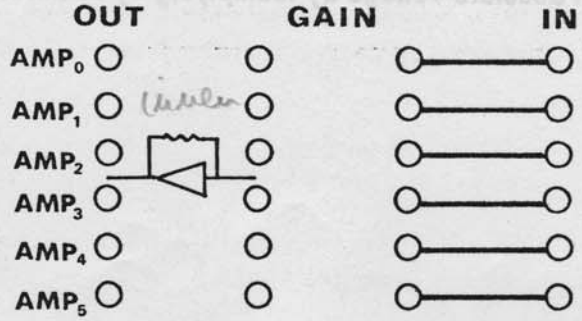
For computers with more than one analog panel, a system of trunking signals is necessary to convey signals from one field to another without sacrificing the benefits of the removable patch panel.

24 Universal Trunks (T_0 - T_{23}) are provided for this purpose. These lines have dedicated positions within the system. Thus, T_0 is a single trunk or signal path linking all removable panels. Once one section of a trunk line is used, that particular trunk line must be considered as fully utilised.

Eight trunk lines (T_8 - T_{11} and T_{20} - T_{23}) are available on the control panel providing means of taking signals to and from peripheral devices external to the EAI 1000. Connections to external devices are made via the external trunk lines (XT_0 - XT_7) which link the External trunk patch panel points to the Slave/Trunk/External connector mounted on the rear of the Control Module.

2.5 Trunk Buffer Amplifiers (Optional)

Provision has been made to accommodate a buffer amplifier card holding six (6) current amplifiers of preset gains. Fig 3 shows the patch point arrangement:



The gain is preset by inserting a gain plug in the appropriate GAIN patch points. Three preset gain settings are provided with the optional buffer card. These are unity gain, X2 gain and X½ gain. GAIN plugs providing other gain settings are available on request.

2.6 EXTERNAL Plotter and CRT Display

As described in Section 2.4, the external trunk lines provide signal paths from the control panel patch area to the Slave/Trunk/External connector. Also provided are lines enabling control of these external devices. These lines are:

A, $\overline{A}$	For a logic signal commanding the plotter to plot.
RAMP	For an analog RAMP signal generated by the Mode Control circuitry and used to provide the horizontal (X) displacement of a CRT trace or plotter pen.

The signal A provides a logic "0" when the OPERATE mode is selected. The Ramp signal is positive going 1 to +5V when OPERATE mode is selected. Fig 4 shows these patch points and their function.

2.7 System Hold

By applying a logic zero (i.e. connection to DIGITAL ground) to the patch point HLD (HOLD), all integrators are placed in the HOLD mode (refer Section 3.2). A signal from the overload section is provided at the OVL (OVERLOAD) patch point which is a logic zero when any function is in an overload condition. If HLD is patched to OVL, the problem solution is held or frozen at the instant any module goes into overload.

2.8 Use of Value Display as Voltmeter

To monitor a signal other than a function output (e .g. a signal from a peripheral device), connect the signal to an unused UNIVERSAL TRUNK line. Address the TRUNK line as described previously and the signal value is displayed. The readout converts to an absolute voltage by multiplying by a factor of 5.

2.9 Logic Elements

The Control Panel provides basic logic control and monitoring facilities, these are:-

2 x LOGIC SWITCHES which provide a logic "1" at S_0 and S_1 respectively as SW_0 and SW_1 are depressed.

2 x LOGIC INDICATORS – 2 x LED lamps L_0, L_1 which are illuminated when a logic "1" is applied to patch points L_0 and L_1 respectively.

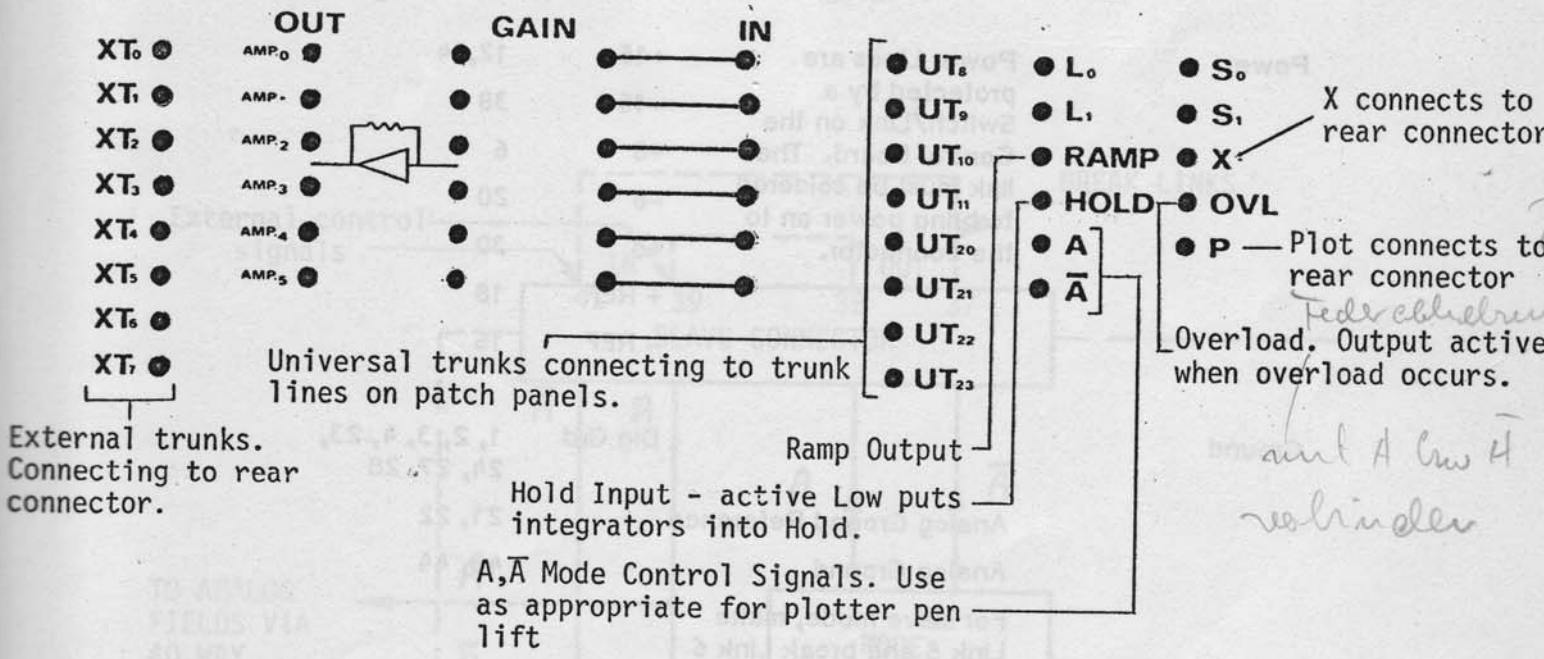


FIG. 4

2.10 SLAVE/TRUNKS/PERIPHERAL CONNECTOR

A single connector (SKU) provides the user with a means of linking the EAI 1000 to external equipment such as displays, plotters, or another EAI 1000 (slaving). This connector accommodates the following:

FUNCTION	NOTES	DESIGNATION	PIN NO.
External Trunks	Terminate On Control Front Panel	XT_0	5
		XT_1	7
		XT_2	9
		XT_3	11
		XT_4	13
		XT_5	15
		XT_6	17
		XT_7	19
Power	Power Lines are protected by a Switch/Link on the Control Board. The link must be soldered to bring power on to the connector.	+15	12,14
		-15	38
		+8	6
		-8	20
		+5	30
		+ REF	18
		- REF	16
Ground		Dig Grd	1, 2, 3, 4, 23, 24, 27, 28
	Analog Ground Reference	-	21, 22
	Analog Ground	-	43, 44
	For slave mode, make Link 5 and break Link 6 on slave computer.		
Mode Control	from Mode Control	A out	35
	from Mode Control	$\bar{A}$ out	37
	To A and $\bar{A}$ buses on Analog & Control trays	A in	40
		$\bar{A}$ in	41
Plotter/Display	Terminate on Front Panel of Control Tray	X	29
		P	31
Ext Hold	Active Low Sets Mode into Hold.	-	33

The XT_{0-7} lines are unassigned and may be utilised as required. If a slave/trunk cable (11.19.0001) is used, the lines XT_{0-7} of the master computer are linked to lines XT_{0-7} of the slaved computer. In addition, lines XT_{0-3} are connected to Y_{0-3} lines of the display oscilloscope.

Control of Integrators $I_{1,2}$

In each analog field, integrators $I_{1,2}$ are connected directly to the A & $\bar{A}$ buses. By making link changes on the slave/trunk connector, these two integrators can be controlled by external signals applied to the A & $\bar{A}$ patch points on the control front panel.

A and $\bar{A}$ links are broken on the slave connector. Control signals can then be patched into A and $\bar{A}$ patch points on the Control Front Panel, thus providing signals on the A and $\bar{A}$ bus lines (Fig. 5).

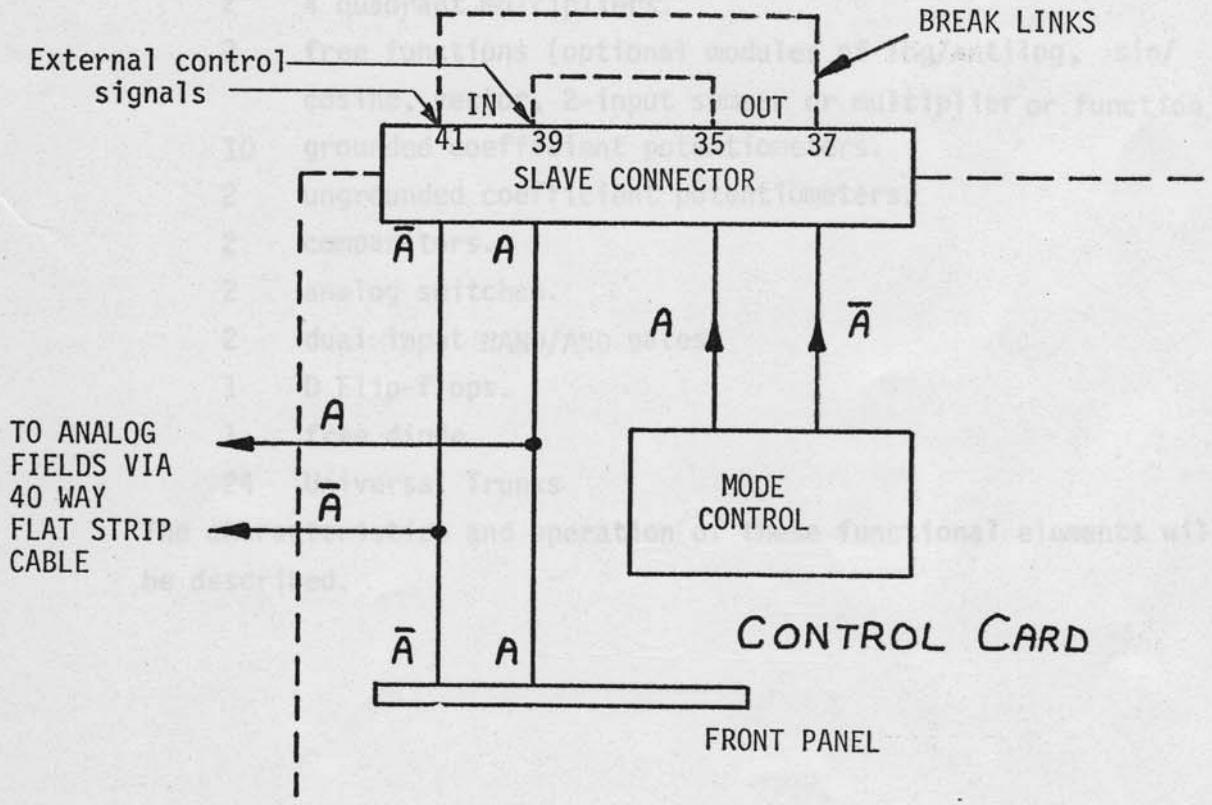


FIG. 5

CHAPTER 3

THE ANALOG TRAY

The analog tray comprises 3 main items

i - The analog removable patch panel

ii - The potentiometer panel

iii - The analog P.C. card

The analog P.C. card has no operational controls. For details refer to maintenance section.

3.1 The Analog Removable Patch Panel

The removable patch panel provides patch points for the function or computing elements housed on the analog P.C. card.

For the purposes of function description and patching, each functional element will be treated as a whole.

The functional elements available on each analog patch panel are:

4 integrators with 3 x 1 plus 2 x 10 gain inputs.

6 summers with 3 x 1 plus 2 x 10 gain inputs.

2 4 quadrant multipliers.

2 free functions (optional modules of log/antilog, sin/cosine, vector, 2-input summer or multiplier or function relay.

10 grounded coefficient potentiometers.

2 ungrounded coefficient potentiometers.

2 comparators.

2 analog switches.

2 dual input NAND/AND gates.

1 D Flip-flops.

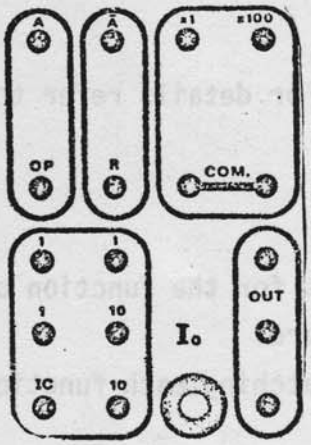
1 free diode

24 Universal Trunks

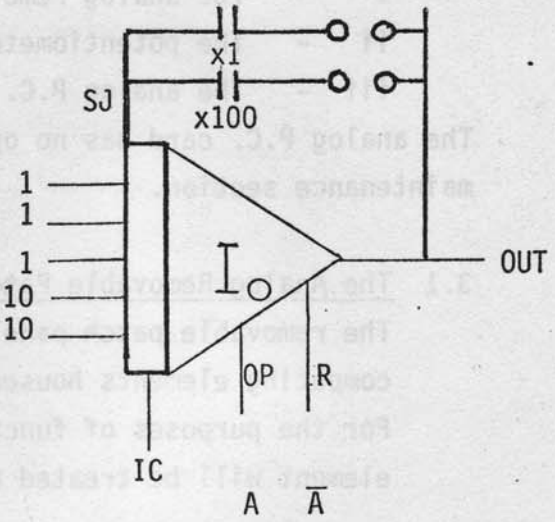
The characteristics and operation of these functional elements will next be described.

3.2 INTEGRATORS

PATCH PANEL LAYOUT



FUNCTIONAL DIAGRAM



Each Integrator has:

3 Unity gain inputs

2 10X gain inputs

1 Unity gain initial condition input

1 Real Time (x1) integration rate

1 100 x Real Time (x100) integration rate

The component elements determining the function accurance are selected to better than 0.25%.

For all applications the appropriate feedback path must be patched. This is shown in the patching diagrams.

Integrators may be set to operate in one of three modes.

a) Initial Condition

In this mode the integrator is internally switched to accept the signal from the INITIAL CONDITION patch point (IC) The output will set to a value equal in magnitude, but opposite in sign, to that applied to the IC patch point.

The facility enables a problem to be programmed with a specific set of

initial conditions. For example - the initial displacement of a pendulum, or the concentration of a chemical solution.

b) Operate.

In this mode the integration is internally switched to accept signals from the gain 1 and gain 10 inputs. Rate of integration is selected by patching from COM to x 1 or x100.

Note: When using the integrator as a summer, OPERATE mode must be selected.

c) Hold

In this mode all inputs are internally disconnected. The output remains at the value attained prior to the instant of switching to HOLD mode.

The Repetative Operation Mode (REP)

In this mode, Initial Condition and Operate are selected alternately at a rate preset by the Range and Period Control. (Refer 2.2.2)

This mode is selected in situations where multiple solutions to a problem are required, enabling adjustment of program parameters for an optimum solution.

External Control of Integrators

Integrators 0 and 3 have their control lines OP & R brought out to the patch panel. These are normally patched directly to A & $\overline{A}$ respectively thus bringing the integrator mode under the control of the Mode Control Circuitry. In certain applications it is necessary to control the mode of the integrator by separate logic signals. These may be derived within the EAI-1000 or externally. External control signals are patched via universal trunk lines or hardwired to the rear connector SKU.

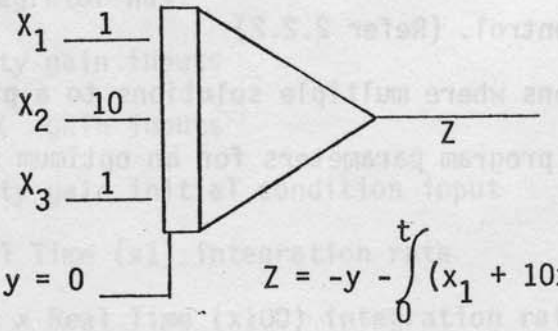
For control of integrators in this manner, the following truth table specifies the required logic signals for all mode conditions.

MODE	Logic signal applied to:	
	OP	R
Operate	0	1
Initial Condition	1	0
Hold	1	1

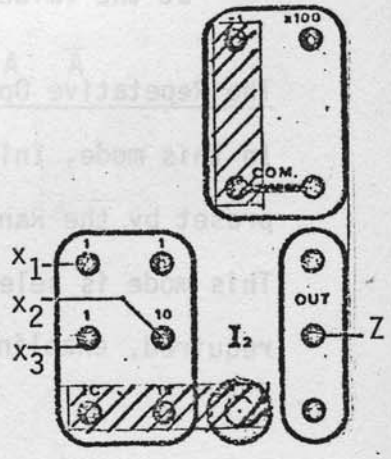
INTEGRATOR CONFIGURATIONS

(a) as an integrator.

real time

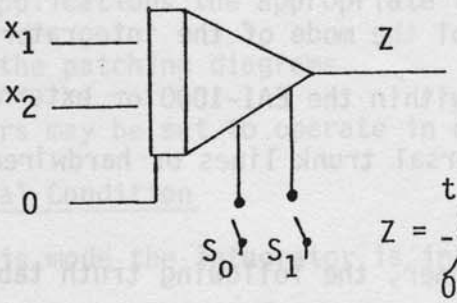


$$Z = -y - \int_0^t (x_1 + 10x_2 + x_3)dt$$

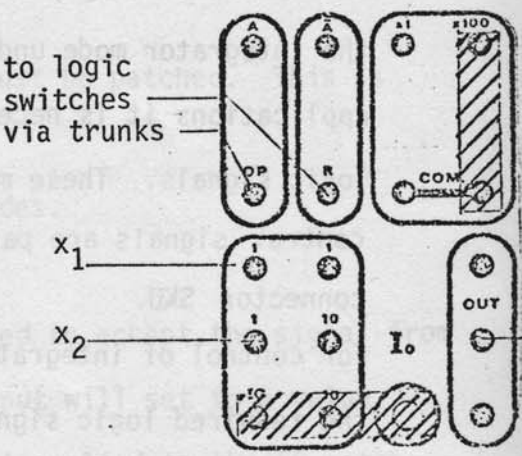


(b) as an integrator with external control.

at real time x 100

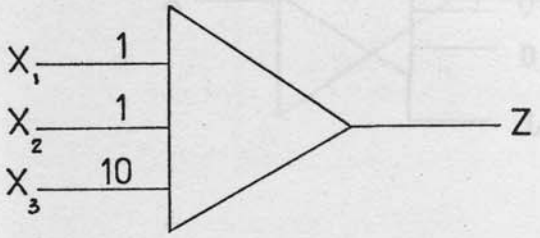


$$Z = -\int_0^t (x_1 + x_2)dt$$

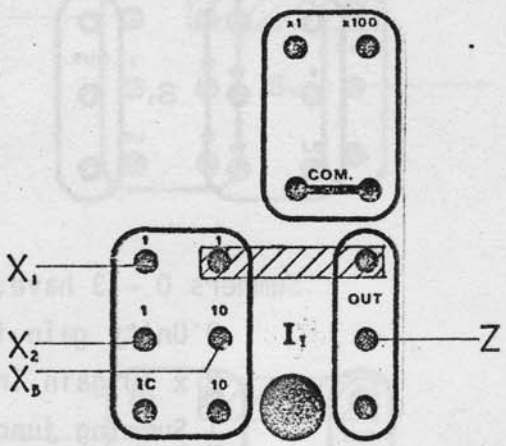


INTEGRATOR CONFIGURATIONS (CONT.)

c) USED AS A SUMMER

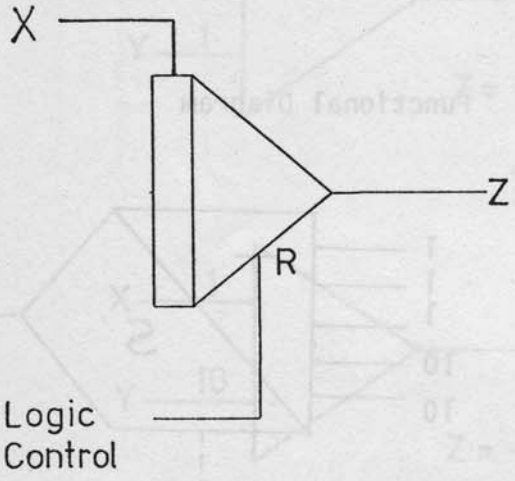


$$Z = -\Sigma X_1 + X_2 + 10X_3$$

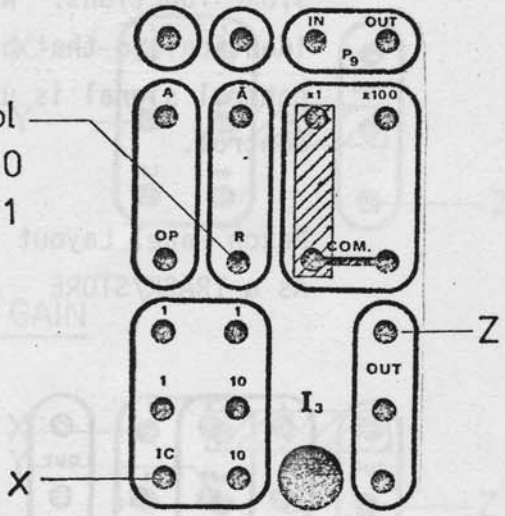


Note: 1. No integrator rate plug fitted.
2. Operate mode must be selected.

d) INTEGRATOR USED AS TRACK / STORE



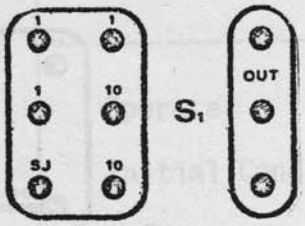
Logic Control
Track - Logic 0
Store - Logic 1



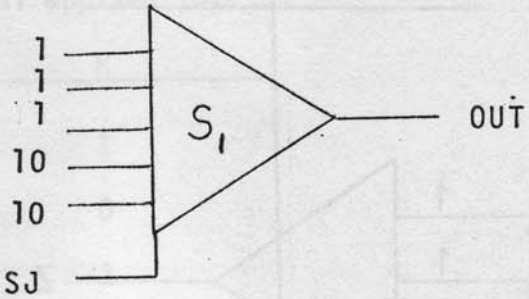
3.3 SUMMERS

a) Summers 0 - 3

Patch Panel Layout



Functional Diagram



Summers 0 - 3 have:

3 Unity gain inputs

2 x 10 gain inputs

1 Summing junction input

The components determining the accuracy of the summing function are selected to better than 0.25%.

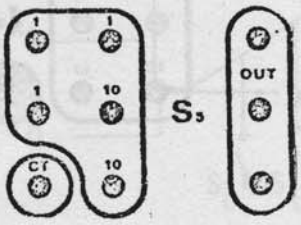
For all applications the appropriate feed back path must be patched. This is shown in the patching diagrams.

b) Summers 4 & 5

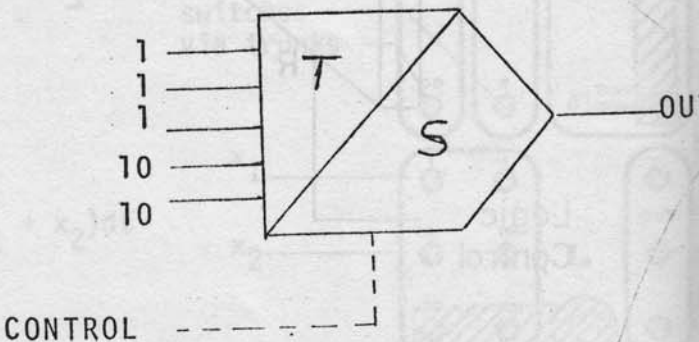
Summers 4 & 5 have the added feature of being able to operate as TRACK/STORE functions. When used as a summer, their operation and patching is identical to that of summers 0 - 3. To operate in the store mode a logic control signal is used. To put function in store, apply logic 0 to the control.

Patch Panel Layout

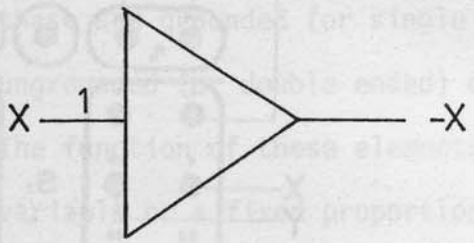
As a TRACK/STORE

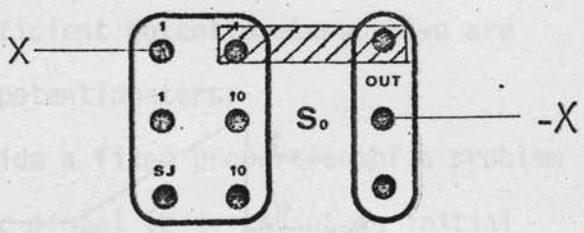


Functional Diagram

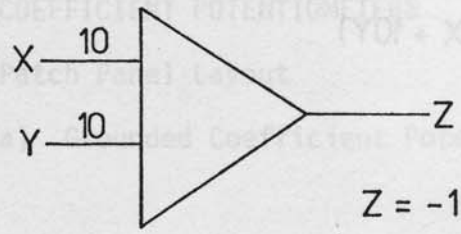


INDICATES SHORTING PLUG

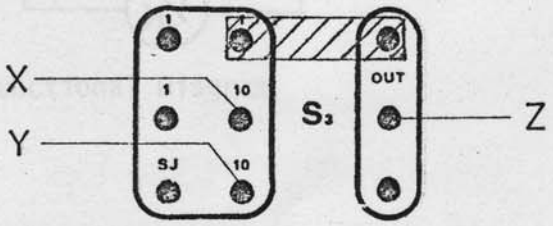




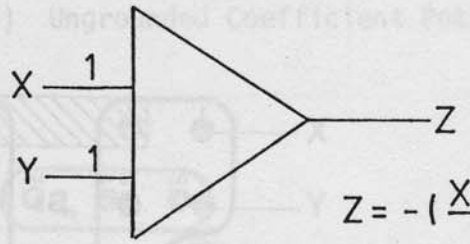
INVERTER



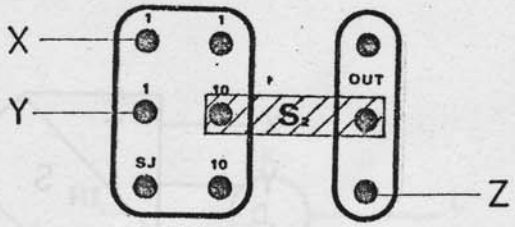
$$Z = -10\,(X + Y)$$



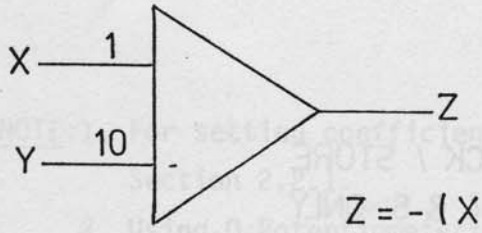
SUMMER x 10 GAIN



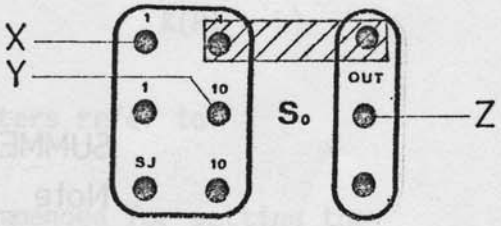
$$Z = -\left(\frac{X + Y}{10}\right)$$



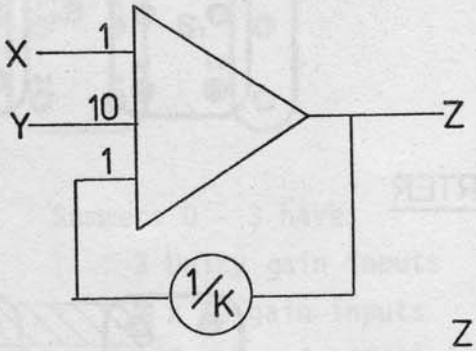
SUMMER x 1/10 GAIN

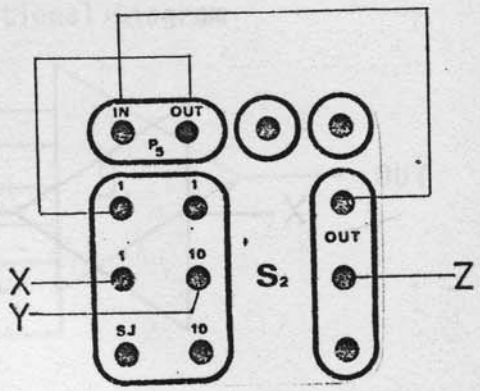


$$Z = -\,(X + 10Y)$$

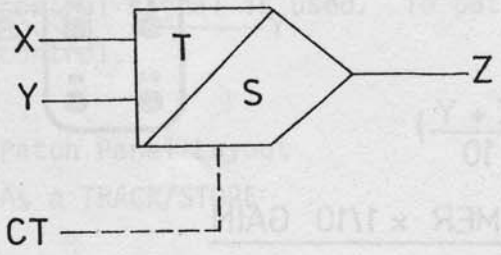


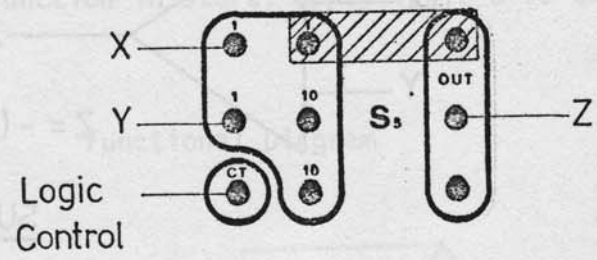
SUMMER PATCHING CONFIGURATIONS





$$Z = -K(X + 10Y)$$





SUMMER AS TRACK / STORE
Note SUMMERS 4 & 5 ONLY

3.4 COEFFICIENT POTENTIOMETERS

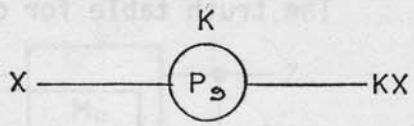
Twelve coefficient potentiometers are provided on each analog field. 10 of these are grounded (or single ended) coefficient potentiometers. Two are ungrounded (or double ended) coefficient potentiometers.

The function of these elements is to provide a fixed proportion of a problem variable or a fixed proportion of a static signal (e.g. to set an initial condition of an integrator). Numerous patch points of both +Ve and -Ve reference signals are provided for this purpose.

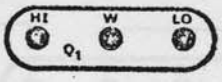
COEFFICIENT POTENTIOMETERS

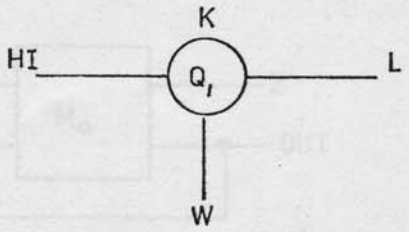
Patch Panel Layout Functional Diagram

a) Grounded Coefficient Potentiometers



b) Ungrounded Coefficient Potentiometers





K(HI - L)

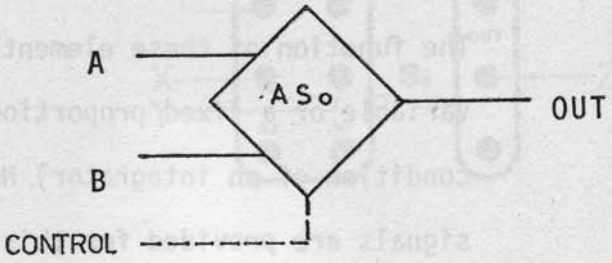
NOTE: 1. For setting coefficient potentiometers refer to Section 2.2.1.

2. Using Q Potentiometers is not recommended for setting the initial conditions of integrators.

3.5 ANALOG SWITCH

Patch Panel Layout

Functional Diagram



The analog switch is a high speed 2 way changeover FET switch. It operates directly into any function input.

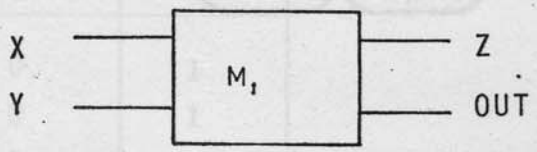
The truth table for operation of the analog switch is as follows -

	CONTROL SIGNAL 1	0
INPUT A	ON	OFF
INPUT B	OFF	ON

3.6 MULTIPLIERS

Patch Panel Layout

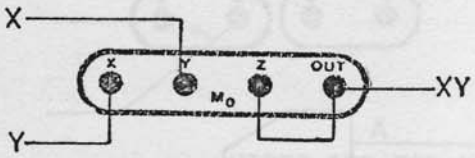
Functional Diagram

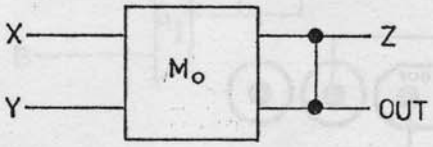


The Multiplier used is of the transconductance type which is internally adjusted to produce correct, machine scaled outputs from scaled inputs.

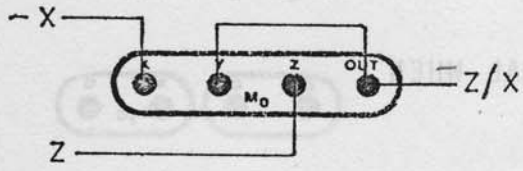
i.e. in the multiply mode the function equation is output = input X x input Y.

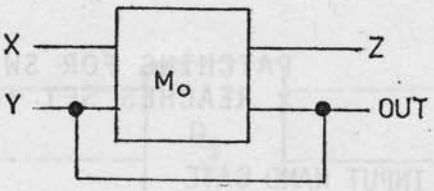
Patching Diagrams





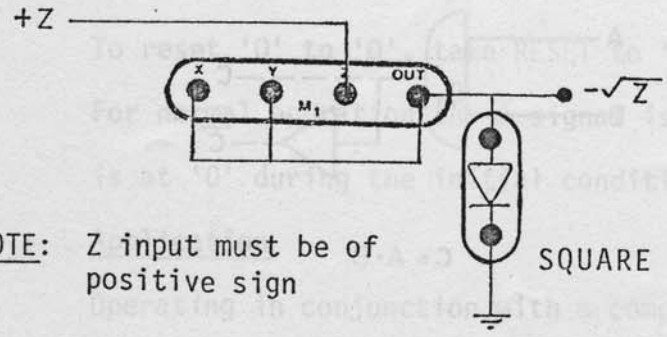
MULTIPLY





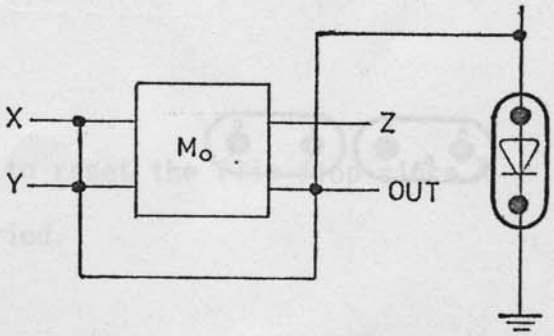
NOTE: X input must be of negative sign

DIVIDE



NOTE: Z input must be of positive sign

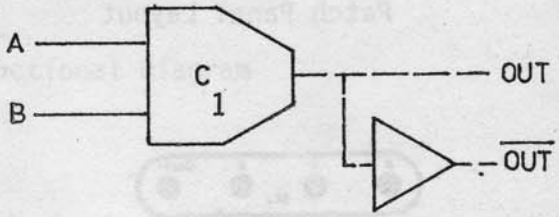
SQUARE ROOT



3.7 COMPARATORS

Patch Panel Layout

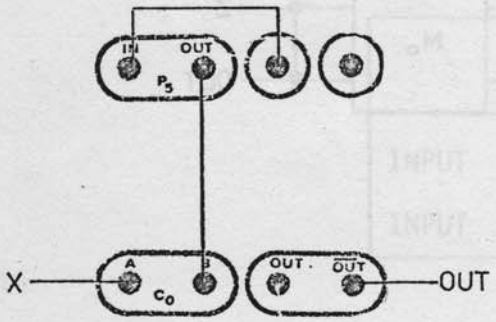
Functional diagram

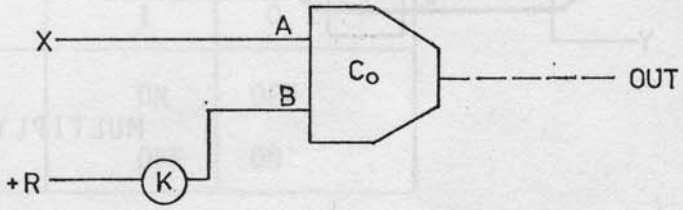


The comparators provide the facility of comparing two analog signals and producing a logic signal change when the one analog signal exceeds that of the other.

The truth table for the comparator is:-

Analog Signals	Logic Signal Output	
	C	$\overline{C}$
A > B	1	0
A < B	0	1



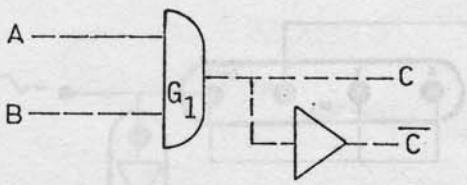


PATCHING FOR SWITCHING SIGNAL WHEN
x REACHES SET + Ve VALUE

3.8 DUAL INPUT NAND GATE

Patch Panel Layout

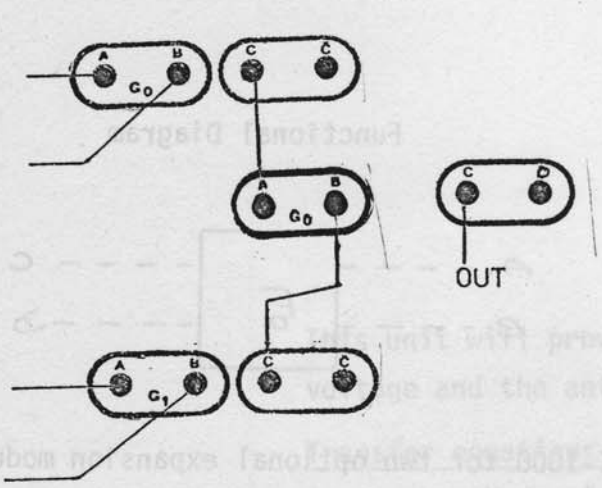
Functional Diagram

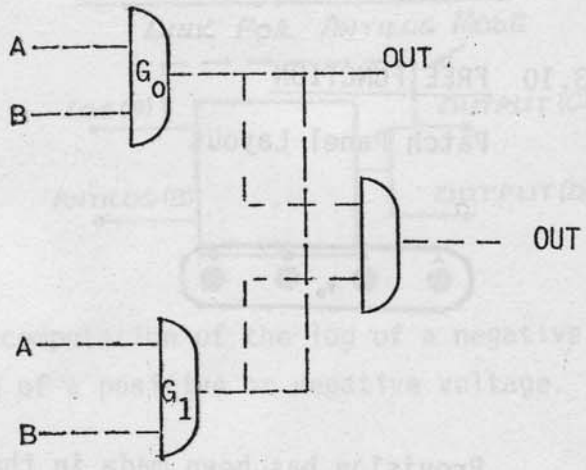


C = A·B

The truth table for the NAND gate is:

A	B	C	$\overline{C}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0





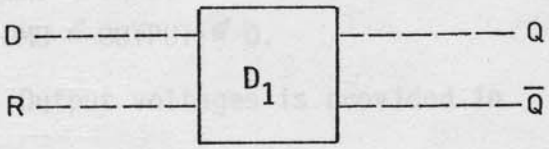
WIRED AND FOR FOUR INPUTS

NOTE: Do not connect outputs in parallel.

3.9 D FLIP-FLOP (Ret-Reset-Flip-Flop)

Patch Panel layout

Functional Diagram



Operation

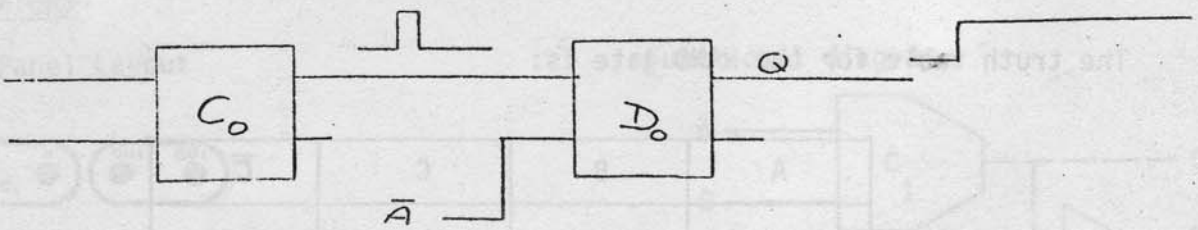
The output Q will set to '1' on the +ve edge at the data input when RESET is at '1'.

To reset 'Q' to '0', take RESET to '0'.

For normal operation the $\overline{A}$ signal is used to reset the flip flop since $\overline{A}$ is at '0' during the initial condition period.

Application

Operating in conjunction with a comparator to produce a logic control signal.

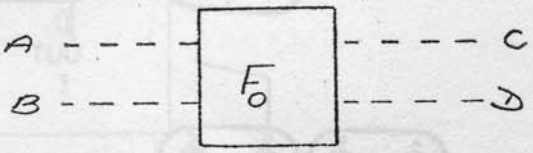


During the OPERATE period, the D flip flop will change state at the first comparator swtich and remain with Q at '1' until INITIAL CONDITION is selected. The flip flop will then reset to Q at '0'.

3.10 FREE FUNCTION

Patch Panel Layout

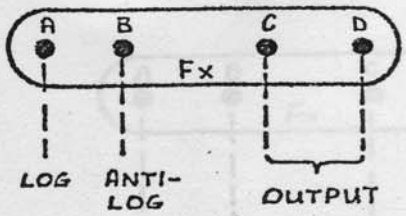
Functional Diagram



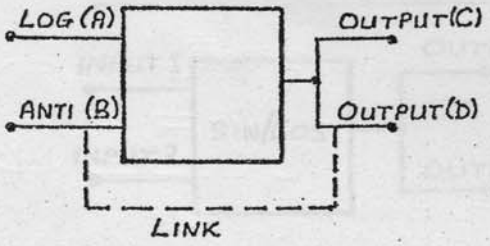
Provision has been made in the EAI-1000 for two optional expansion modules. For fitting and checking expansion modules refer to maintenance section.

3.10.1 Log/Antilog (Free Function)

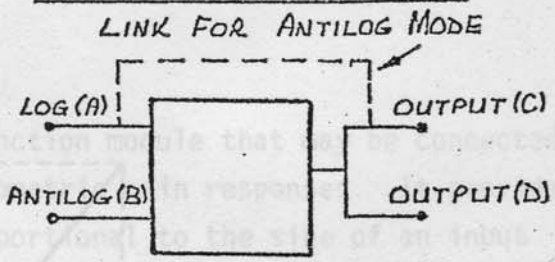
PATCH PANEL LAYOUT



LOG GENERATOR



ANTI LOG GENERATOR



This unit will provide computation of the log of a negative voltage and the antilog of a positive or negative voltage.

Transfer equations are:

i. Log Mode, Output = $.5 \log_{10} \left(\frac{\text{INPUT}}{-0.01}\right)$

Where,

-1.0MU (machine unit) $\leq$ OUTPUT $\leq +1.0\text{MU}$

$-1.0\text{MU} \leq$ INPUT < -0.01 MU

ii. Antilog Mode, OUTPUT = $0.01 \log_{10} \left(\frac{\text{INPUT}}{-0.5}\right)$

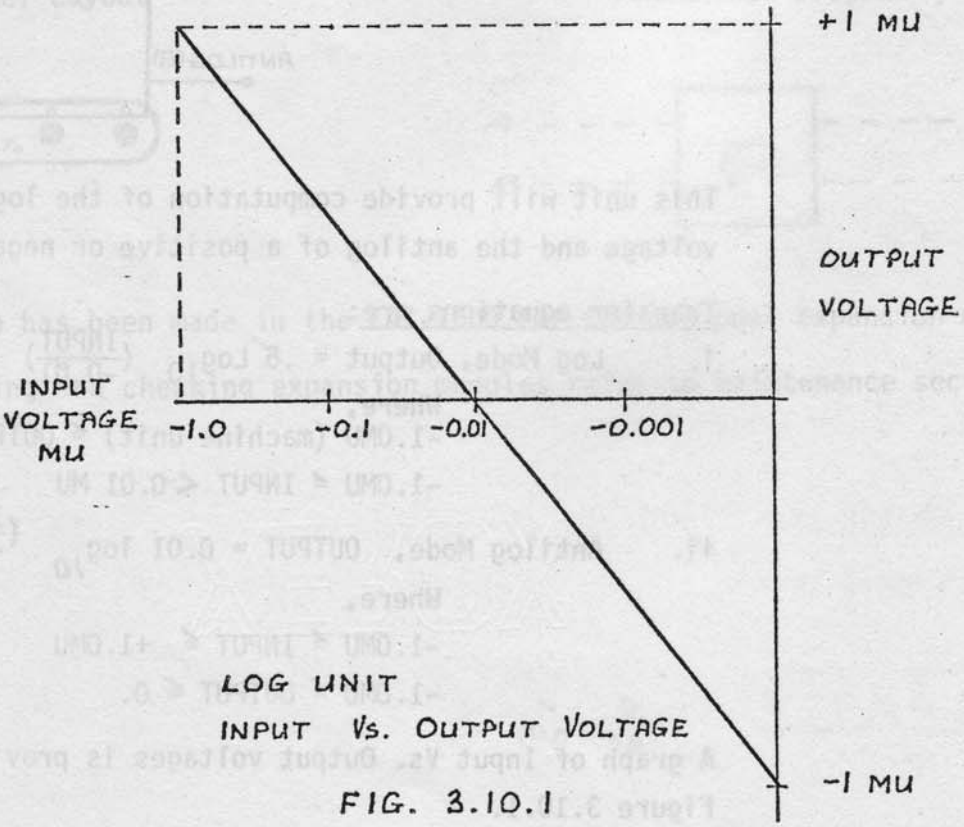
Where,

$-1.0\text{MU} \leq$ INPUT $\leq +1.0\text{MU}$

$-1.0\text{MU} \leq$ OUTPUT $\leq 0.$

A graph of Input Vs. Output voltages is provided in Figure 3.10.1.

NOTE: Amplifier offset (eos) has been adjusted at the factory for optimum performance.



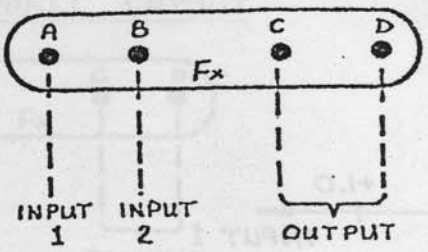
LOG UNIT
INPUT Vs. OUTPUT VOLTAGE

FIG. 3.10.1

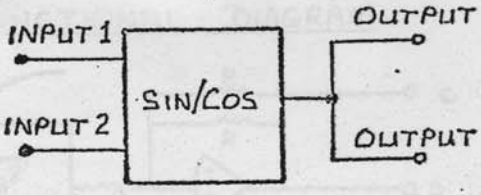
NOTE: Input must be within the range of .01MU to -1MU (-ve Ref).

3.10.2 Sin/Cos Function Generator

PATCH PANEL LAYOUT



FUNCTIONAL DIAGRAM



This unit is an analog function module that may be connected to provide various trigonometric gain responses. It provides a D.C. voltage output proportional to the sine of an input voltage where a 1.0mu input represents ±90 degrees of input angle. In addition, the module may be connected to obtain cosine functions.

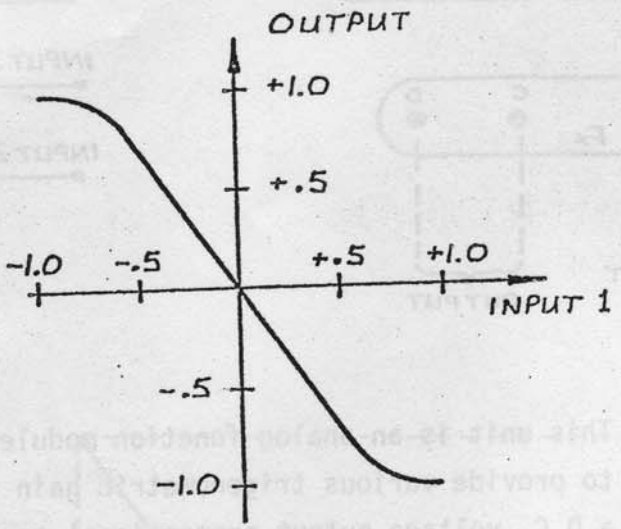
Transfer equations are:

i. For Sine Function, OUTPUT = sine θ, θ = INPUT x 90 degr
and -1.0mu $<$ INPUT 1 $<$ +1.0mu.

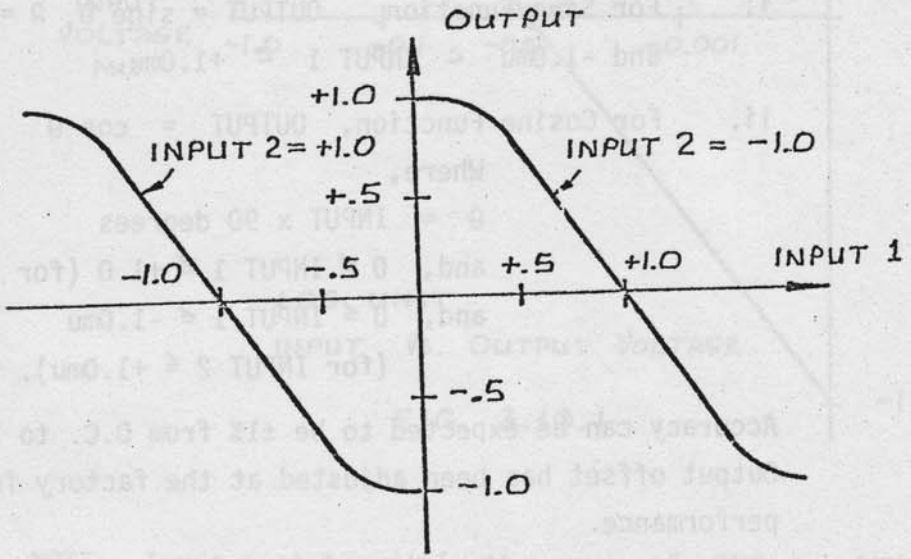
ii. For Cosine Function, OUTPUT = cos θ
Where,
θ = INPUT x 90 degrees
and, 0 $\leq$ INPUT 1 $\leq$ +1.0 (for INPUT 2 = -1.0mu
and, 0 $\leq$ INPUT 1 $\leq$ -1.0mu
(for INPUT 2 $\leq$ +1.0mu).

Accuracy can be expected to be ±1% from D.C. to 1KHz. Output offset has been adjusted at the factory for optimum performance.

Figure 3.10.2 shows the output functions for sine and cosine operation.



SINE FUNCTION

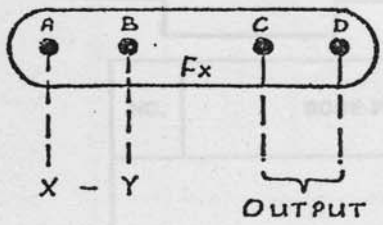


COSINE FUNCTION

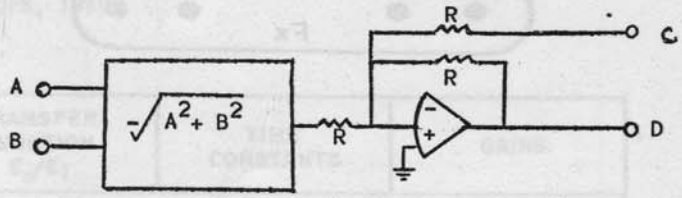
FIG. 3.10.2.

3.10.3 Vector Function Generator

PATCH PANEL LAYOUT



FUNCTIONAL DIAGRAM



TRANSFER FUNCTION

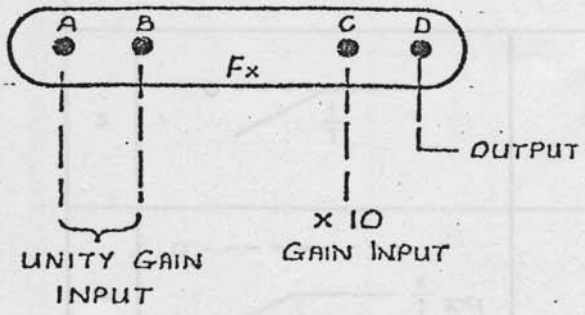
$$D = \pm\sqrt{A^2 + B^2}$$

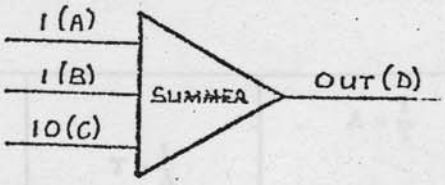
WITH C PATCHED TO D

$$D = +.5\sqrt{A^2 + B^2}$$

Output offset has been adjusted at the factory for optimum performance.

3.10.4 Summer (Free Function)

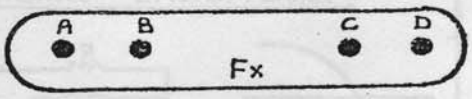


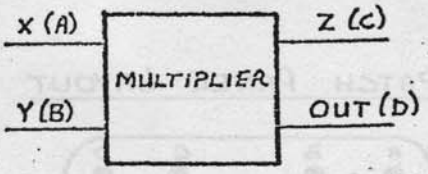


Transfer Function: Output = A + B + 10C.

NOTE: Patch unused input to ground on free summers.

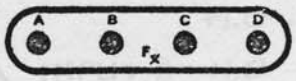
3.10.5 Multiplier (Free Function)





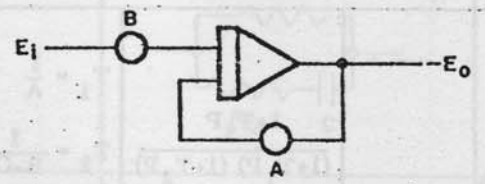
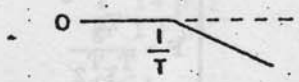
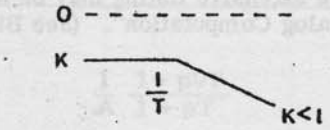
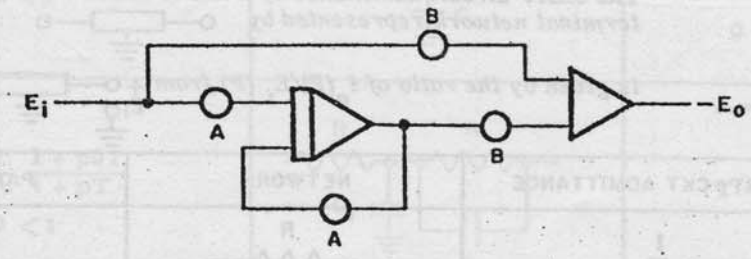
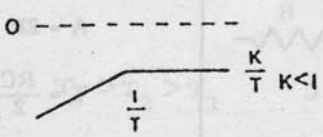
Refer to Section 3.6, Multipliers, for patching diagrams for obtaining multiply, divide and squareroot.

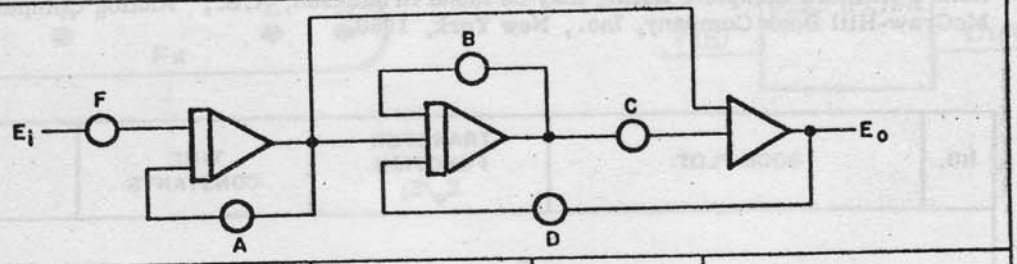
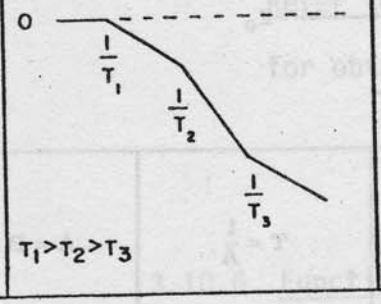
3.10.6 Function Relay (Free Function)



TRANSFER FUNCTION SIMULATION

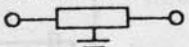
(1) The following table contains examples of amplifier circuits for simulating transfer functions . A more complete listing may be found in Jackson, A.S., "Analog Computation", McGraw-Hill Book Company, Inc., New York, 1960.

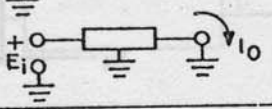
NO.	BODE PLOT	TRANSFER FUNCTION E_o/E_i	TIME CONSTANTS	GAINS
				
1		$\frac{1}{1+Tp}$	$T = \frac{1}{A}$	$A = B = \frac{1}{T}$
2		$\frac{K}{1+Tp}$	$T = \frac{1}{A}$ $K = \frac{B}{A}$	$A = \frac{1}{T}$ $B = \frac{K}{T}$
				
3		$\frac{Tp}{1+Tp}$	$T = \frac{1}{A}$	$A = \frac{1}{T}$ $B = 1$
4		$\frac{Kp}{1+Tp}$	$T = \frac{1}{A}$ $K = \frac{B}{A}$	$A = \frac{1}{T}$ $B = \frac{K}{T}$

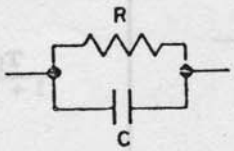
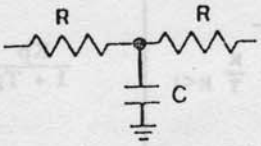
NO.	BODE PLOT	TRANSFER FUNCTION E_o/E_i	TIME CONSTANTS	GAINS
				
5.		$\frac{1+T_3P}{(1+T_1P)(1+T_2P)}$	$T_1 = \frac{1}{A}$ $T_2 = \frac{1}{B-CD}$ $T_3 = \frac{1}{B-C}$	$A = \frac{1}{T_1}$ $B = C + \frac{1}{T_3}$ C = Arbitrary >0 $D = \frac{1}{C}\left(\frac{1}{T_3} - \frac{1}{T_2}\right) + 1$ $F = \frac{T_3}{T_1 T_2}$

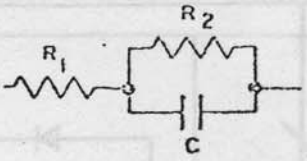
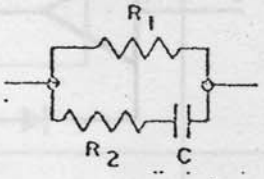
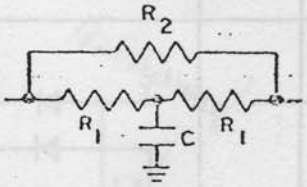
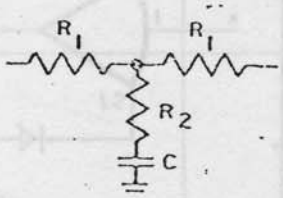
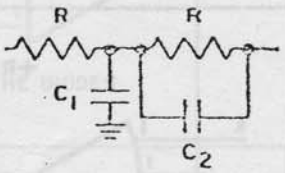
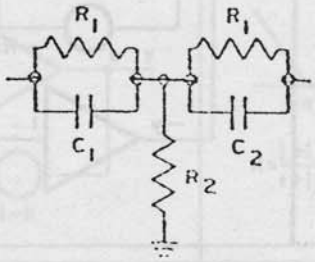
(2) The following table contains the short-circuit admittance and component values for some useful networks for simulating transfer functions. A more extensive listing may be found in Jackson, A.S., "Analog Computation", and Fifer, S. "Analog Computation". (See Bibliography.)

NOTE

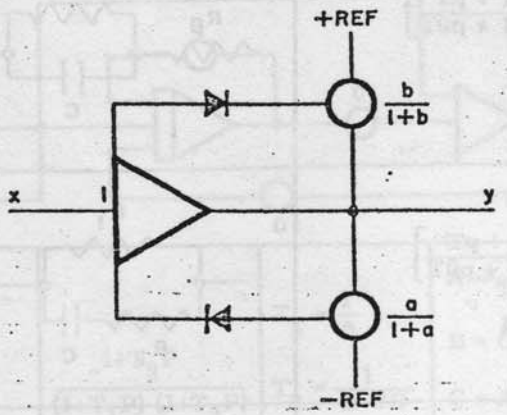
The short-circuit admittance of a two or three terminal network represented by 

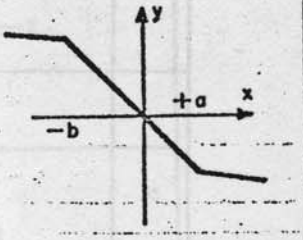
is given by the ratio of $I_o(P)/E_i(P)$ *from* 

NO.	SHORT-CKT ADMITTANCE	NETWORK	PARAMETERS
1.	$\frac{1}{A}$		A = R
2.	$\frac{1 + pT}{A}$		A = R T = RC
3.	$\frac{1}{A(1 + pT)}$		A = 2R $T = \frac{RC}{2}$

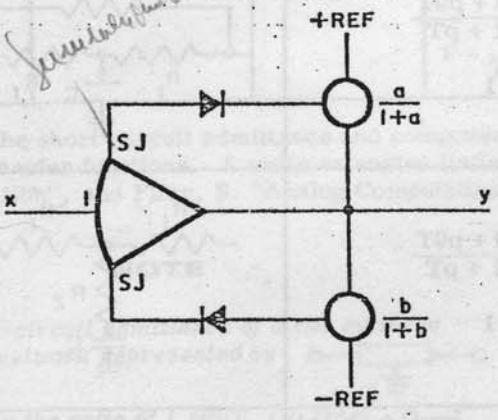
NO.	SHORT-CKT ADMITTANCE	NETWORK	
4.	$\frac{1}{A}\left[\frac{1+pT}{1+p\theta T}\right]$ $\theta < 1$		$A = R_1 + R_2$ $T = R_2 C$ $\theta = \frac{R_1}{R_1 + R_2}$
5.	$\frac{1}{A}\left[\frac{1+pT}{1+p\theta T}\right]$ $\theta < 1$		$A = R_1$ $T = (R_1 + R_2) C$ $\theta = \frac{R_2}{R_1 + R_2}$
6.	$\frac{1}{A}\frac{1+p\theta T}{1+pT}$ $\theta < 1$		$A = \frac{2R_1 R_2}{2R_1 + R_2}$ $T = \frac{R_1 C}{2}$ $\theta = \frac{2R_1}{2R_1 + R_2}$
7.	$\frac{1}{A}\frac{1+p\theta T}{1+pT}$ $\theta < 1$		$A = 2R_1$ $T = \left[R_2 + \frac{R_1}{2}\right] C$ $\theta = \frac{2R_2}{2R_2 + R_1}$
8.	$\frac{1}{A}\frac{1+p\theta T}{1+pT}$ $\theta < 1$		$A = 2R$ $T = \frac{R}{2}(C_1 + C_2)$ $\theta = \frac{2C_2}{C_1 + C_2}$
9.	$\frac{1}{A}\left[\frac{(1+pT_1)(1+pT_3)}{(1+pT_2)}\right]$ $T_1 > T_2 > T_3$		$A = 2R_1 + \frac{R_1^2}{R_2}$ $T_1 = R_1 C_1$ $T_2 = \left[\frac{R_1 R_2}{R_1 + 2R_2}\right](C_1 + C_2)$ $T_3 = R_1 C_2$

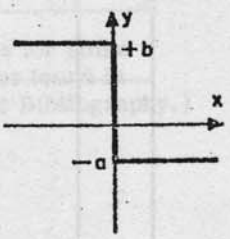
5. LIMITER



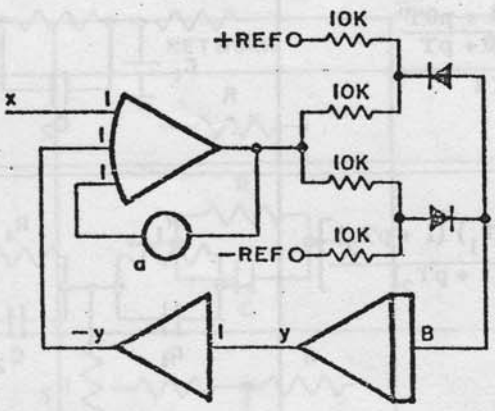


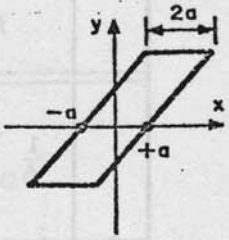
6. BANG-BANG CIRCUIT (CAN BE USED AS COMPARATOR



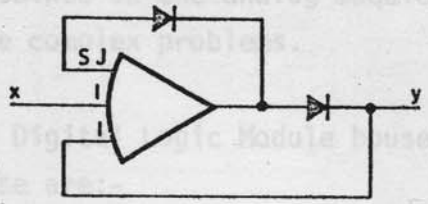
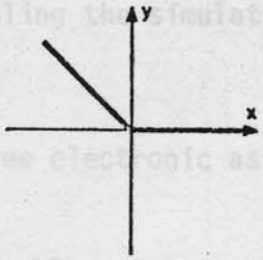
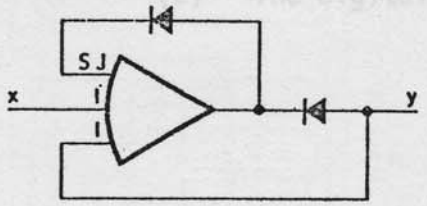
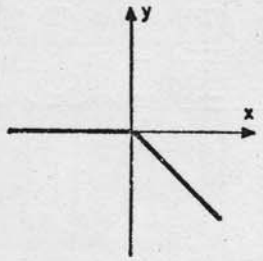
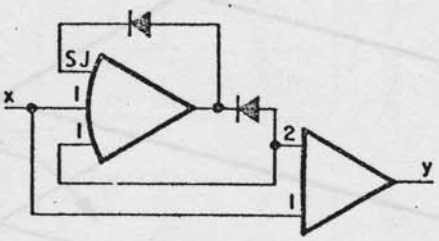
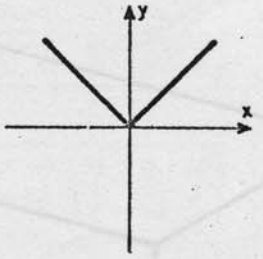
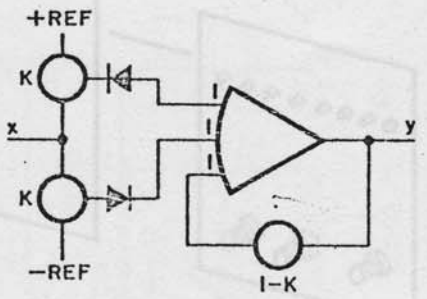
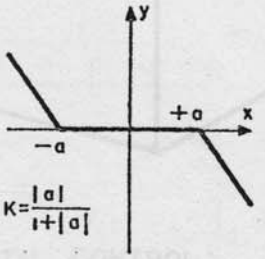


7. BACKLASH (HYSTERESIS)





REPRESENTATION OF CONSTRAINTS AND NONLINEARITIES

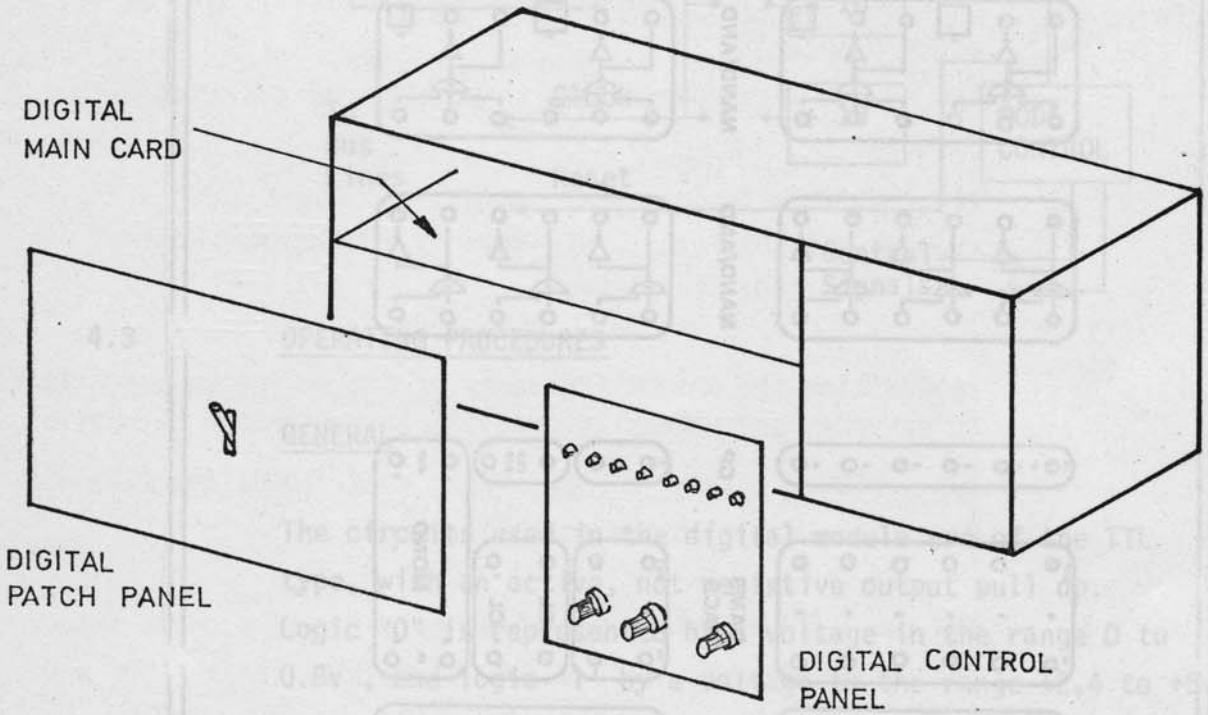
1. HARD ZERO LIMIT		
2. HARD ZERO LIMIT		
3. ABSOLUTE VALUE	 FOR $-\|x\|$, REVERSE THE DIODES	
4. DEAD SPACE		

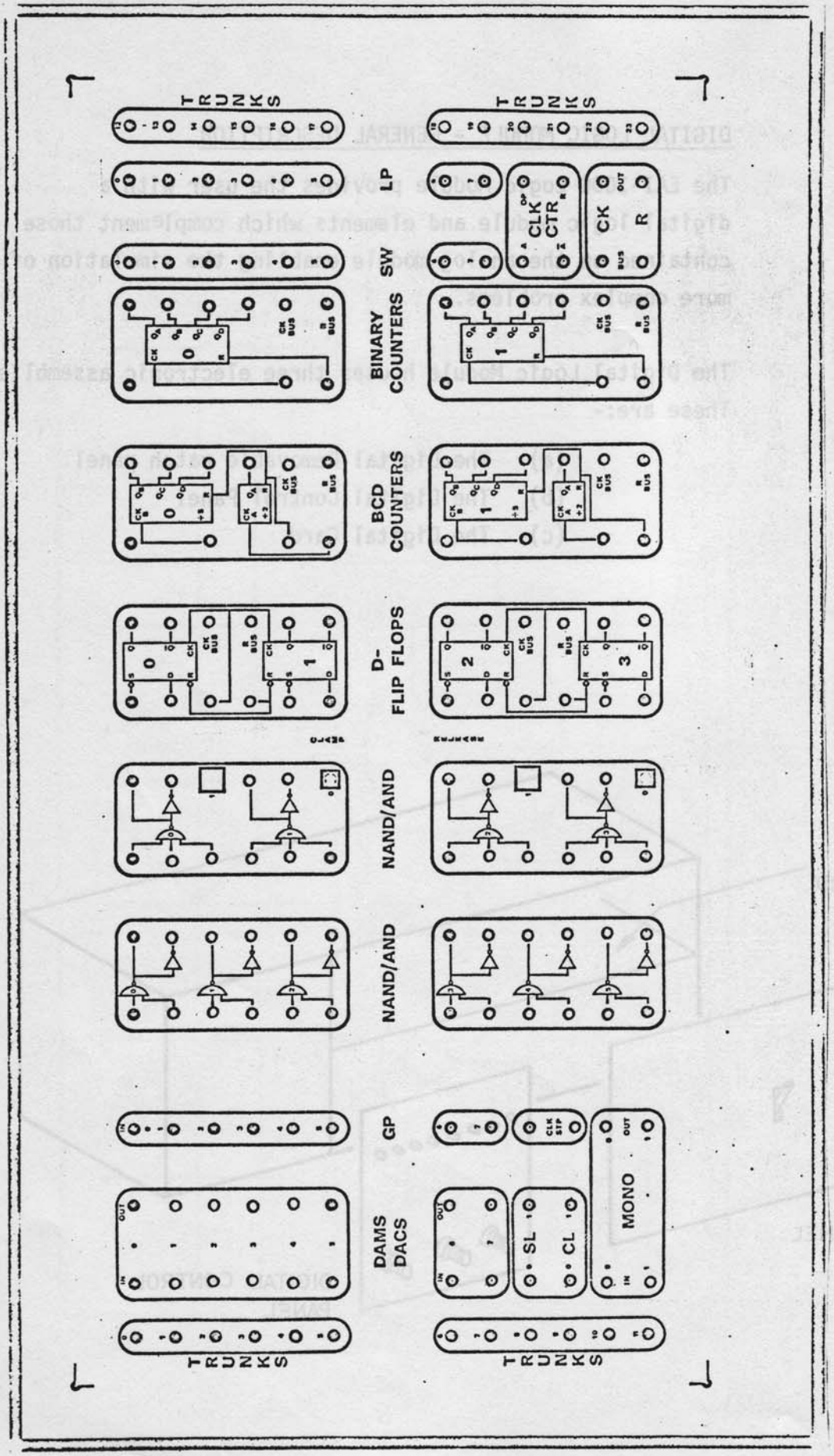
4.1 DIGITAL LOGIC MODULE - GENERAL DESCRIPTION

The EAI-1000 Logic Module provides the user with a digital logic module and elements which complement those contained on the analog module enabling the simulation of more complex problems.

The Digital Logic Module houses three electronic assemblies These are:-

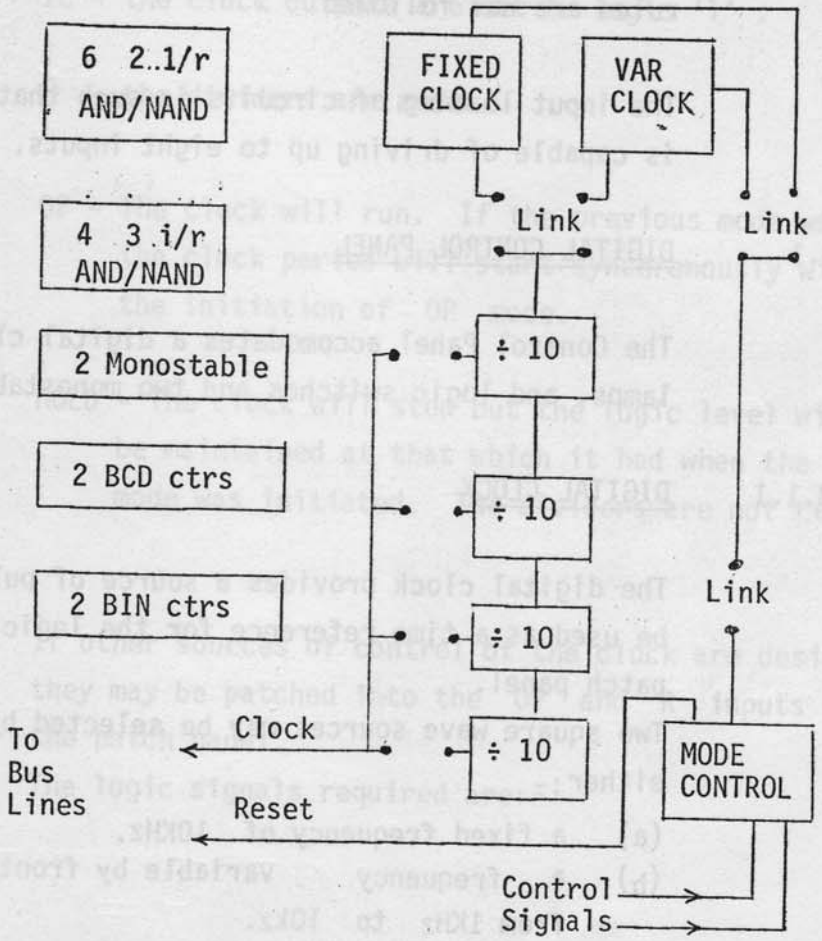
(a) The Digital Removable patch panel
(b) The Digital Control Panel
(c) The Digital Card




TRUNKS
LP
SW
BINARY COUNTERS
BCD COUNTERS
D-FLIP FLOPS
NAND/AND
NAND/AND
GP
DAMS DACS
TRUNKS
TRUNKS
CLK CTR
CK
R
CK BUS
R BUS
SL
CL
MONO
IN
OUT

The patch point connections for all the logic elements are brought out on the removable patch panel. Connections to the analog modules are made via the Universal Trunking System.

4.2 DIGITAL LOGIC MODULE BLOCK DIAGRAM:



4.3 OPERATING PROCEDURES

GENERAL

The circuits used in the digital module are of the TTL type, with an active, not resistive output pull up. Logic "0" is represented by a voltage in the range 0 to 0.8v , and logic '1' by a voltage in the range +2.4 to +5v.

The patch points on this module should not be connected to analog patch points or to any voltage source outside the range 0v to +5v. In addition, two output patch points should not be connected together as if one output attempts to reach logic 1 and the other logic '0' excessive current will flow. Permanent damage may occur if these rules are not followed.

The input loading of circuits is such that each output is capable of driving up to eight inputs.

4.3.1 DIGITAL CONTROL PANEL

The Control Panel accomodates a digital clock, and logic lamps, and logic switches and two monostable controls.

4.3.1.1 DIGITAL CLOCK

The digital clock provides a source of pulses which may be used as a time reference for the logic circuits on the patch panel.
Two square wave sources may be selected by patching, with either:-

(a) a fixed frequency of 10KHz.
(b) a frequency variable by front panel control from 1KHz to 10kz.

In addition the output frequency of the source selected is divided in decades, and access is provided to the decade outputs at 1Hz , 10Hz , 100Hz , and 1kHz with 10kHz input, and down to 0.1Hz with the variable input.

The clock is normally controlled by the mode signals from the Control board. This requires patching A to OP and $\bar{A}$ to R on the digital patch panel.

The condition set by the three modes are:-

IC - the clock outputs are set to logic '1' .

- the dividers are reset.

OP - The clock will run. If the previous mode was IC the clock period will start synchronously with the initiation of OP mode.

HOLD - The clock will stop but the logic level will be maintained at that which it had when the HOLD mode was initiated. The dividers are not reset.

If other sources of control of the clock are desired they may be patched into the OP and R inputs on the patch panel.
The logic signals required are:-

CLOCK STATE	OP	R
IC	1	0
OP	0	1
HOLD	1	1

4.3 1.2 LAMPS

The eight logic indicator lamps are illuminated when logic '1' signal or open circuit is applied to the appropriate patch point on the removable patch panel.

Each lamp is fully buffered to eliminate signal loading.

4.3 1.3 SWITCHES

The eight logic switches generate a logic '1' in the centre position, a logic '0' in the UP position, and momentary logic '0; in the down position. The switches are fully buffered against switch bounce. The switch outputs are available on the patch panel.

4.3 1.4 MONOSTABLE

The monostables generate positive going (logic '1') pulses adjustable in width from 50uS to 250 mS.

Triggering is by a signal at the trigger input (IN) going from logic '1' to logic '0'.

The monostable will not be retriggered by further signals until the timing cycle is completed.

4.3 1.5 LOCAL/REMOTE SWITCH

This switch is a provision for remote hybrid operation of the EAI-1000. For normal operation it should be switched to Local.

4.3 1.6 RESET BUS.

The reset bus line, connected to the various patch points, is controlled by the mode control inputs, by the same circuits as the clock. In the HOLD and OP mode the reset signal is at logic '1' and in the IC mode goes to logic '0'.

4.4 LOGIC ELEMENTS

The removable Patch Panel provides patch points for the following logic elements:-

4.4 1. NAND/AND

The AND/NAND gates are conventional and obey the following truth tables:-

2 1/p Gates

A	B	AND	NAND
0	0	0	0
1	0	0	0
0	1	0	0
1	1	1	0

3 1/p Gates

INPUTS			OUTPUTS	
A	B	C	AND	NAND
0	0	0	0	1
1	0	0	0	1
0	1	0	0	1
1	1	0	0	1
0	0	1	0	1
1	0	1	0	1
0	1	1	0	1
1	1	1	1	0

4.4 2. D. FLIP - FLOP

The D type flip- flops transfer the signal level at the D input to the Q output, when a positive going input edge (logic '0' to '1') is applied to the clock input. No further change will occur to the output until a further positive edge is applied or the set (S) or reset (R) input is taken to logic '0'.

TRUTH TABLES

Dynamic

Input D before clock edge	Output after clock edge	
D	Q	$\bar{Q}$
0	0	1
1	1	0

Static

Input		Output	
S	R	Q	$\bar{Q}$
0	0	1	1
0	1	1	0
1	0	0	1
1	1	No change	

4.4.3. BCD COUNTER

Each counter is an independant counter with 2 sections of $\div 2$ and $\div 5$.

Counting occurs on a negative going edge at the clock input. The counter will be reset by a logic '0' at the R input.

The truth table shows the outputs when Q_A is connected to CPB.

COUNT	OUTPUT			
	Q_D	Q_B	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

If a square wave output is required the input should be connected to CP B , and CP A patched to Q_D. In this case outputs have no binary significance.

4.4 3. BINARY COUNTER

The Binary Counter is a four stage counter. Counting occurs on a negative going edge of the clock input. To reset the counter the R input must be taken to logic '0'.

The truth table shows the signals at the outputs, For two counters connected in series.

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	0
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

MAINTENANCE

SECTION

NOTE: The CMOS integrated circuits used in the EAI 1000 have inbuilt gate protecting diodes preventing damage by static discharge. Normal careful handling will not cause damage.

5. CONSTRUCTION

5.1 CABINET CONSTRUCTION

The dual sized frame construction method utilised by the EAI 1000 provides flexibility and easy addition of expansion frames.

Each frame is attached to the frame above by four screws, with access to these screws being from the underside.

The four removable rubber feet provide access to the set of four screws in the control frame.

All the electronics are accessible from the front of the computer. The maintenance kit (11-100-0005) provides cables, extenders and support brackets for all service requirements. The electronic sub-assemblies are located by means of "POSISCREWS", and "POSIDRIVE" tools are recommended to minimise possible damage to the cabinet, the legend panels and screw heads.

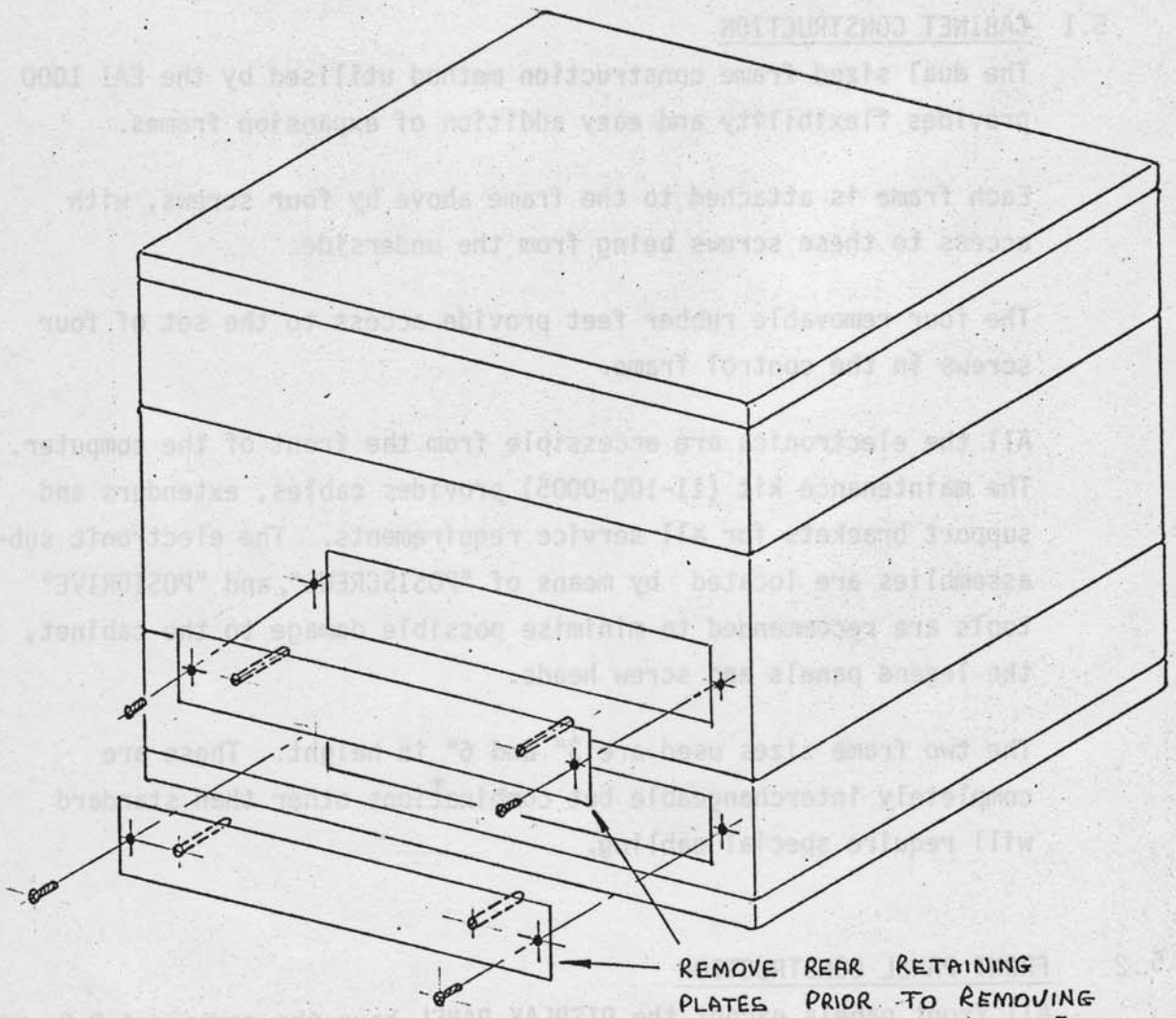
The two frame sizes used are 3" and 6" in height. These are completely interchangeable but combinations other than standard will require special cabling.

5.2 FRONT PANEL CONSTRUCTION

All front panels except the DISPLAY PANEL have the component P.C. card bonded to the Legend decal. The components mounted on these P.C. cards are few and not subject to stress (electrical, mechanical or thermal). Failure of these components is considered to be unlikely. In such an event however, it is recommended that the faulty component be cut from the component side of the P.C. card and a replacement component soldered directly to the cut leads of the component ON THE COMPONENT SIDE OF THE P.C. CARD.

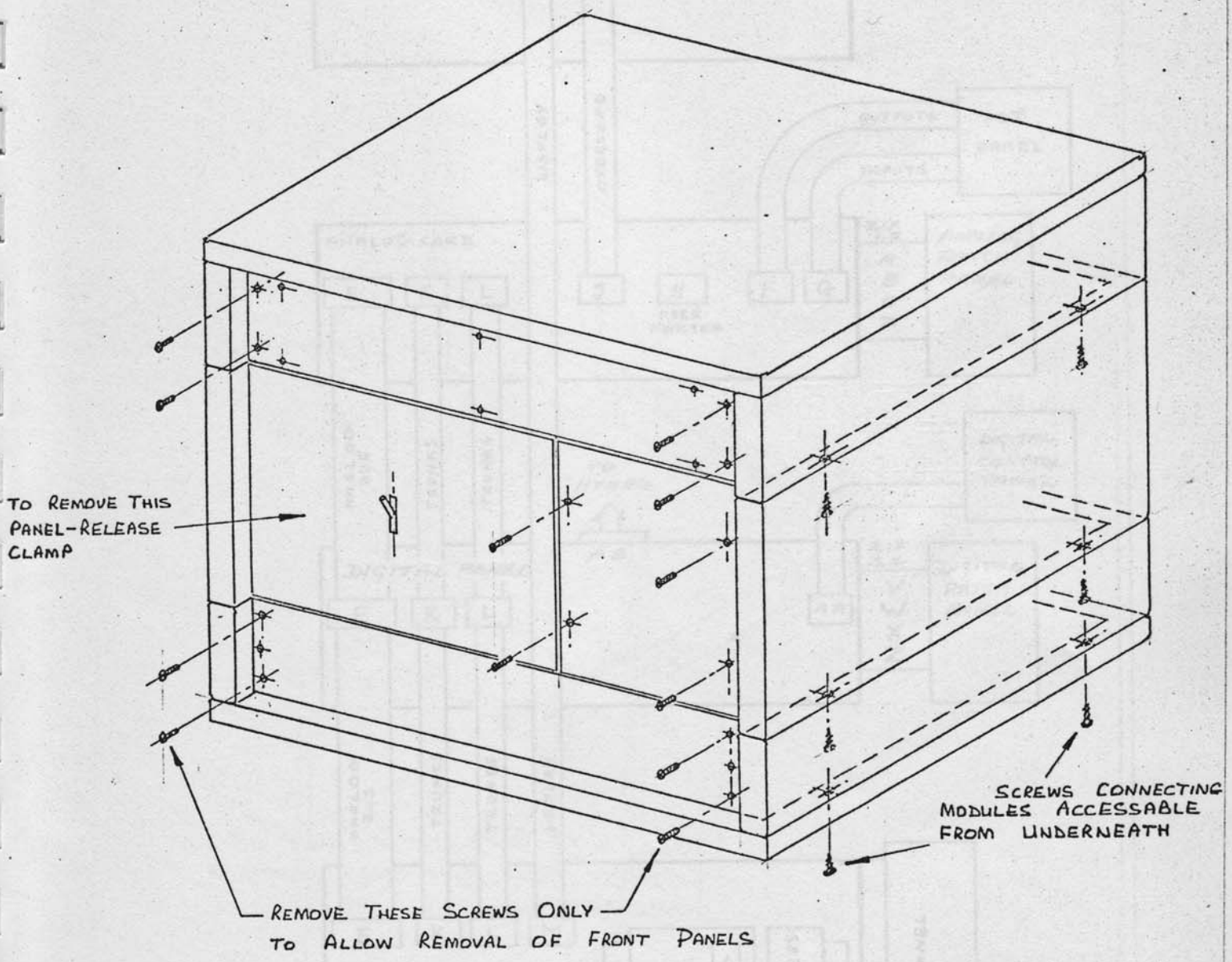
5.3 INTER PANEL CABLING

All interpanel cabling is accomplished by means of 3 sizes of flat strip cable and associated connectors. These are 40 way, 26 way and 16 way. Access to the connectors is via rear panel openings and from the front



REAR VIEW OF EAI-1000

FIGURE 5.1



FRONT VIEW OF EAI-1000

FIGURE 5.2

The drawing (Fig 5.3.1.) details the interconnections for the maximum system expansion. For smaller systems the cable routing is unchanged other than that the omitted frames and associated electronics do not connect into the system.

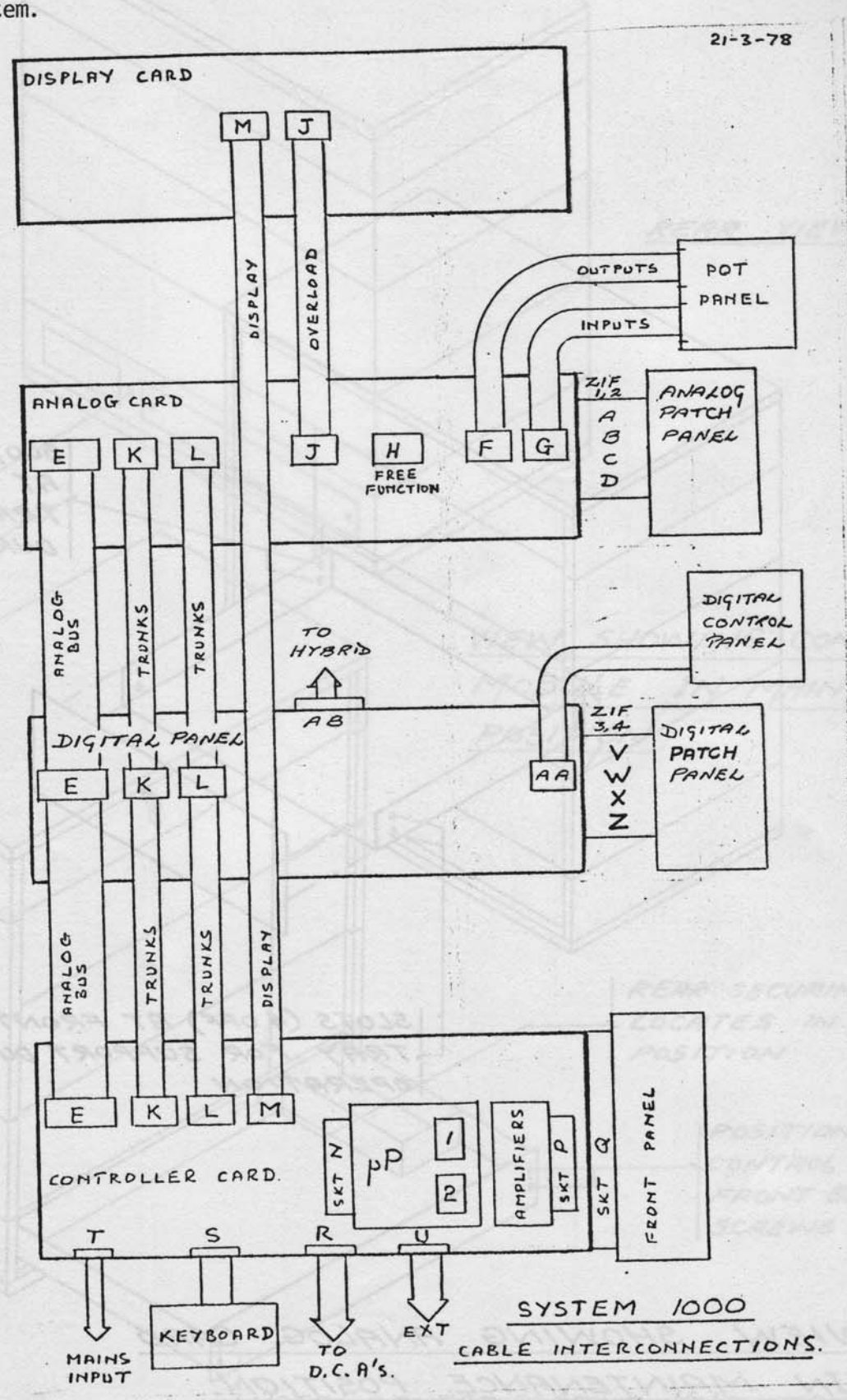
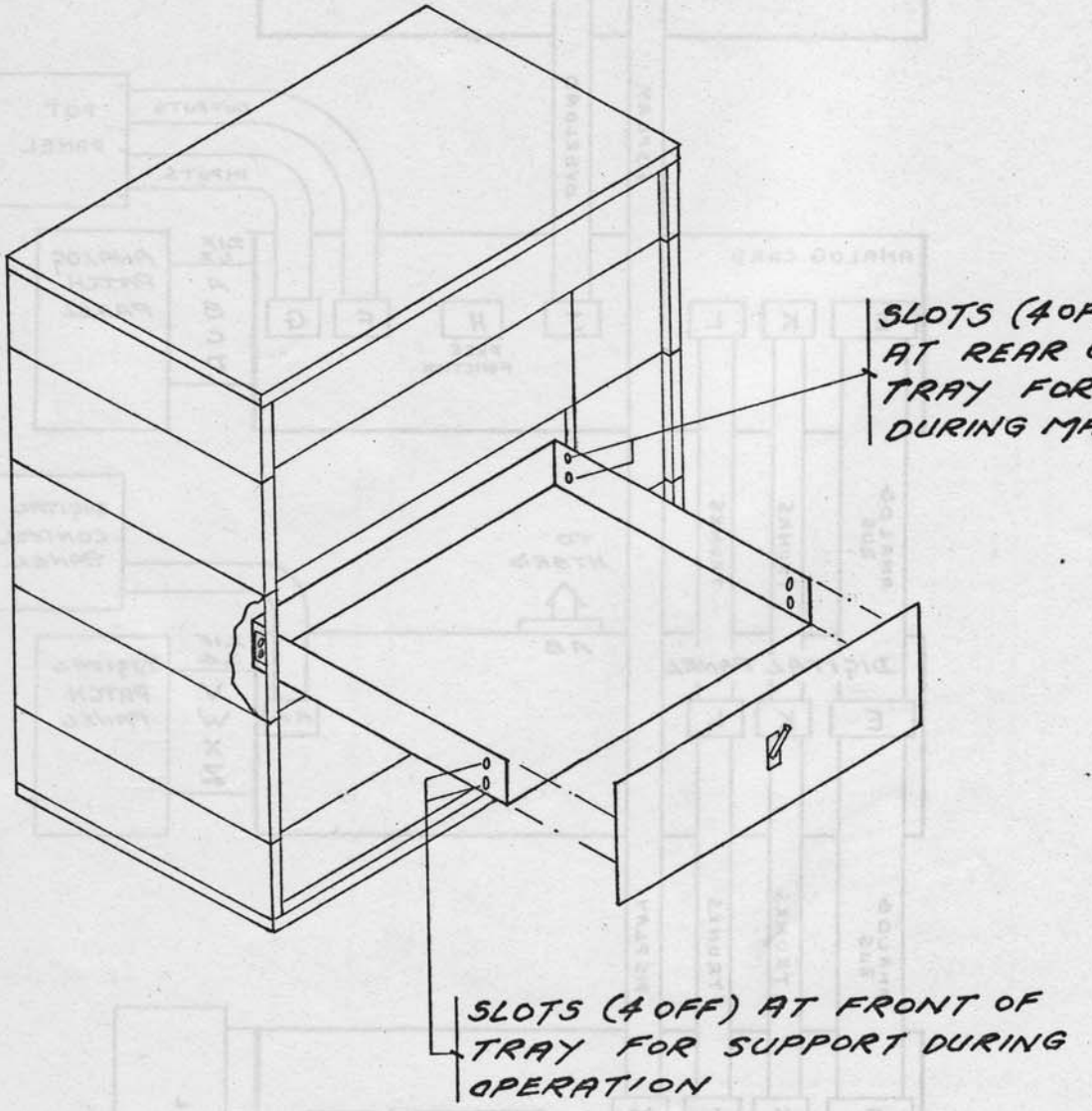
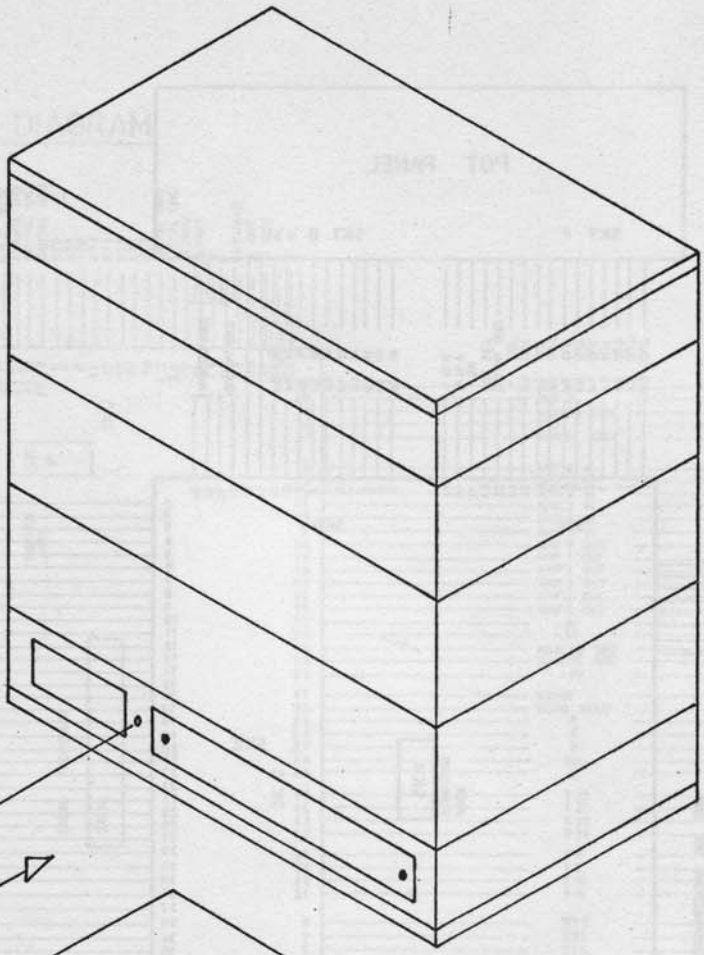


FIGURE 5.3.1. A



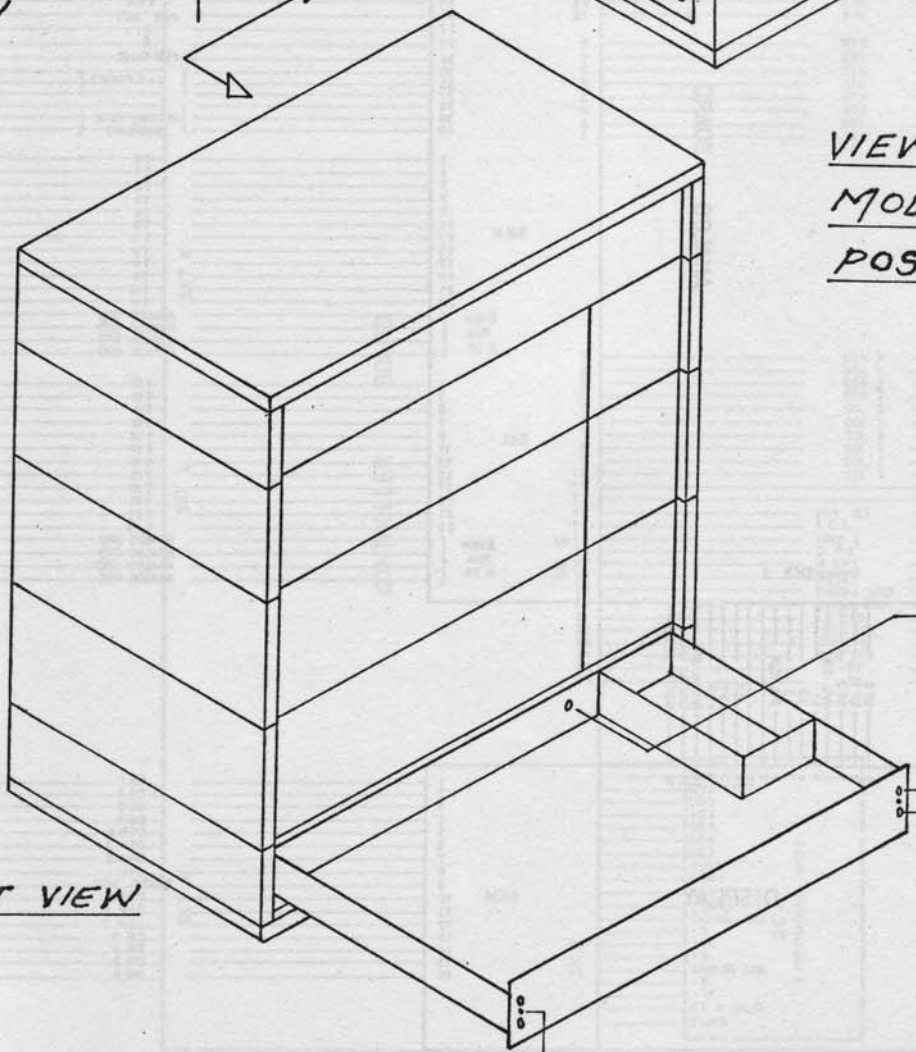
VIEW SHOWING ANALOG CARD IN MAINTENANCE POSITION.



REAR VIEW

POSITION OF
ONTROL MODULE
REAR SECURING
SCREW

VIEW SHOWING CONTROL
MODULE IN MAINTENAN
POSITION



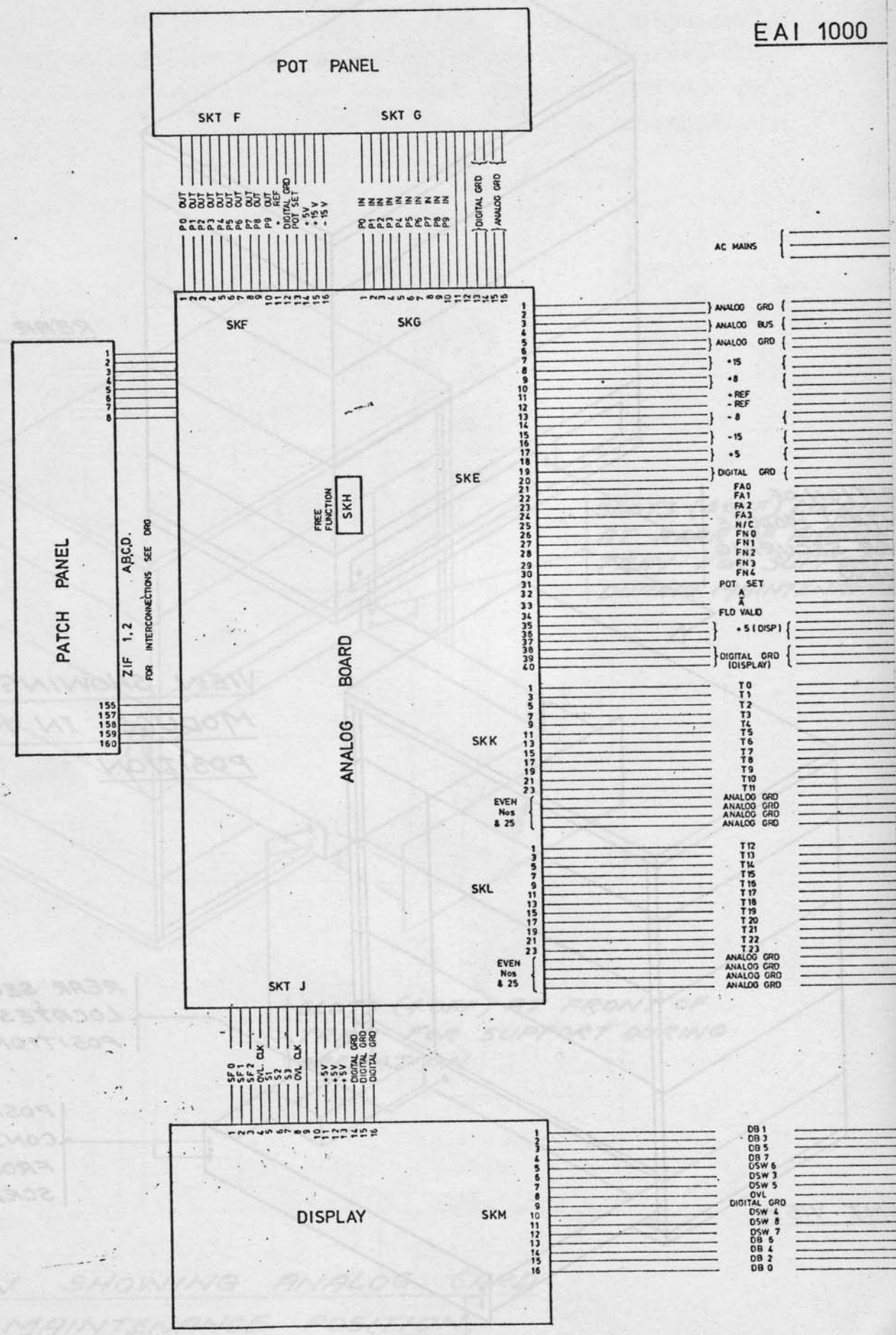
REAR SECURING SCRE
LOCATES IN THIS
POSITION

POSITION OF
CONTROL MODUL
FRONT SECURIN
SCREWS (4 OFF)

RONT VIEW

NOTE! CENTRE SCREWS HOLD FRONT
PANEL TO CONTROL CARD
DO NOT REMOVE

EAI 1000


POT PANEL
SKT F
SKT G
P0 OUT
P1 OUT
P2 OUT
P3 OUT
P4 OUT
P5 OUT
P6 OUT
P7 OUT
P8 OUT
P9 OUT
REF
DIGITAL GRD
POT SET
+5V
+15 V
-15 V
P0 IN
P1 IN
P2 IN
P3 IN
P4 IN
P5 IN
P6 IN
P7 IN
P8 IN
P9 IN
DIGITAL GRD
ANALOG GRD
AC MAINS
SKF
SKG
SKE
SKH
FREE FUNCTION
PATCH PANEL
ZIF 1,2
A,B,C,D.
FOR INTERCONNECTIONS SEE DRG
ANALOG BOARD
ANALOG GRD
ANALOG BUS
ANALOG GRD
+15
+8
+REF
-REF
-8
-15
+5
DIGITAL GRD
FA0
FA1
FA2
FA3
N/C
FN0
FN1
FN2
FN3
FN4
POT SET
A
X
FLD VALID
+5 (DISP)
DIGITAL GRD (DISPLAY)
SKK
T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
EVEN Nos & 25
ANALOG GRD
SKL
T12
T13
T14
T15
T16
T17
T18
T19
T20
T21
T22
T23
SKT J
SF 0
SF 1
SF 2
OVL CLK
S1
S2
S3
OVL CLK
+5V
DIGITAL GRD
DISPLAY
SKM
DB 1
DB 3
DB 5
DB 7
DSW 6
DSW 3
DSW 5
OVL
DSW 4
DSW 8
DSW 7
DB 6
DB 4
DB 2
DB 0

INTERCONNECTION DIAGRAM

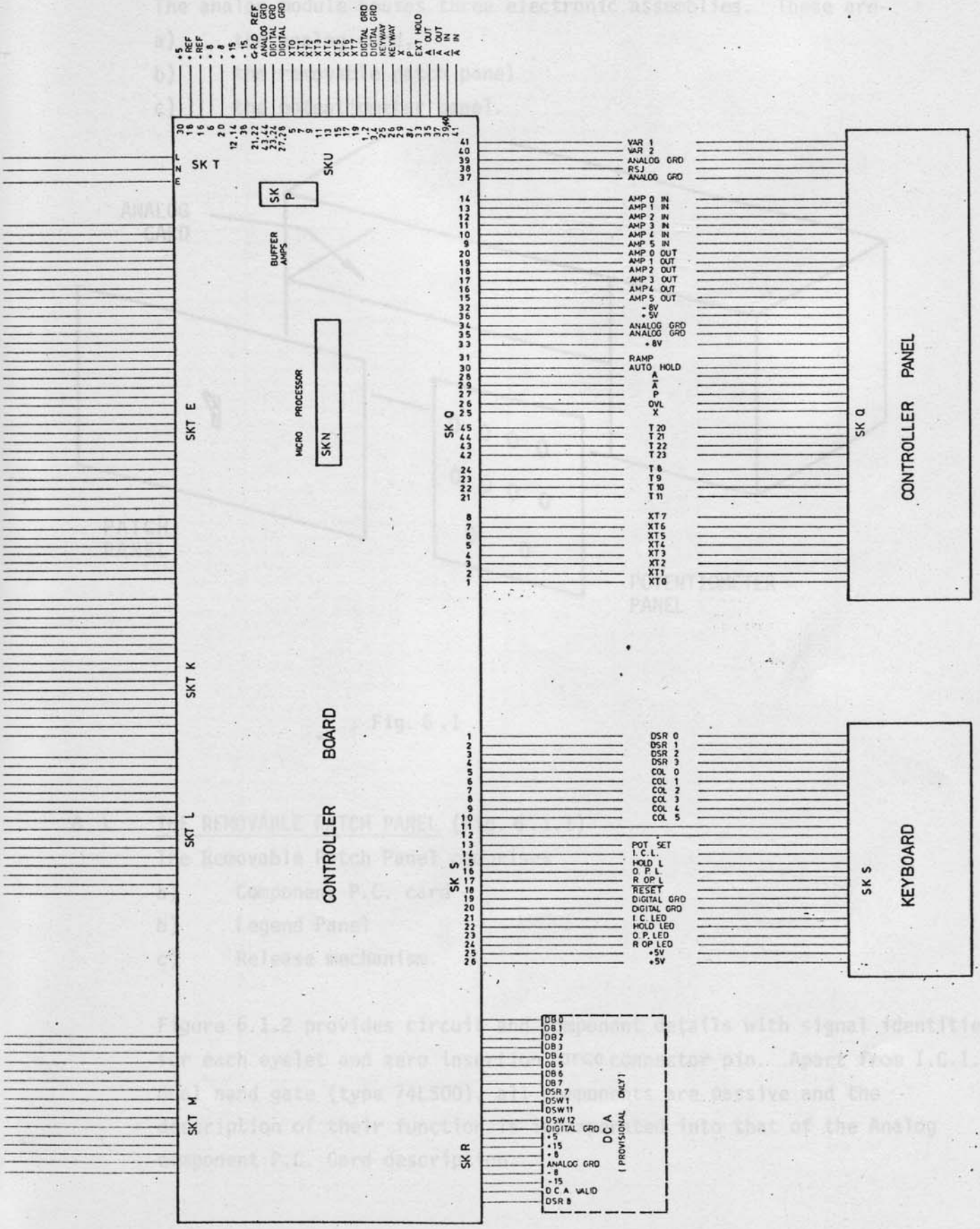


FIG. 5.3.1 B

CHAPTER 6

6. THE ANALOG MODULE

The analog module houses three electronic assemblies. These are-

a) the analog card,

b) the removable patch panel

c) the potentiometer panel.

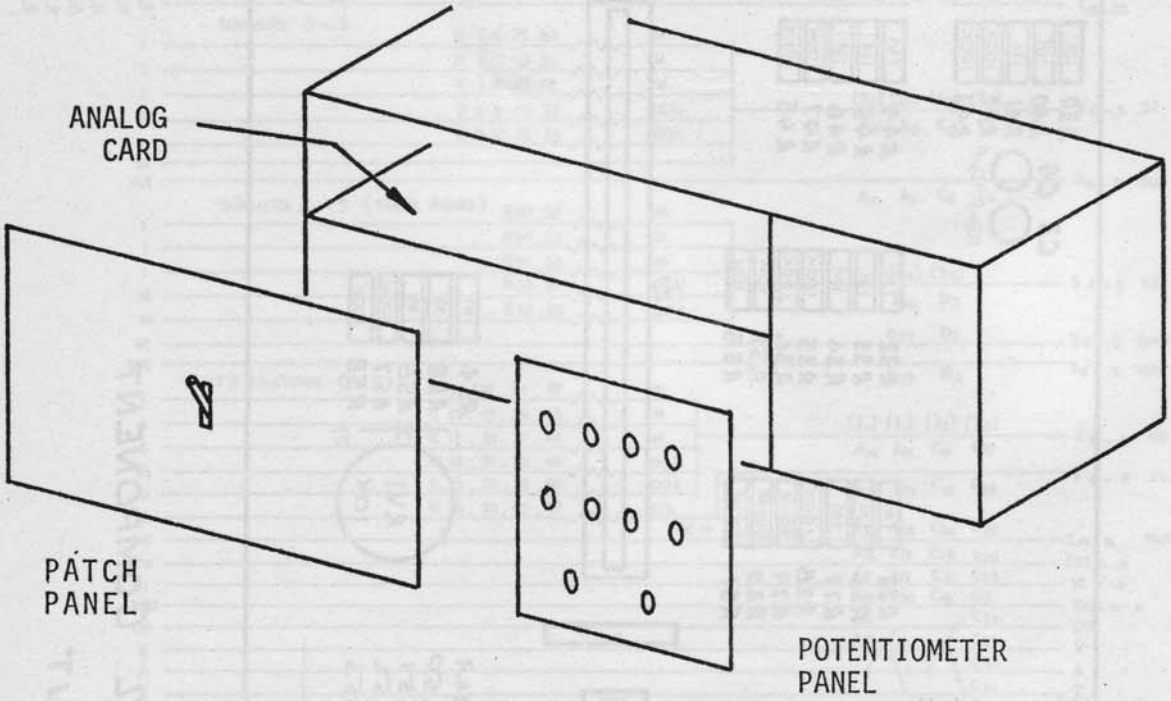


Fig. 6.1

6.1 THE REMOVABLE PATCH PANEL (Fig. 6.1.1)

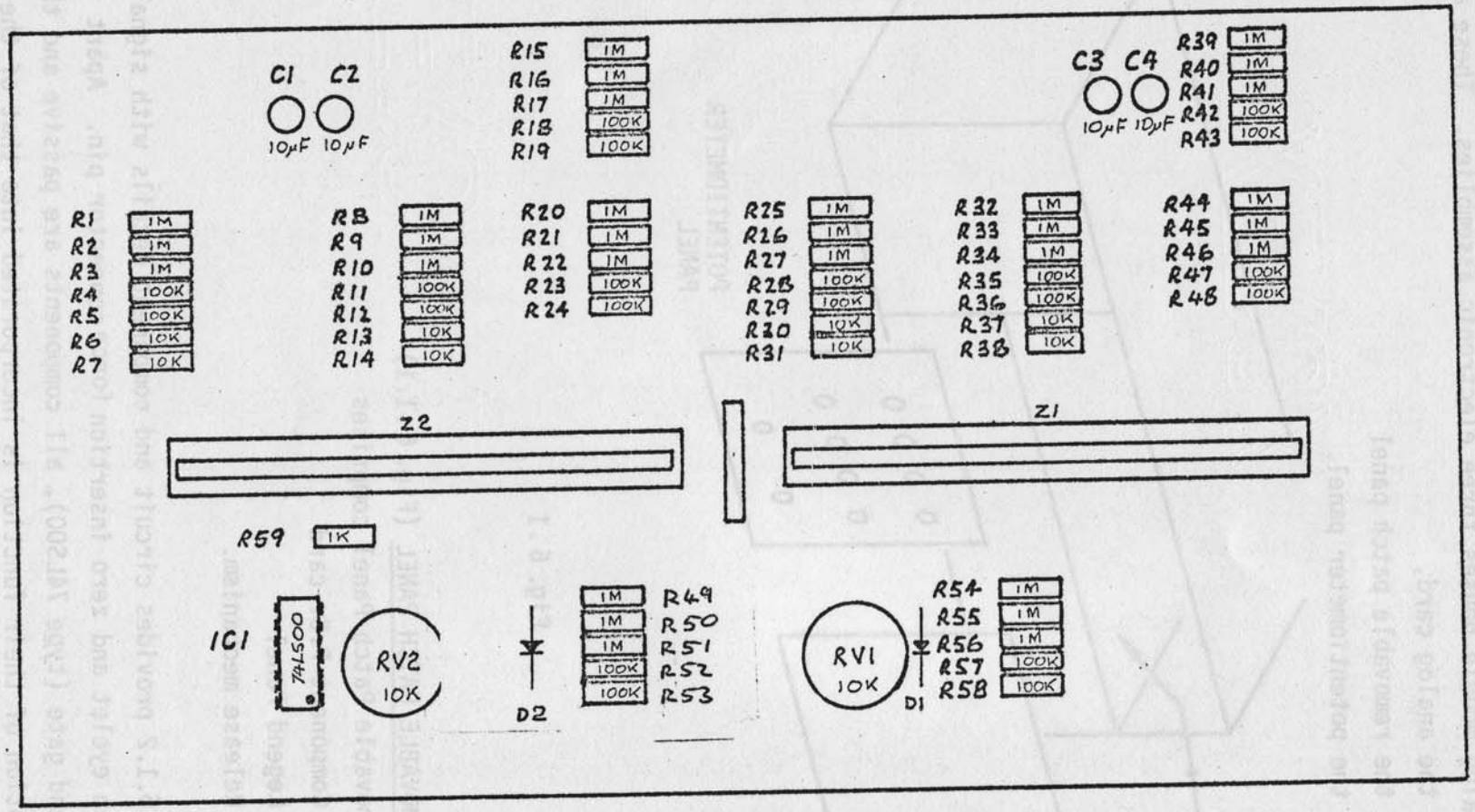
The Removable Patch Panel comprises

a) Component P.C. card

b) Legend Panel

c) Release mechanism.

Figure 6.1.2 provides circuit and component details with signal identities for each eyelet and zero insertion force connector pin. Apart from I.C.I., dual nand gate (type 74LS00), all components are passive and the description of their function is incorporated into that of the Analog component P.C. Card description.



PATCH PANEL COMPONENT LAYOUT

FIG 6.1.1.

REMOVEABLE PATCH PANEL

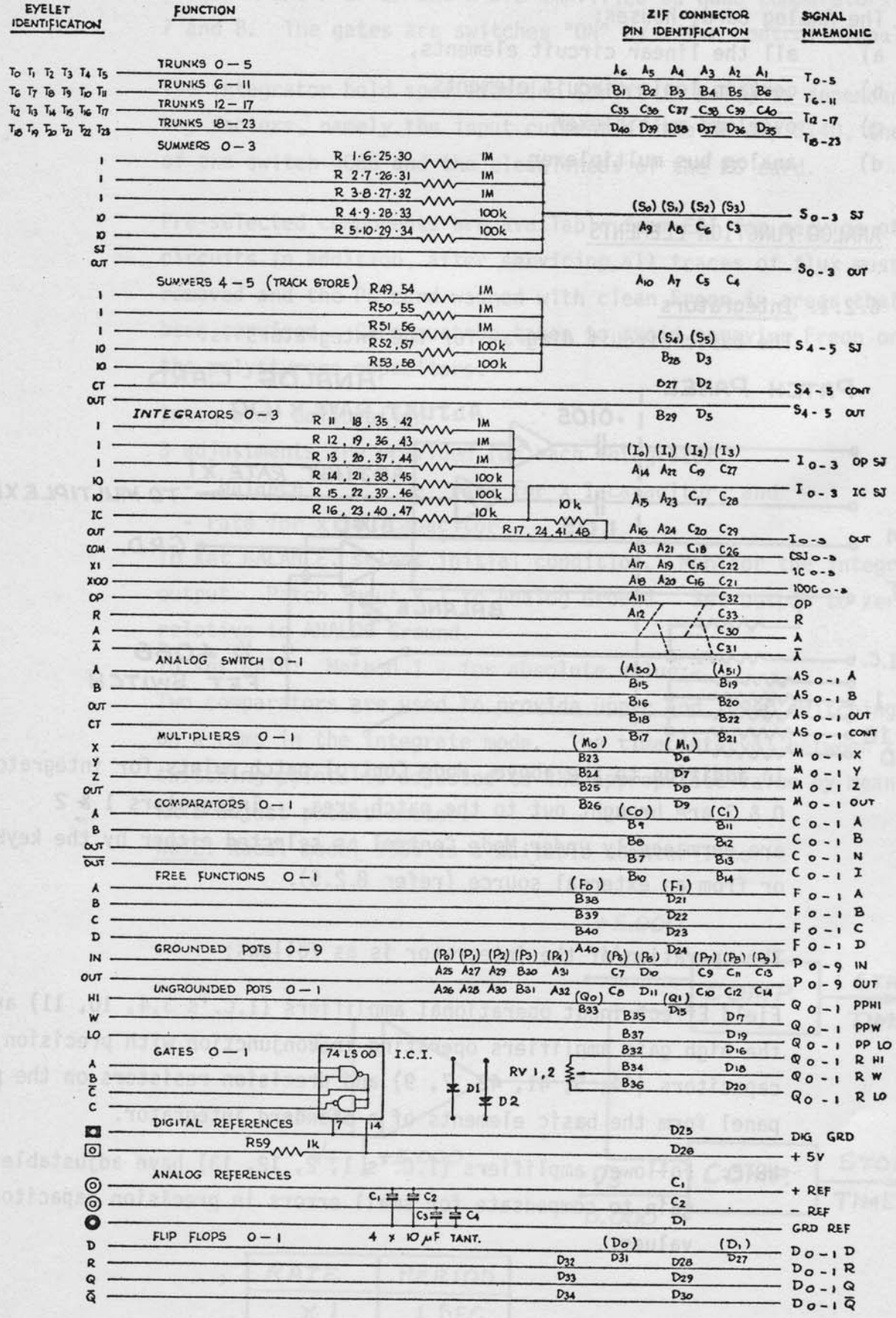


Fig. 6.1.2

6.2 THE ANALOG CARD (Figs. 6.2.1, 6.2.2., 6.2.3)

The Analog Card, houses:

a) all the linear circuit elements,

b) certain logic circuit elements

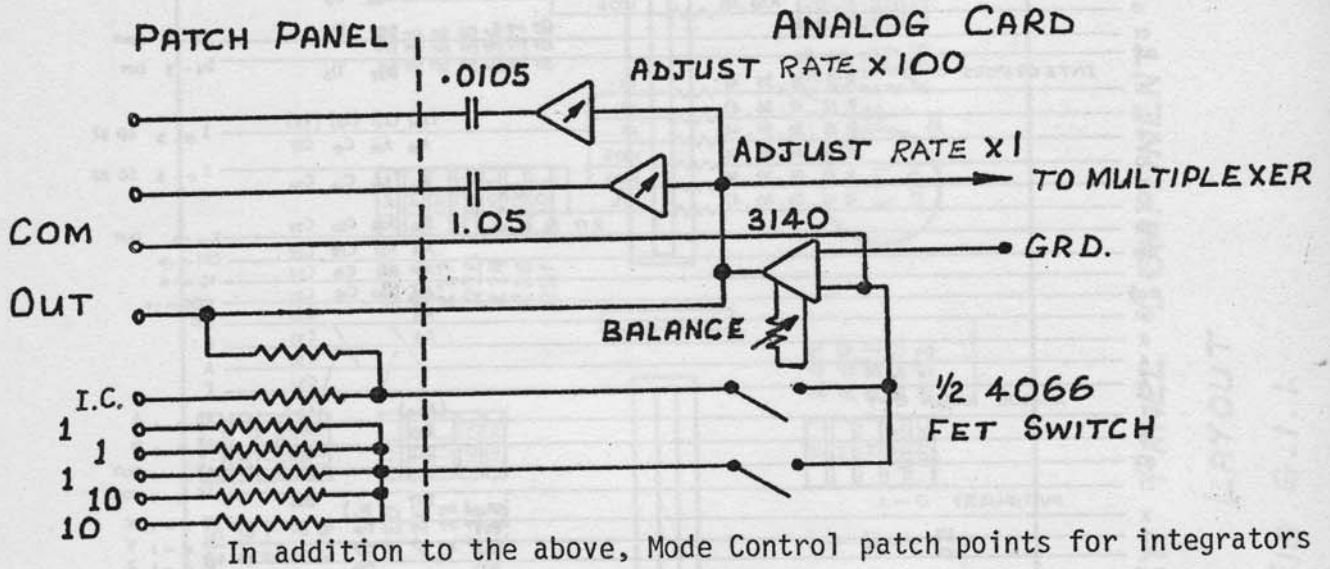
c) overload multiplexer

d) analog bus multiplexer.

ANALOG FUNCTION ELEMENTS

6.2.1. Integrators

The basic circuit diagram for the integrators is:



In addition to the above, Mode Control patch points for integrators 0 & 3 are brought out to the patch area. Integrators 1 & 2 are permanently under Mode Control as selected either by the keyboard or from an external source (refer 8.2.5).

The operation of the integrator is as follows:

Field Effect input operational amplifiers (I.C.'s 3,4, 10, 11) are the high gain amplifiers operating in conjunction with precision capacitors (C4, 5, 41, 42, 7, 9) and precision resistors on the patch panel form the basic elements of a standard integrator.

NOTE: Follower amplifiers (I.C.'s 1, 2, 12, 13) have adjustable gain to compensate for small errors in precision capacitor values.

The appropriate summing junction is gated to the Op-amp inputs by IC's 5 and 6 (Quad bilateral electronic switches). Logic control signals - either A and $\overline{A}$ or OP and R are amplified bu quad comparators IC's 7 and 8. The gates are switches "ON" by a +ve control signal of +8v.

The integrator hold specification (drift in hold) is dependant on 3 key factors, namely the input current of the OP-amp 3140, the leakage of the switch 4066 and the cleanliness of the PC card.

Pre-selected components are available from EAI for service of these circuits. In addition, after servicing, all traces of flux must be removed and the PC card washed with clean Freon in areas that have been serviced. Care must be taken to avoid spraying Freon on to the polystyrene capacitors.

Integrator Calibration

3 adjustments are provided for each integrator:

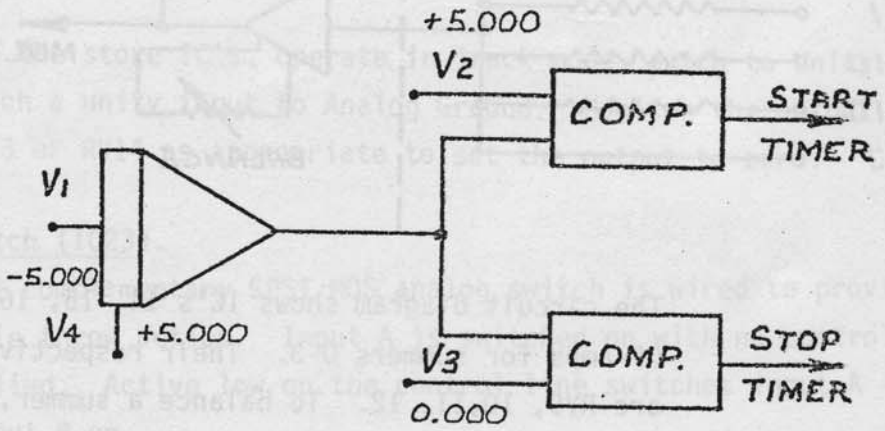
- balance
- rate for x 1 capacitor, and
- rate for x 100 capacitor

To set BALANCE, select initial condition. Monitor the integrator output. Patch input x 1 to Analog Ground. Set output to zero volts relative to ANALOG Ground.

To set RATE: Method 1 - for absolute value:-

Two comparators are used to provide upper and lower switching points on a ramp in the integrate mode. The time interval between the switching points is adjusted to the appropriate value by means of the RATE adjust potentiometer.

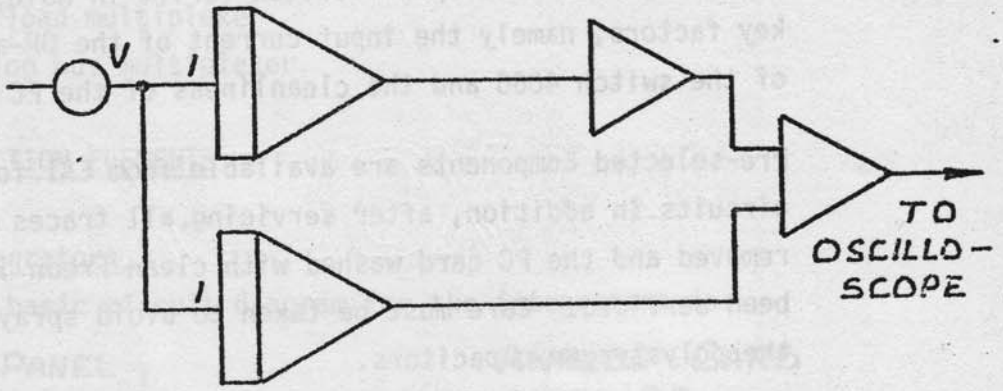
NOTE: Racal model 9905 is a suitable counter-Timer.



RATE	PERIOD
X 1	1 SEC.
X 100	0.01 SEC.

Method 2. For relative setting

Where a check of integration rate relative to other integrators is required, patch is shown below.

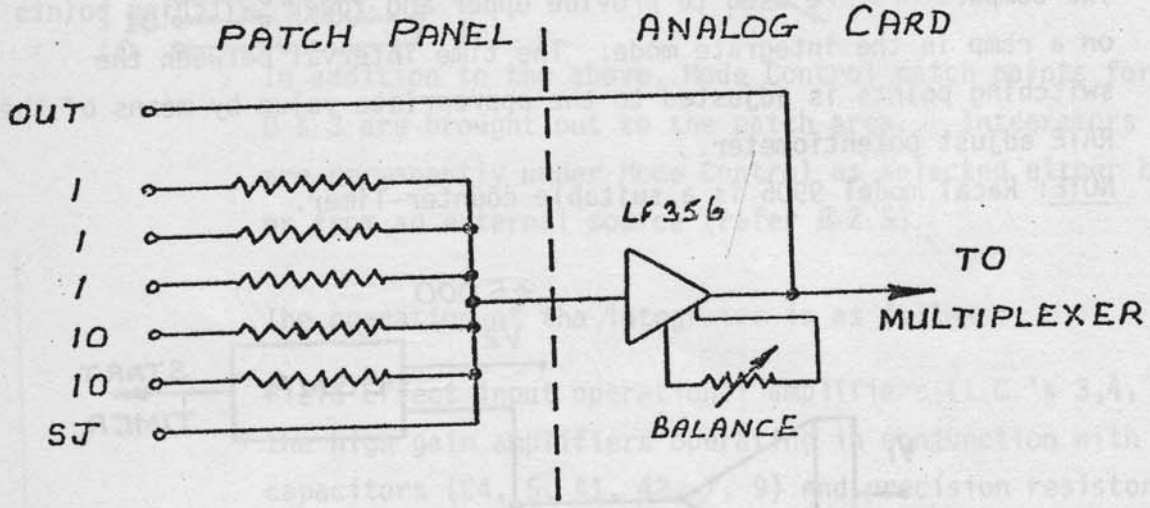


Set v to .500 volts.

Monitor the summer output on an oscilloscope. Set the Rate Adjust potentiometer of each slave integrator to give zero signal.

6.2.2. Summers 0-3

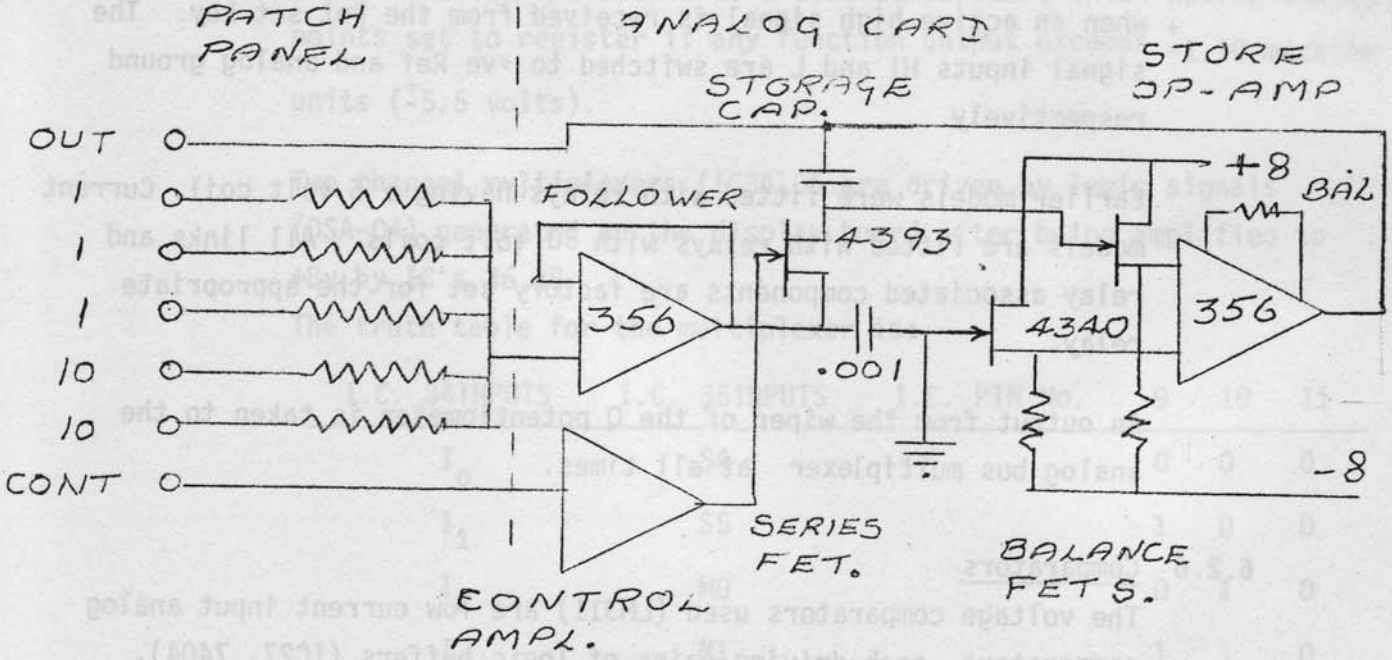
The basic circuit diagram for the summers 0-3 is:



The circuit diagram shows IC's 14, 15, 16, 17 are the F.E.T. OP-amps for summers 0-3. Their respective balance potentiometers are RV9, 10,11, 12. To balance a summer, patch for unity gain. Connect a Unity gain input to Analog ground. Monitor the output adjust the appropriate balance potentiometer to give zero volts at the summer output.

6.2.3 Summers 4,5 (Summer Track/Store

The basic circuit diagram is:



The summing followers IC's 18,20 reduce the impedance of the summing junction. During summing operation the store IC's 19,21 retain a charge across capacitors C19 and 22 equal to the signal voltage. When switches TR1, TR2 are opened, incoming signals are blocked. The Store IC's retain an output voltage from the Store capacitor equal to signal at the instant of the switch opening.

The series FET (2N4393) is selected for low leakage. The two input FET's (2N4340) are selected as a matched pair to balance the input currents of the output OP-AMP (LF356). Pre-selected components are available from EAI for service of these areas.

To balance the store IC's, operate in track mode, patch to Unity gain. Patch a unity input to Analog Ground. Monitor the output and adjust RV13 or RV14 as appropriate to set the output to zero.

6.2.4 Analog Switch (IC23).

A twin dual complementary SPST MOS analog switch is wired to provide dual, double throw action. Input A is switched on with no control signal applied. Active low on the control line switches input A off and input B on.

No adjustments can be made to these functional elements.

6.2.5 Q Potentiometers

A four pole changeover relay RLAI is energised by transistor TR3 when an active high signal is received from the Pot set key. The signal inputs H1 and L are switched to +ve Ref and analog ground respectively.

Earlier models were fitted with relays having a 5 volt coil. Current models are fitted with relays with 30 volt coils. All links and relay associated components are factory set for the appropriate relay.

An output from the wiper of the Q potentiometer is taken to the analog bus multiplexer at all times.

6.2.6 Comparators

The voltage comparators used (LM311) are low current input analog comparators, each driving pairs of logic buffers (IC27, 7404), providing true and inverted outputs. Hysterysis is provided by feedback resistors.

6.2.7 Flip Flop

A single dual D Flip Flop IC30, 7474, provides the Flip Flop functions.

6.2.8 Power Supply Buffers

The power lines +15, -15, +8, -8, +5 and digital ground are brought in via the 40-way bus and distributed.

To prevent any loading on the REFERENCE supplies and to eliminate voltage drops on distribution lines, +ve Ref, -ve Ref and ANALOG GROUND are buffered by IC's 24,25,26 respectively. Buffering is provided by operational amplifiers operating in the follower mode.

6.2.9 Multipliers

The multiplier module used is the AD534JH 4-quadrant multplier.
The procedure for checking accuracy of set up is as follows:

a) Set Zero with X and Y input at zero
b) Set Balance for equal readings with 2 +ve Ref inputs comparing with 2 -ve inputs.
c) Set Gain such that all readings are within six digits of full-scale for all four reference input combinations.
d) Repeat steps a) to c)

The Multiplier is now set for Multiply and Divide modes.

6.2.10 Overload

The overload system (FIG 6.2.3) operates by multiplexing the outputs of 14 functional elements to a dual comparator, which has switching points set to register if any function output exceeds $\pm$1.10 machine units ($\pm$5.5 volts).

Two channel multiplexers (IC34,35 are driven by logic signals (OSA-04) generated on the display board after being amplified to +8v by IC's 36,38.

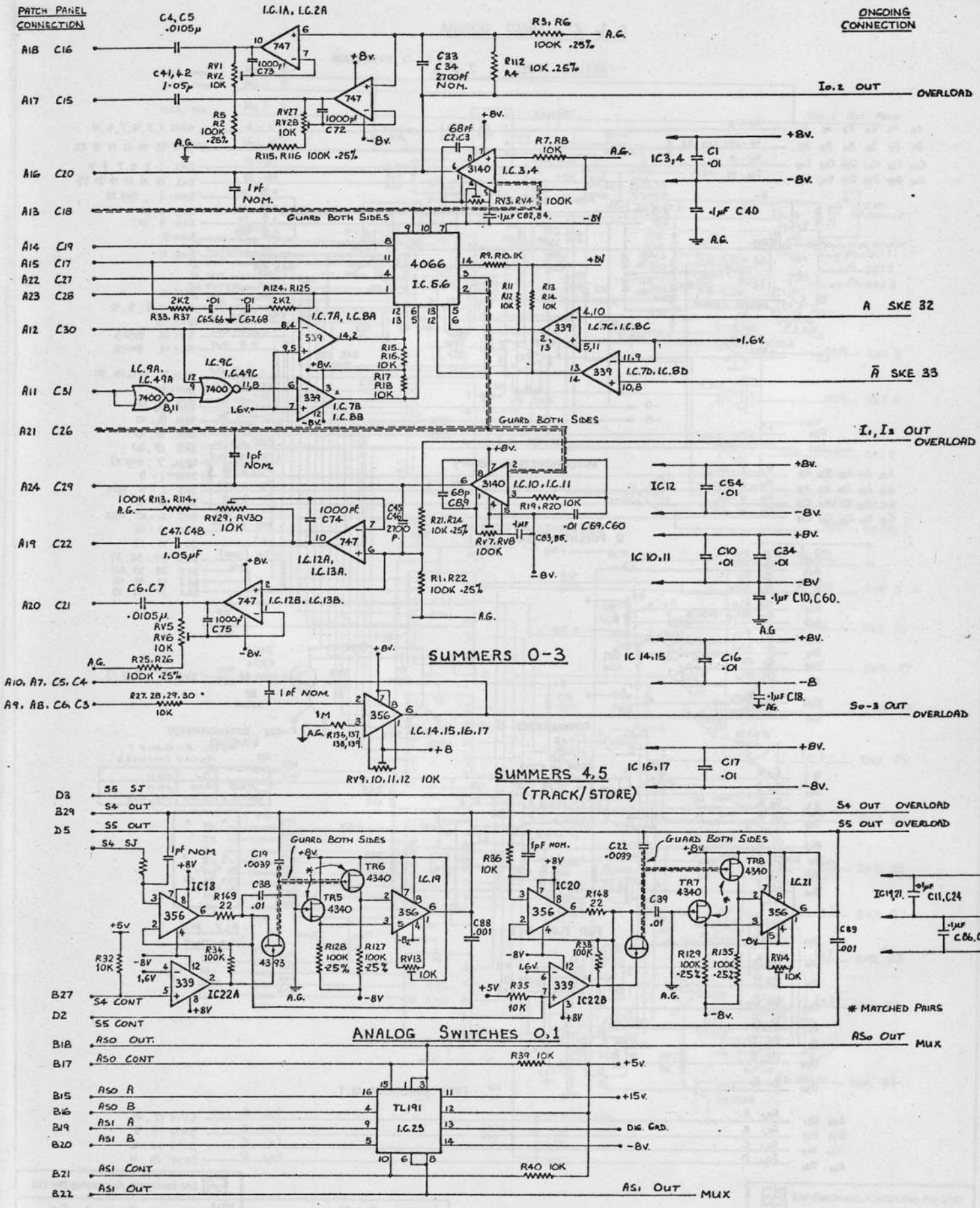
The truth table for the multiplexer is:

I.C. 34INPUTS	I.C. 35INPUTS	I.C. PIN No.	9	10	11
I_o	S4		0	0	0
I_1	S5		1	0	0
I_2	M0		0	1	0
I_3	M1		1	1	0
S_o	F0		0	0	1
S_1	F1		1	0	1
S_2	N/C		0	1	1
S_3	N/C		1	1	1
OSA3	OSA4		OSA0	OSA1	OSA2

When the system is patched to set MODE in "hold" when an overload occurs, the comparator switching voltages are lowered by 50mV by IC51 (4016) to ensure that the system remains in a stable HOLD condition.

NOTE: The Field selector for the overload output signal must be set to the number of the field allocated to the analog card. This is done by the digiswitch on the analog card.

NOTE: Ref Dwg 11-045-001 R3 SH1. Where RCA 3140 fitted in summers - IC's 14-21. Balance pot goes to -ve supply, compensation capacitor fitted and 68 ohm resistor fitted in series with output.



DRG. Nº 11-045-0001 OS REV 3

(1 OF 3)

UPDATED 27/6/79 C.M.
UPDATED 23/8/79 S.R.

FIG. 6.2.1.

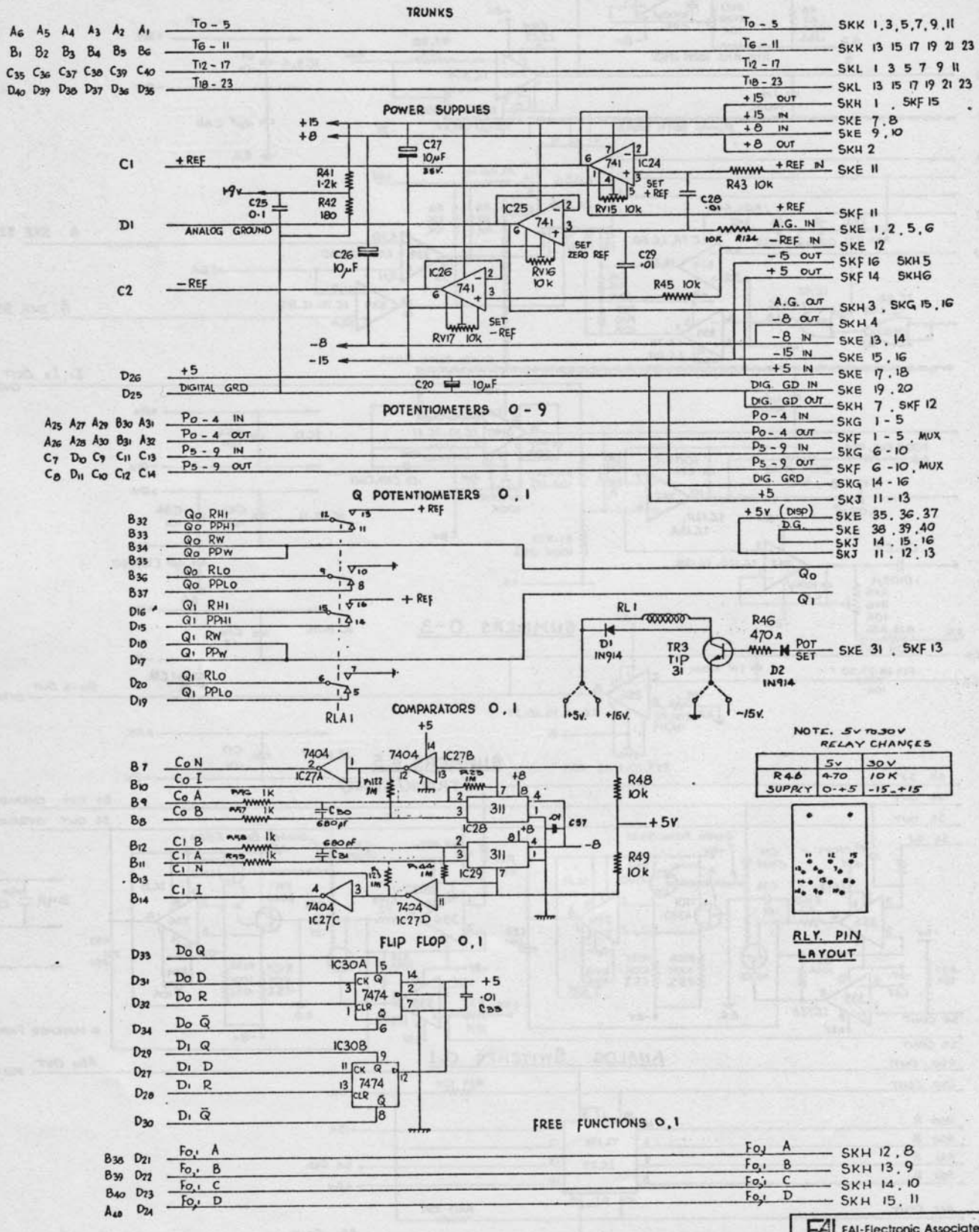
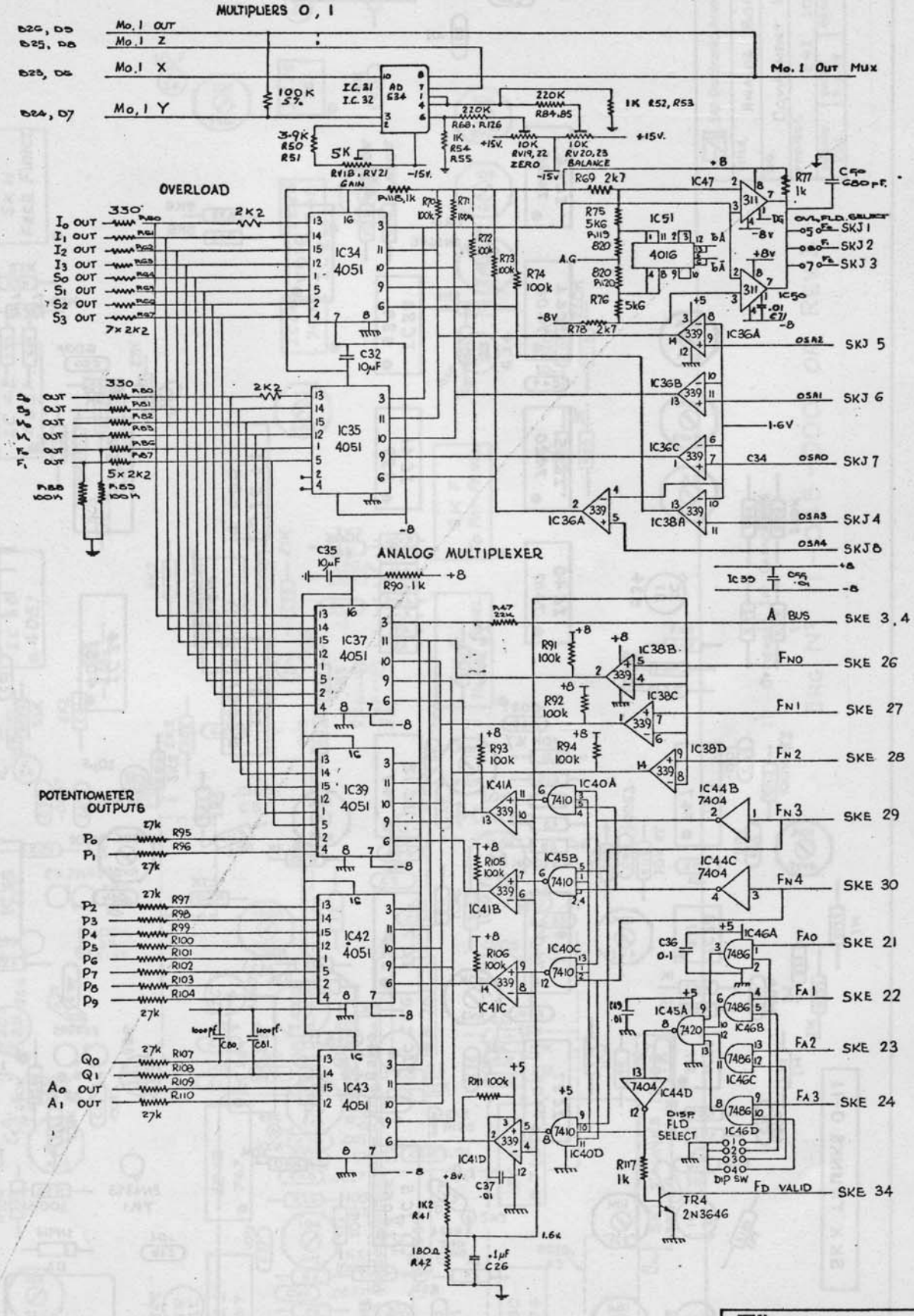

ANALOG PANEL 2 of 3
TRUNKS
A6 A5 A4 A3 A2 A1 To - 5
B1 B2 B3 B4 B5 B6 T6 - 11
C35 C36 C37 C38 C39 C40 T12 - 17
D40 D39 D38 D37 D36 D35 T18 - 23
To - 5 SKK 1,3,5,7,9,11
T6 - 11 SKK 13 15 17 19 21 23
T12 - 17 SKL 1 3 5 7 9 11
T18 - 23 SKL 13 15 17 19 21 23
POWER SUPPLIES
+15 OUT SKH 1 . SKF 15
+15 IN SKE 7,8
+8 IN SKE 9,10
+8 OUT SKH 2
+REF IN SKE 11
C1 +REF
D1 ANALOG GROUND
C2 -REF
D26 +5
D25 DIGITAL GRD
C27 10µF 35V.
R41 1·2k
R42 180
C25 0·1
C26 10µF
C20 10µF
IC24 741
IC25 741
IC26 741
RV15 10k
RV16 10k
RV17 10k
R43 10k
C28 ·01
C29 ·01
R45 10k
SET +REF
SET ZERO REF
SET -REF
+REF SKF 11
A.G. IN SKE 1,2,5,6
-REF IN SKE 12
-15 OUT SKF 16 SKH 5
+5 OUT SKF 14 SKH 6
A.G. OUT SKH 3 . SKG 15,16
-8 OUT SKH 4
-8 IN SKE 13,14
-15 IN SKE 15,16
+5 IN SKE 17,18
DIG. GD IN SKE 19,20
DIG. GD OUT SKH 7 . SKF 12
POTENTIOMETERS 0 - 9
A25 A27 A29 B30 A31 Po - 4 IN
A26 A28 A30 B31 A32 Po - 4 OUT
C7 D10 C9 C11 C13 P5 - 9 IN
C8 D11 C10 C12 C14 P5 - 9 OUT
Po - 4 IN SKG 1 - 5
Po - 4 OUT SKF 1 - 5 . MUX
P5 - 9 IN SKG 6 - 10
P5 - 9 OUT SKF 6 - 10 . MUX
DIG. GRD SKG 14 - 16
+5 SKJ 11 - 13
+5V (DISP) SKE 35,36,37
D.G. SKE 38,39,40
SKJ 14,15,16
SKJ 11,12,13
Q POTENTIOMETERS 0,1
B32 Qo RH1
B33 Qo PPH1
B34 Qo RW
B35 Qo PPW
B36 Qo RLO
B37 Qo PPLO
D16 Q1 RH1
D15 Q1 PPH1
D18 Q1 RW
D17 Q1 PPW
D20 Q1 RLO
D19 Q1 PPLO
RLA 1
+REF
Qo
Q1
RL 1
D1 IN914
D2 IN914
TR3 TIP 31
R46 470Ω
POT SET
SKE 31 . SKF 13
+5V.
+15V.
-15V.
COMPARATORS 0,1
B7 Co N
B10 Co I
B9 Co A
B8 Co B
B12 C1 B
B11 C1 A
B13 C1 N
B14 C1 I
7404 IC27A
7404 IC27B
7404 IC27C
7424 IC27D
311 IC28
311 IC29
R48 10k
R49 10k
+5V
-8
NOTE. 5V TO 30V RELAY CHANGES
5V 30V
R46 470 10K
SUPPLY 0-+5 -15-+15
RLY. PIN LAYOUT
FLIP FLOP 0,1
D33 Do Q
D31 Do D
D32 Do R
D34 Do Q̄
D29 D1 Q
D27 D1 D
D28 D1 R
D30 D1 Q̄
IC30A 7474
IC30B 7474
CK Q CLR Q̄
FREE FUNCTIONS 0,1
B36 D21 Fo,1 A
B39 D22 Fo,1 B
B40 D23 Fo,1 C
A40 D24 Fo,1 D
Fo,1 A SKH 12,8
Fo,1 B SKH 13,9
Fo,1 C SKH 14,10
Fo,1 D SKH 15,11
EAI-Electronic Associates Pty. Ltd.
REVISION 15-2-79
6 POLE RLY NOW 4 POLE
JUMPERS FOR TIP31 TO ±15V, 5V & DIODE D2 ADDED.
TITLE. ANALOG PANEL 2 of 3
NO. CIRCUIT DIAGRAM
PROJECT. EAI 1000
DRAWN. V.G.B.
DATE. 15-2-79
DESIGNER
SHT. NO.
DRG. Nº 11-045-0001 OS REV. 3

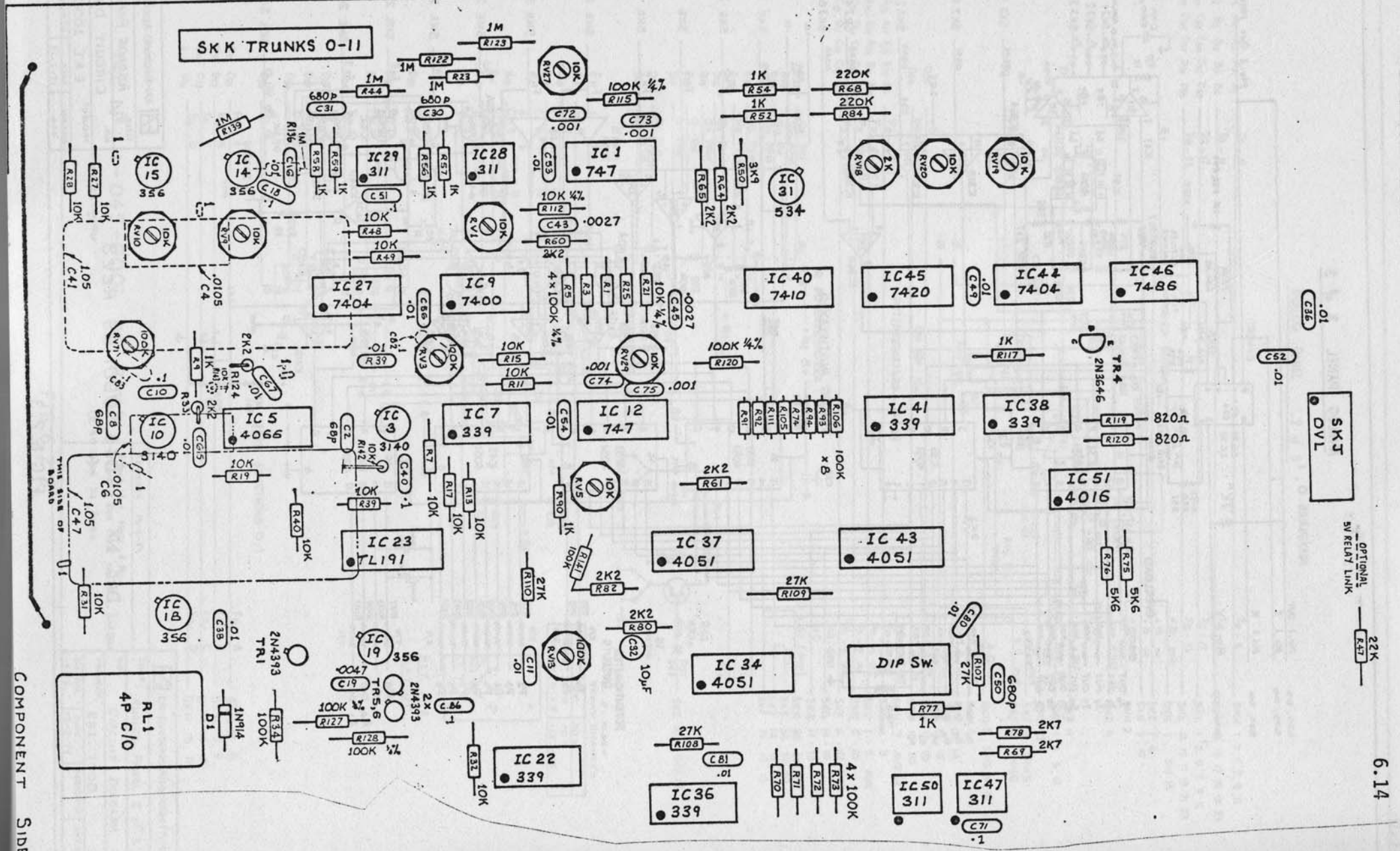
FIG 6.2.2



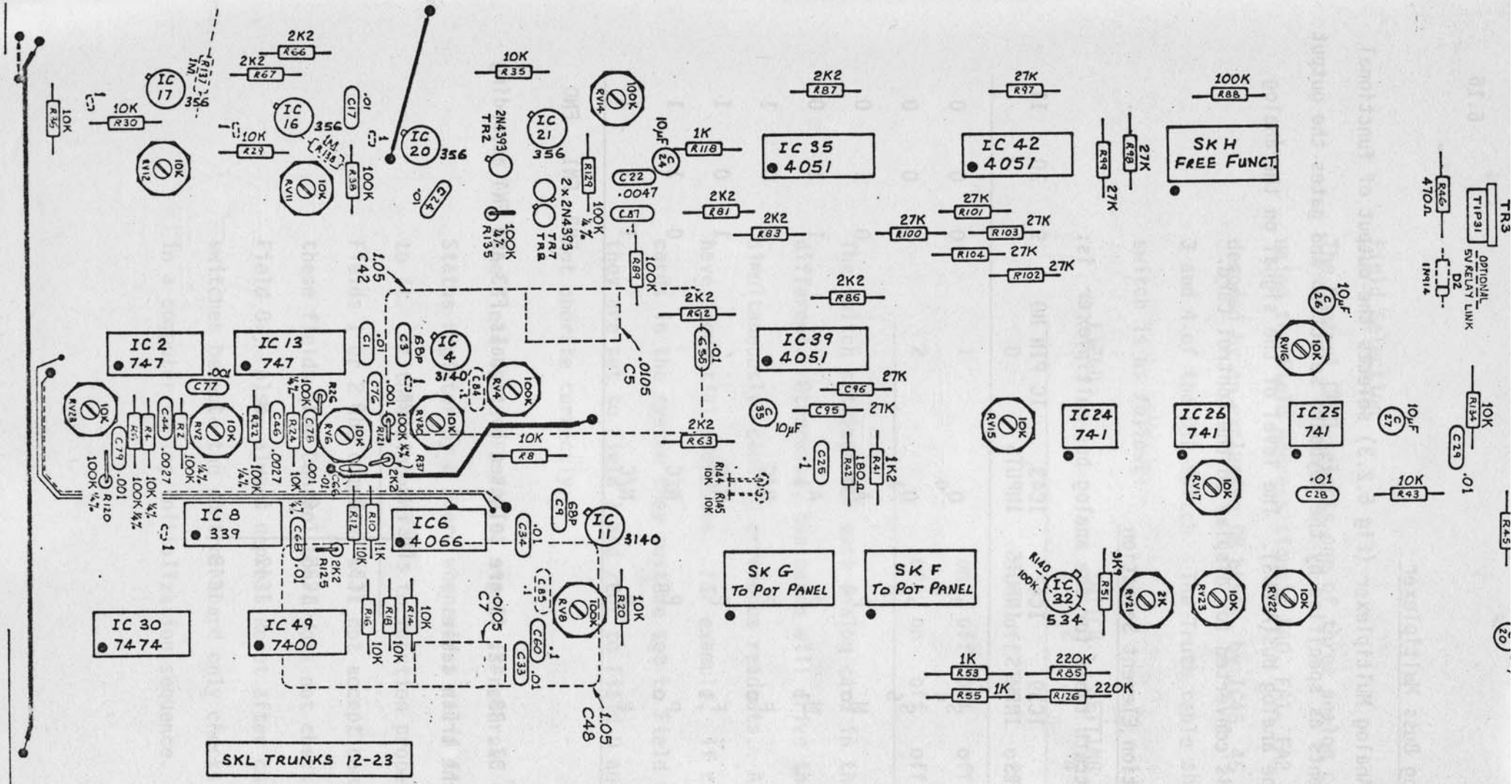
DRG. Nº 11-045-0001 OS REV. 3
(1 OF 3)
UPDATED 27-6-79

FIG 6.2.3

ANALOG BOARD - COMPONENT LAYOUT



COMPONENT SIDE VIEW



1 OPTIONAL 1pF CAPACITORS

DRG. Nº 11-045-0001 OA REV. 3

EAI-Electronic Associates Pty. Ltd.			
TITLE. ANALOG BOARD			
NO. COMPONENT LAYOUT			
PROJECT. EAI 1000			
DRAWN. VGA.	DATE. 5-2-79	DESIGNER	SHT. NO.

6.15

FIG 6.2.4

6.2.11 Analog Buss Multiplexer

The Analog Multiplexer (Fig 6.2.3) selects the output of functional elements as specified by the keyboard selection and gates the output to the analog bus(A BUS). The level of the signal on the analog bus is converted for display on the Control Card.

Function Element Selection

The truth table for the analog bus multiplexer is:

IC37 INPUTS	IC39 INPUTS	IC42 INPUTS	IC43 INPUTS	IC PIN NO	9	10	11
I_o	S_4	P_2	Q_o		0	0	0
I_1	S_5	P_3	Q_1		1	0	0
I_2	M_o	P_4	A_o		0	1	0
I_3	M_1	P_5	A_1		1	1	0
S_o	F_o	P_6	N/C		0	0	1
S_1	F_1	P_7	N/C		1	0	1
S_2	P_o	P_8	N/C		0	1	1
S_3	P_1	P_9	N/C		1	1	1
					FN2	FN1	FN0

IC's 37, 38, 42, 43 are selected by signals FN3 and FN4 according to the truth table:

	FN3	FN4
IC37	0	0
IC38	0	1
IC42	1	0
IC43	1	1

Field Selection

The Control CARD selects one of three analog cards in the system using the Field Address signals FA0, FA1, FA2 and FA3, which are decoded by an exclusive OR basis by IC46, 45 and positions 1,2,. 3 and 4 of the DIP Switch. The Truth table shows the field selection switch is as follows:

FIELD	SWITCH SETTING 1	2	3	4
0	off	off	off	off
1	on	off	off	off
2	off	on	off	off

The switch settings for each analog card in the system must be different. Otherwise, two cards will drive the Analog Bus simultaneously causing erroneous readouts. Also the cards must have sequential addresses. For example, if there are two analog cards in the system they must be set to Field 0 and Field 1. If they are set to Field 1 and 2 or to Field 0 and 2 the system will not operate correctly.

The Field Valid (FD VALID) signal is returned to the Control Board Status register by a board whenever a valid field address is presented to it. If this signal fails to function properly on boards assigned to Fields 1 or 2 the computer will not accept component addresses for these fields.(The Control board does not check this signal for Field 0.) Also, always depress Reset after changing the field select switches because the control board only checks for the fields present in a computer during initialization sequence.

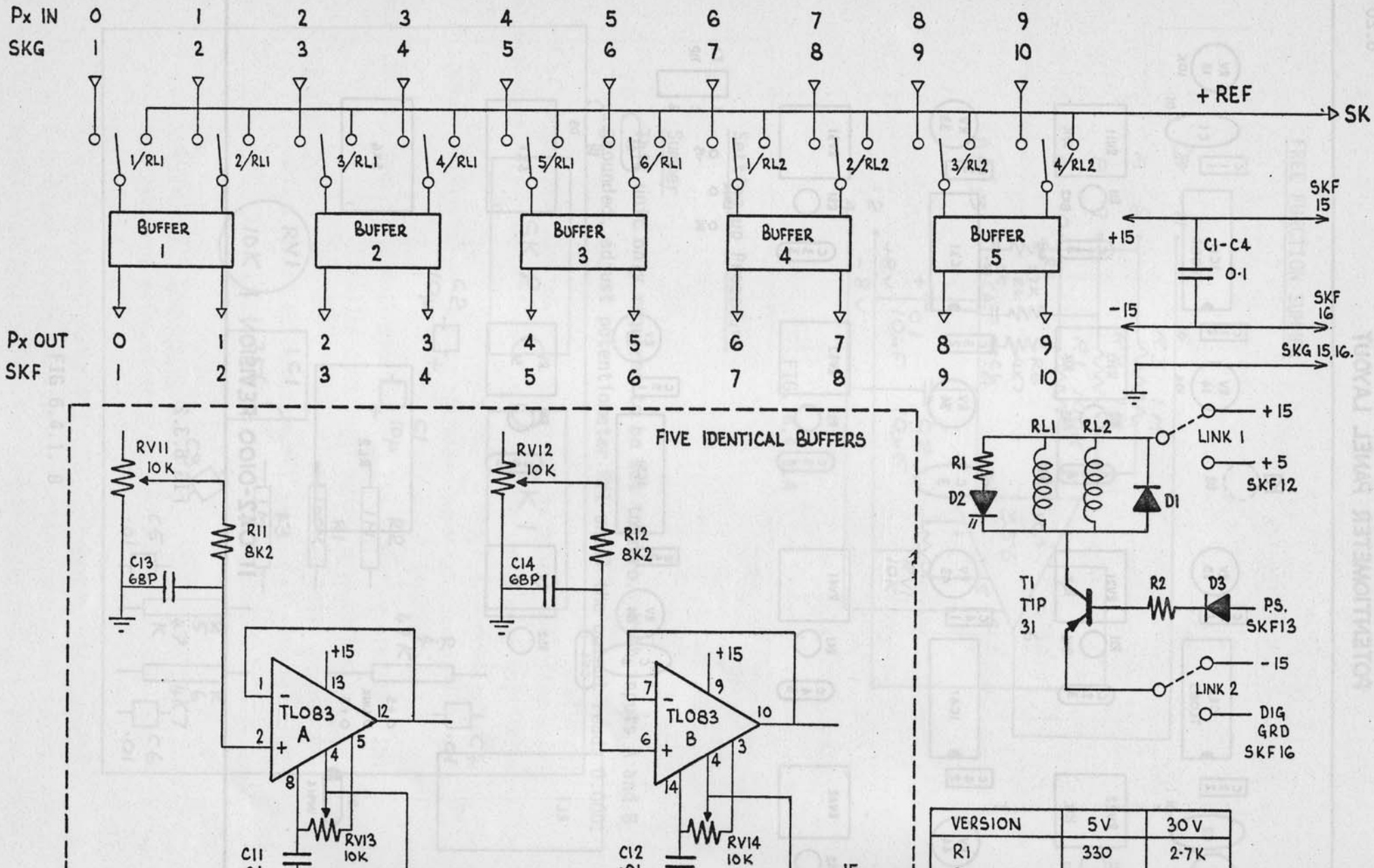
6.3 THE POTENTIOMETER PANEL

The potentiometer panel houses 10 potentiometers with buffered outputs. Two flat-strip cables carry signals and power from the Analog Card.

The potentiometer "IN" signal is taken via a relay to the potentiometer. The potentiometer output signal is buffered by an OP-AMP (LF356) and return to the appropriate potentiometer "OUT" patch point. RL 1 and 2 are energised directly from the potentiometer set (P.S.) key on the Keyboard. This key supplies +5v to TR1, (TIP31). The relays then apply +ve Ref to the input of all potentiometers.

Ealier models were fitted with relays having a 5 volt coil. Current models are fitted with relays with 30 volt coils. All links and relay associated components are factory set for the appropriate relay. (Refer Page 6.8).

POTENTIOMETER PANEL CIRCUIT DIAGRAM



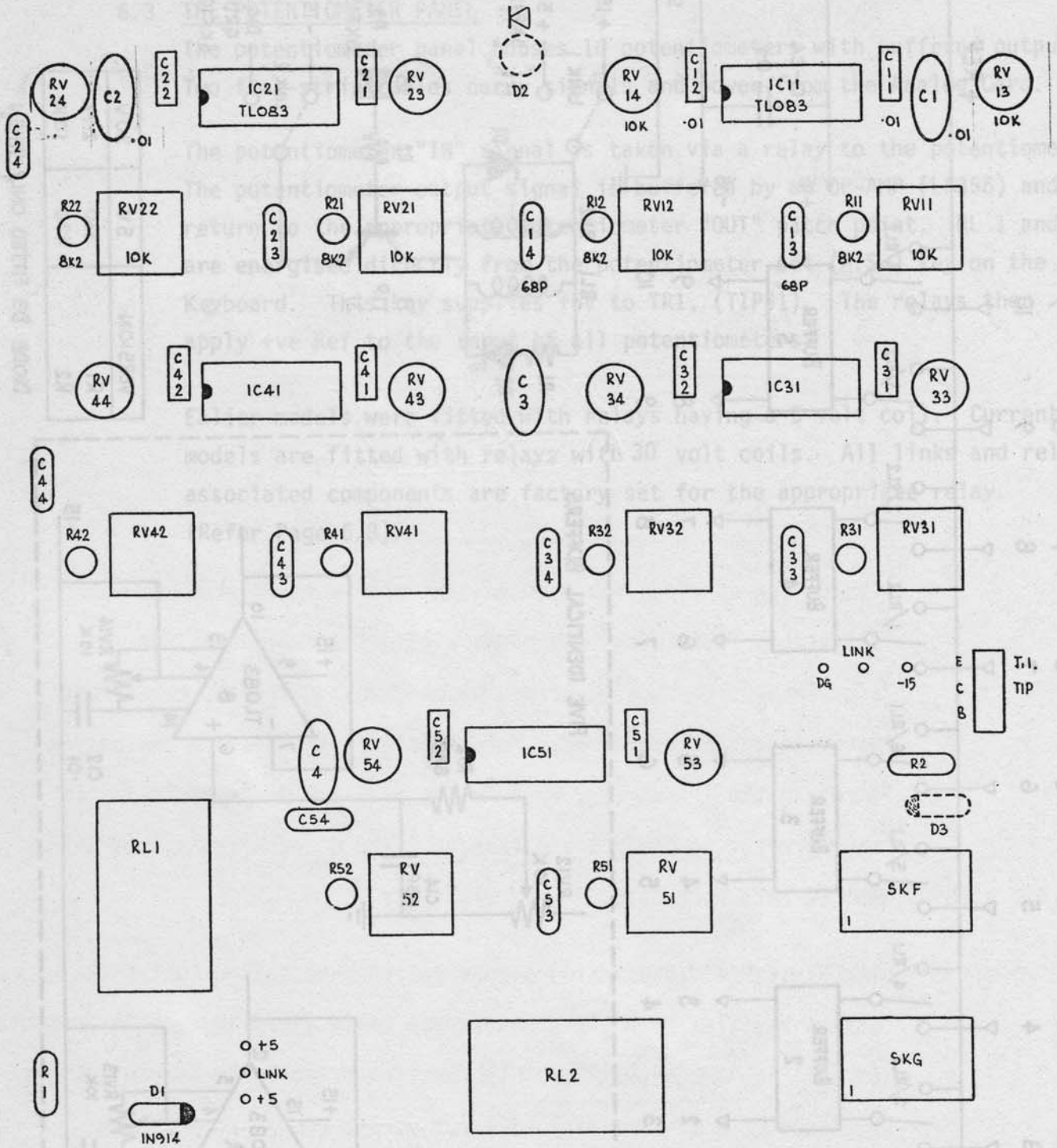
VERSION	5V	30V
R1	330	2·7K
R2	470	10K

DIODE D3 FITTED ONLY WHEN ANALOG CARD IS 30V AND POT PANEL IS 5V

FIG 6.3.1

DRAWING 11·042·0100 REVISION 1

POTENTIOMETER PANEL LAYOUT



II-042-0100 REVISION 1

FIG 6.3.2

FREE FUNCTION SUMMER

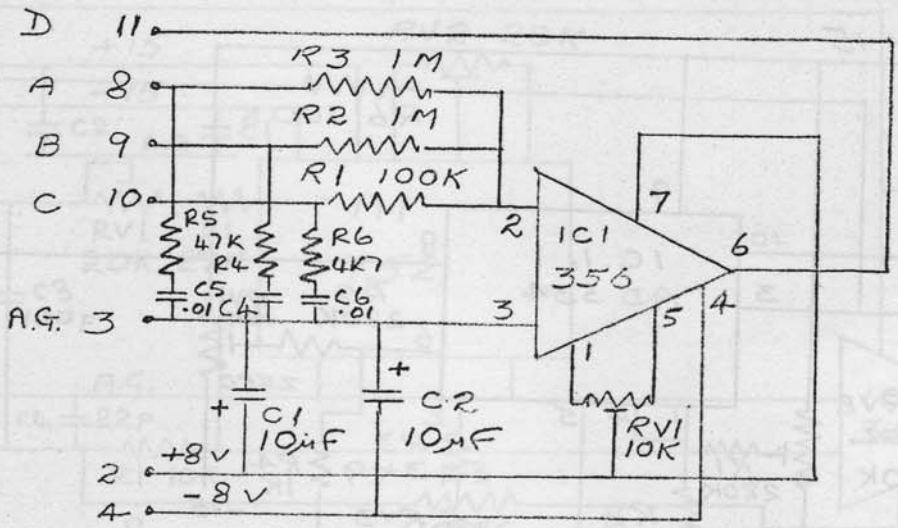


FIG. 6.4.1.A

Setting up Procedure

Summer

This unit only requires to be set to zero. With inputs A and B grounded, adjust potentiometer RV1 until the output reads 0.000.

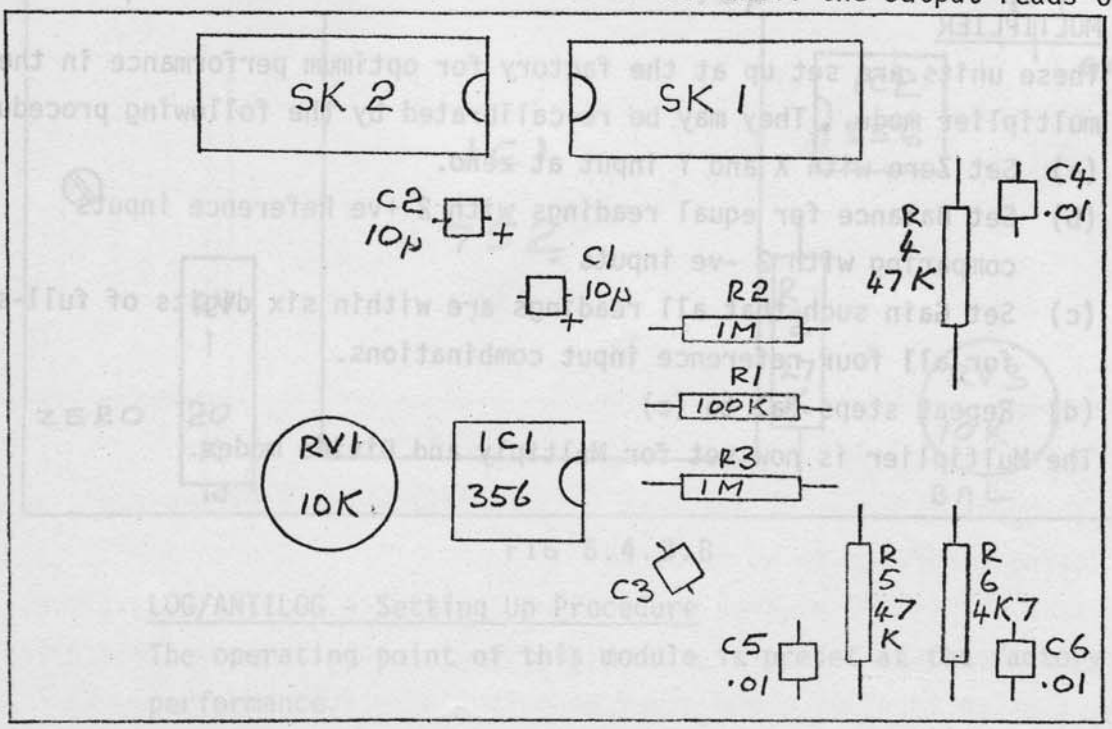


FIG 6.4.1. B

FREE FUNCTION MULTIPLIER

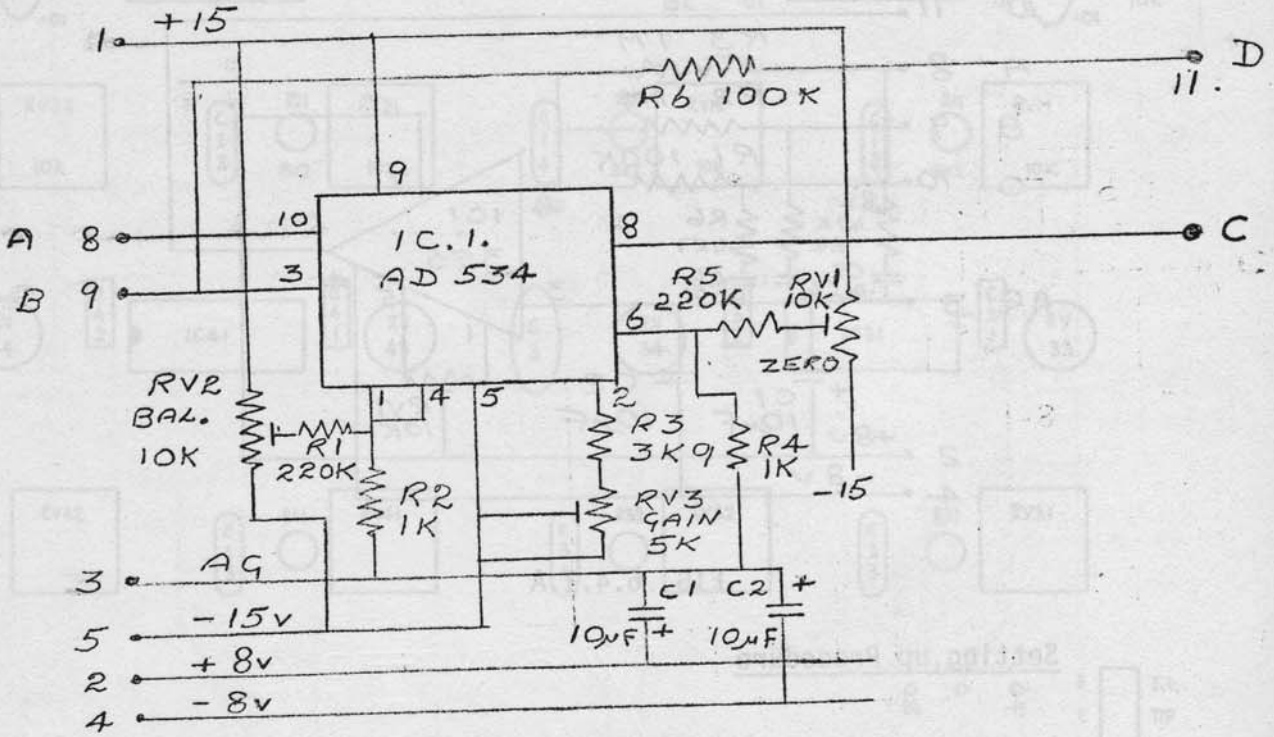


FIG 6.4.2

Setting Up Procedure

MULTIPLIER

These units are set up at the factory for optimum performance in the multiplier mode. They may be re-calibrated by the following procedure:-

(a) Set Zero with X and Y input at zero.

(b) Set Balance for equal readings with 2 +ve Reference inputs comparing with 2 -ve inputs -

(c) Set Gain such that all readings are within six digits of full-scale for all four reference input combinations.

(d) Repeat steps (a) to (c)

The Multiplier is now set for Multiply and Divide modes.

FREE FUNCTION LOG MODULE

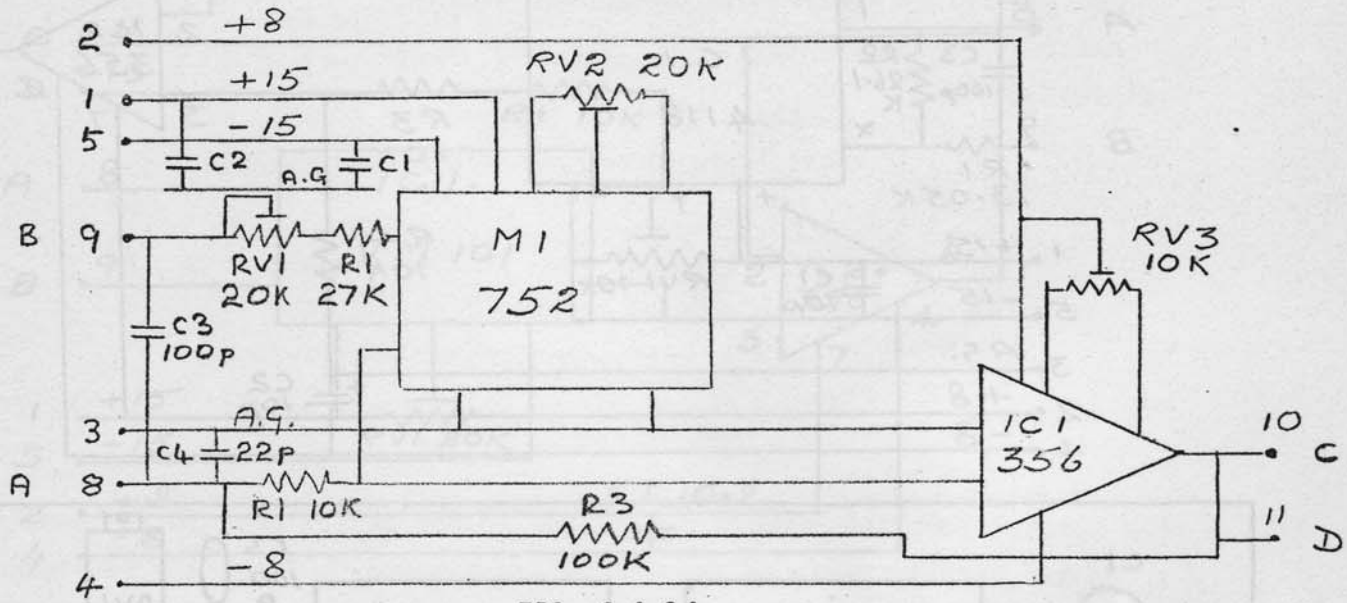


FIG. 6.4.3A

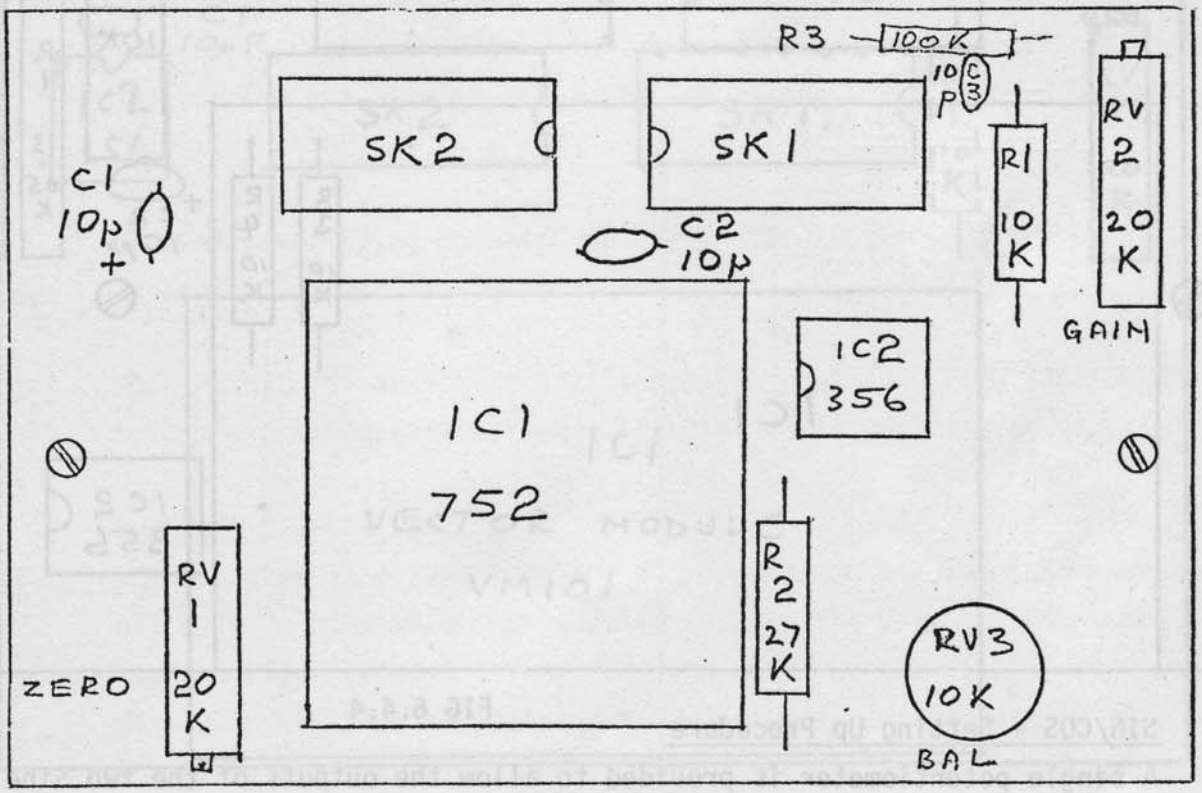


FIG 6.4.3.B

LOG/ANTILOG - Setting Up Procedure

The operating point of this module is preset at the factory for optimum performance.

Note that Potentiometer RV3 (10K ohm) must not be adjusted.

With B and C connected, fee -.01 MU to input A (ensure that this is exactly -50.0mV). Adjust RV2 so that the output D is zero. With an input of -1.000 MU, adjust RV1 such that output D is +1.000.

FREE FUNCTION SIN/COSINE MODULE

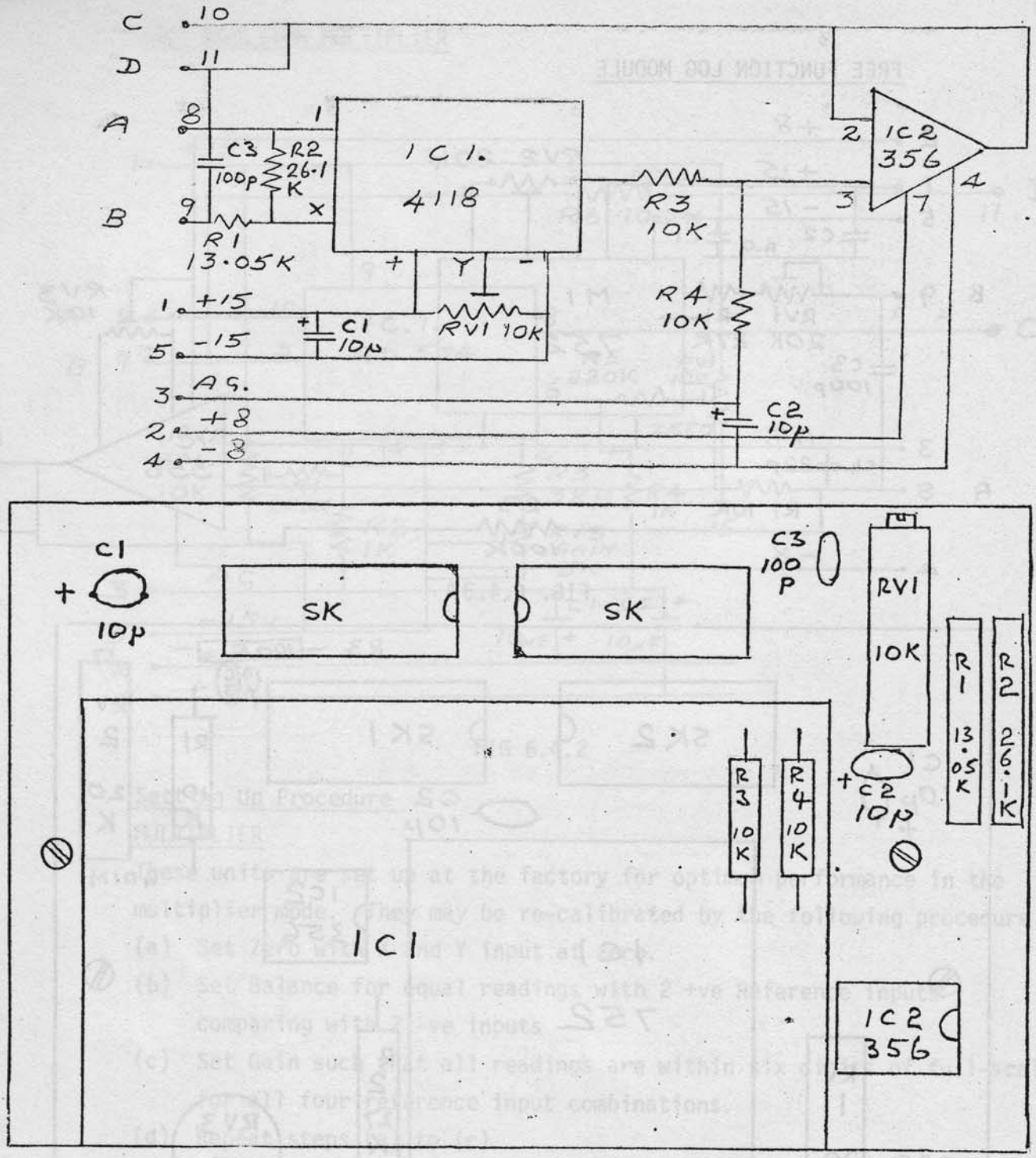


FIG 6.4.4

SIN/COS - Setting Up Procedure

A single potentiometer is provided to allow the outputs of the two Sine and two Cosine quadrants to be balanced.

With a 45^{0} (+.500 Machine Unit) input to input A (Sine), adjust the Potentiometer such that the output (C and D) reads +.707 on the display. Check that an input of -.500 gives an output of -.707.

With a +.500 input to input B(Cosine), check that the output reads -.707. Similarly, an input ot -.500 should give an output of +.707.

Readjust the potentiometer if necessary such that the output errors are minimised.

FREE FUNCTION VECTOR MODULE

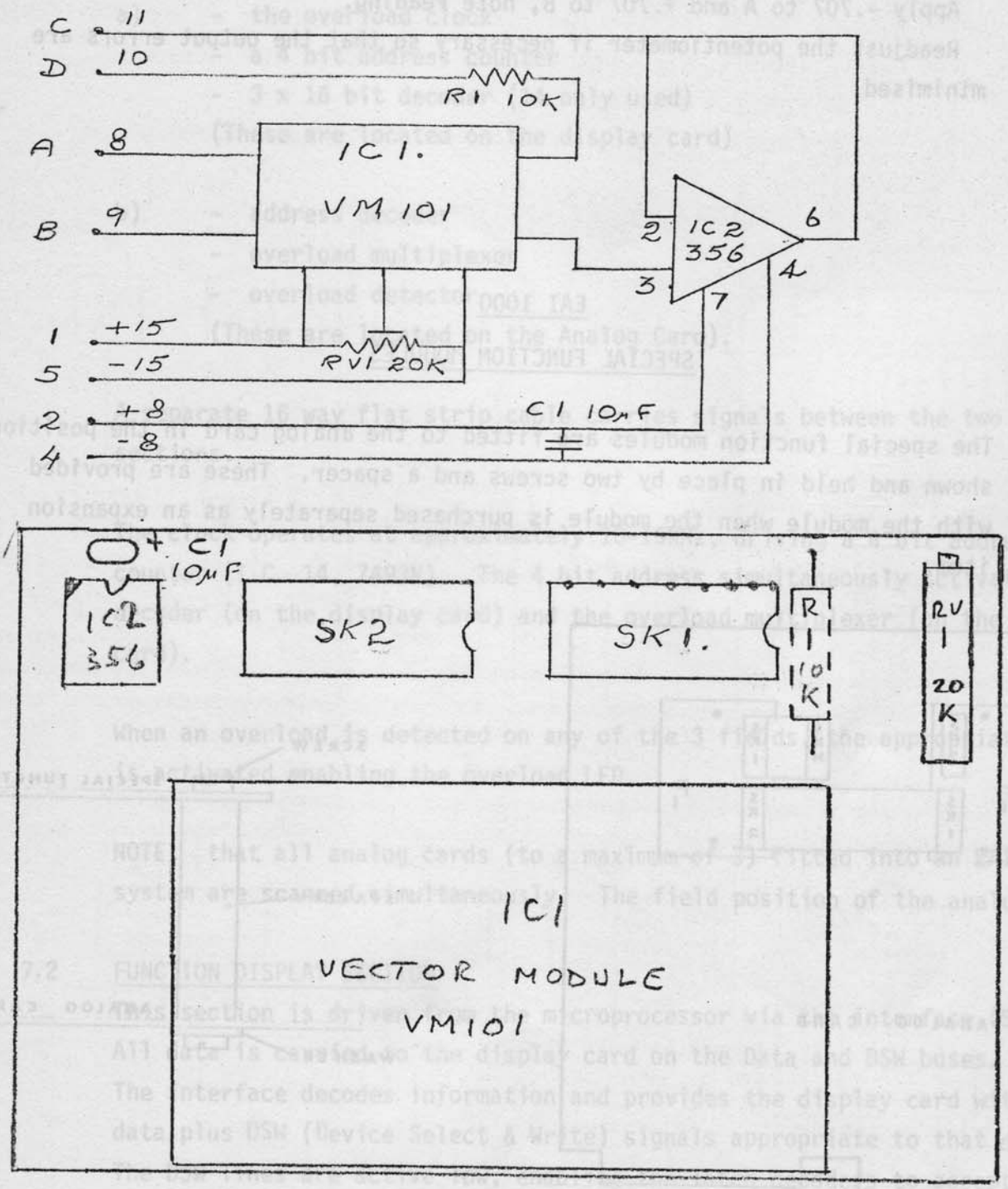


FIG 6.2.5

VECTOR - Setting Up Procedure

A potentiometer is provided to allow the outputs from the four quadrants to be balanced.

Apply +.707 to inputs A & B, adjust the potentiometer so that the output C is +1.000.

Apply -.707 to inputs A and B. Output reading should be -1.000.

Apply +.707 to A and -.707 to B, not reading.

Vector - Setting Up Procedure (cont'd)

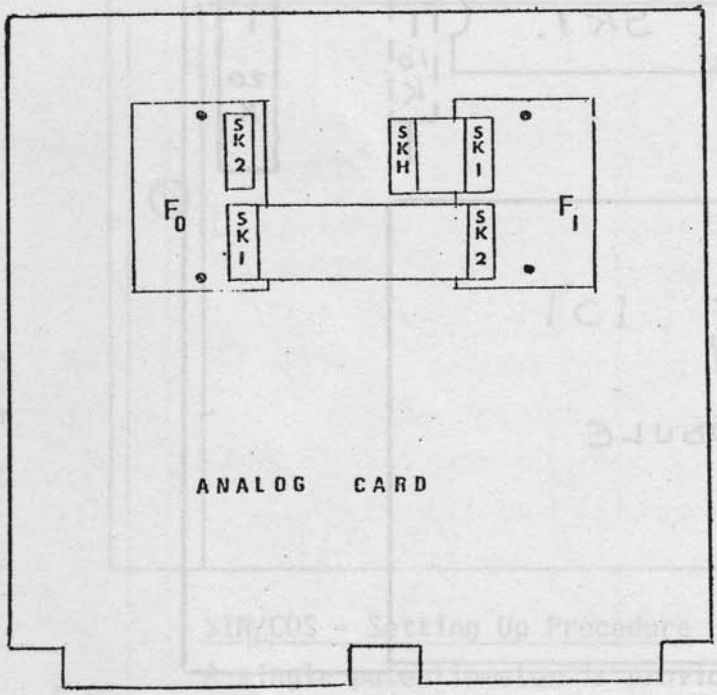
Apply -.707 to A and +.707 to B, note reading.

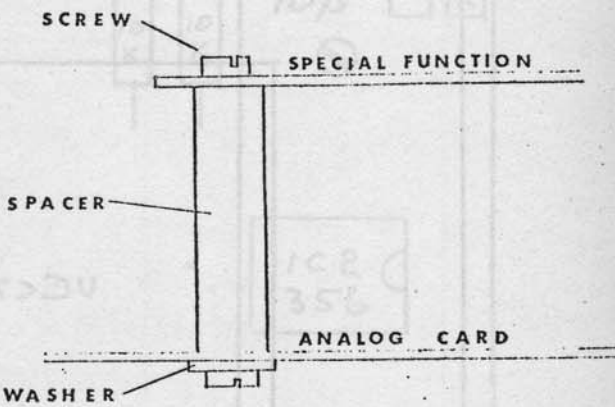
Readjust the potentiometer if necessary so that the output errors are minimised.

EAI 1000

SPECIAL FUNCTION MODULES

The special function modules are fitted to the analog card in the positions shown and held in place by two screws and a spacer. These are provided with the module when the module is purchased separately as an expansion item.





Connections are made to the special functions from SK H. F_1 is the first function fitted and F_0 when fitted is connected to SK2 of F_1 for each analog card. All power supply lines for F_0 are fed from SK H via F_1.

7.1. OVERLOAD DISPLAY

The overload system is independent of the microprocessor and comprises:

a)
- the overload clock
- a 4 bit address counter
- 3 x 16 bit decoder (14 only used)

(These are located on the display card)

b)
- address decoder
- overload multiplexer
- overload detector

(These are located on the Analog Card).

A separate 16 way flat strip cable carries signals between the two sections.

The clock operates at approximately 10-15KHz, driving a 4 bit address binary counter (I.C. 14, 7493N). The 4 bit address simultaneously activates the decoder (on the display card) and the overload multiplexer (on the analog card).

When an overload is detected on any of the 3 fields, the appropriate decoder is activated enabling the overload LED.

NOTE: that all analog cards (to a maximum of 3) fitted into an EAI-1000 system are scanned simultaneously. The field position of the analog card.

7.2 FUNCTION DISPLAY SECTION

This section is driven from the microprocessor via the interface (5.2.2). All data is carried to the display card on the Data and DSW buses. The interface decodes information and provides the display card with data plus DSW (Device Select & Write) signals appropriate to that data. The DSW lines are active low, enabling the latch decoders to accept and hold the appropriate data.

Data lines D_0 - D_3 are used to transmit information for all function, field, function number displays. D_0 - D_3 are also used for '+1' and 10^{-2} displays. D_{4-7} are used for 10^{-1} and 10^{-3} displays.

CHAPTER 7

7. DISPLAY MODULE

The Display Module provides the readout of information of the EAI-1000 to the User. The P.C. card supports two independent sections,

a) for overload display, and

b) for function, field, function number and value display.

DISPLAY MODULE FUNCTION DIAGRAM

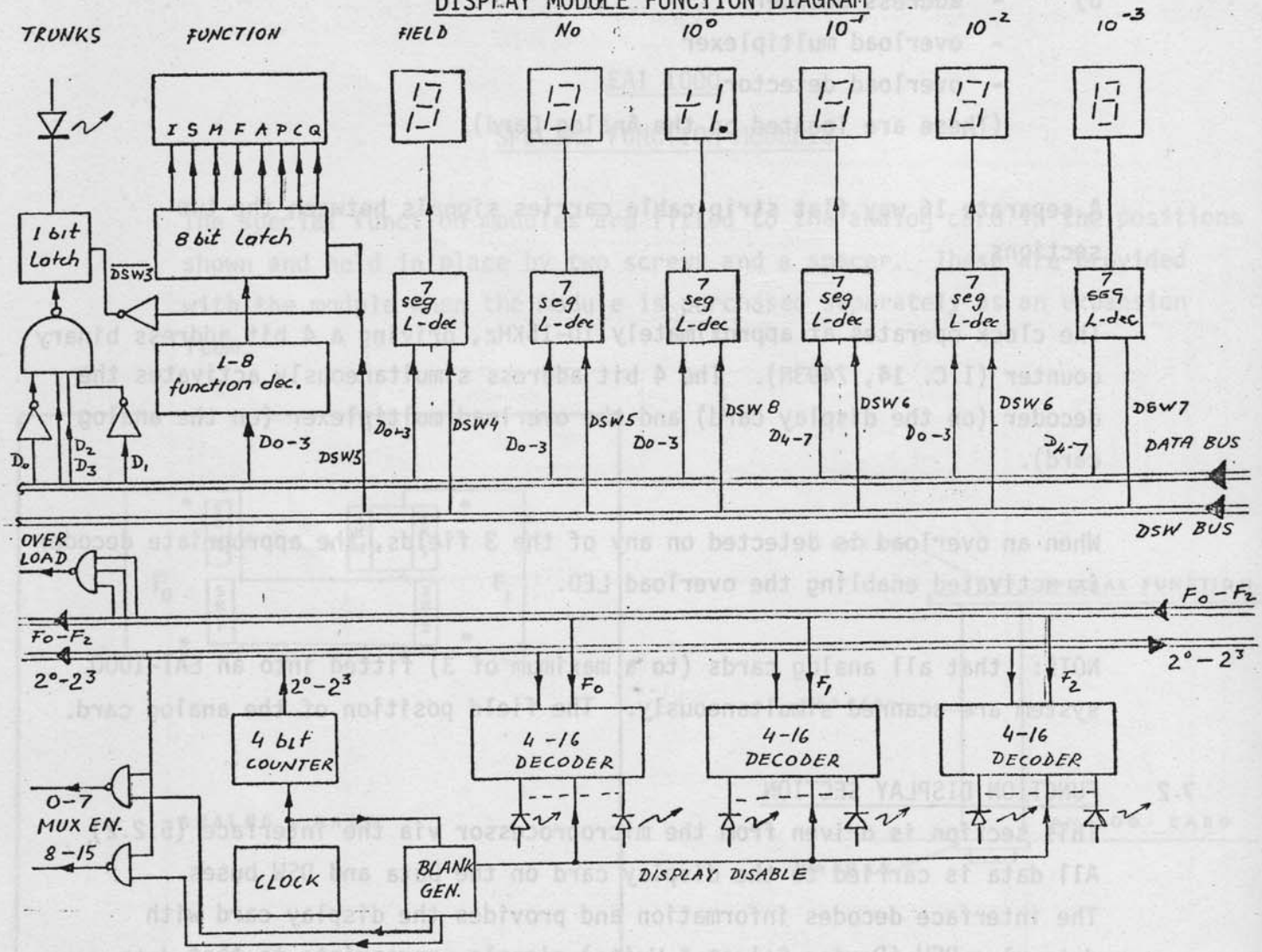


Fig7.1.A

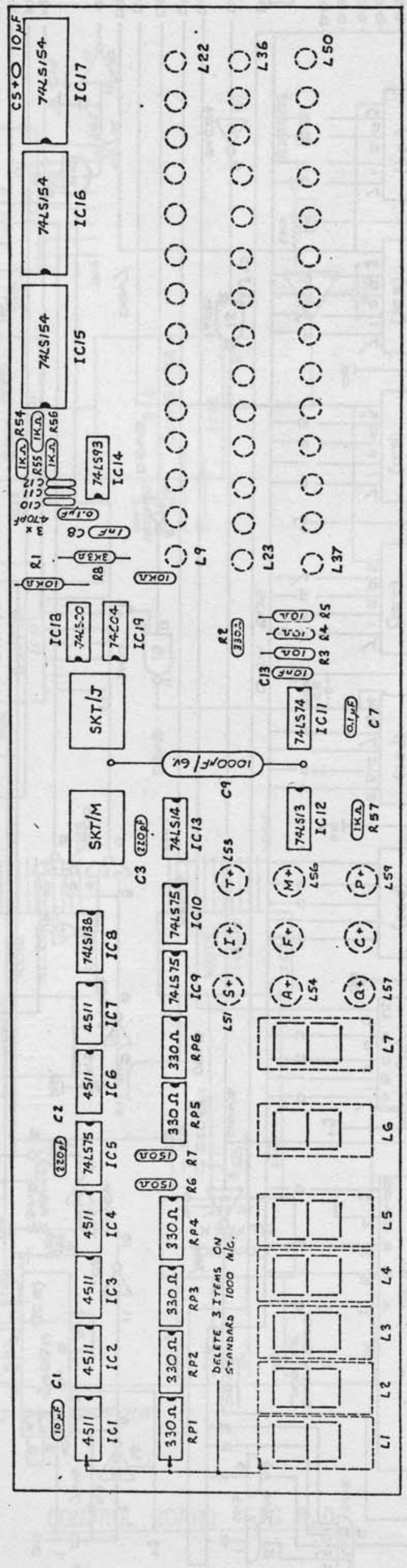

DISPLAY LAYOUT
(COMPONENT SIDE)
DELETE 3 ITEMS ON STANDARD 1000 N.C.
IC1 IC2 IC3 IC4 IC5 IC6 IC7 IC8 IC9 IC10 IC11 IC12 IC13 IC14 IC15 IC16 IC17 IC18 IC19
4511
74LS75
74LS138
74LS14
74LS74
74LS13
74LS93
74LS154
74LS30
74C04
SKT/M
SKT/J
330Ω
RP1 RP2 RP3 RP4 RP5 RP6
C1 C2 C3 C5 C7 C8 C9 C10 C13
10μF
330pF
220pF
1000μF/6V
0.1μF
1nF
470pF
10KΩ
1KΩ
150Ω
3K3Ω
330Ω
R1 R2 R3 R4 R5 R6 R7 R8 R54 R55 R56 R57
L1 L2 L3 L4 L5 L6 L7 L9 L22 L23 L36 L37 L50
L51 L53 L54 L56 L57 L59
S+ I+ T+ A+ F+ M+ Q+ C+ P+

Figure 7.2

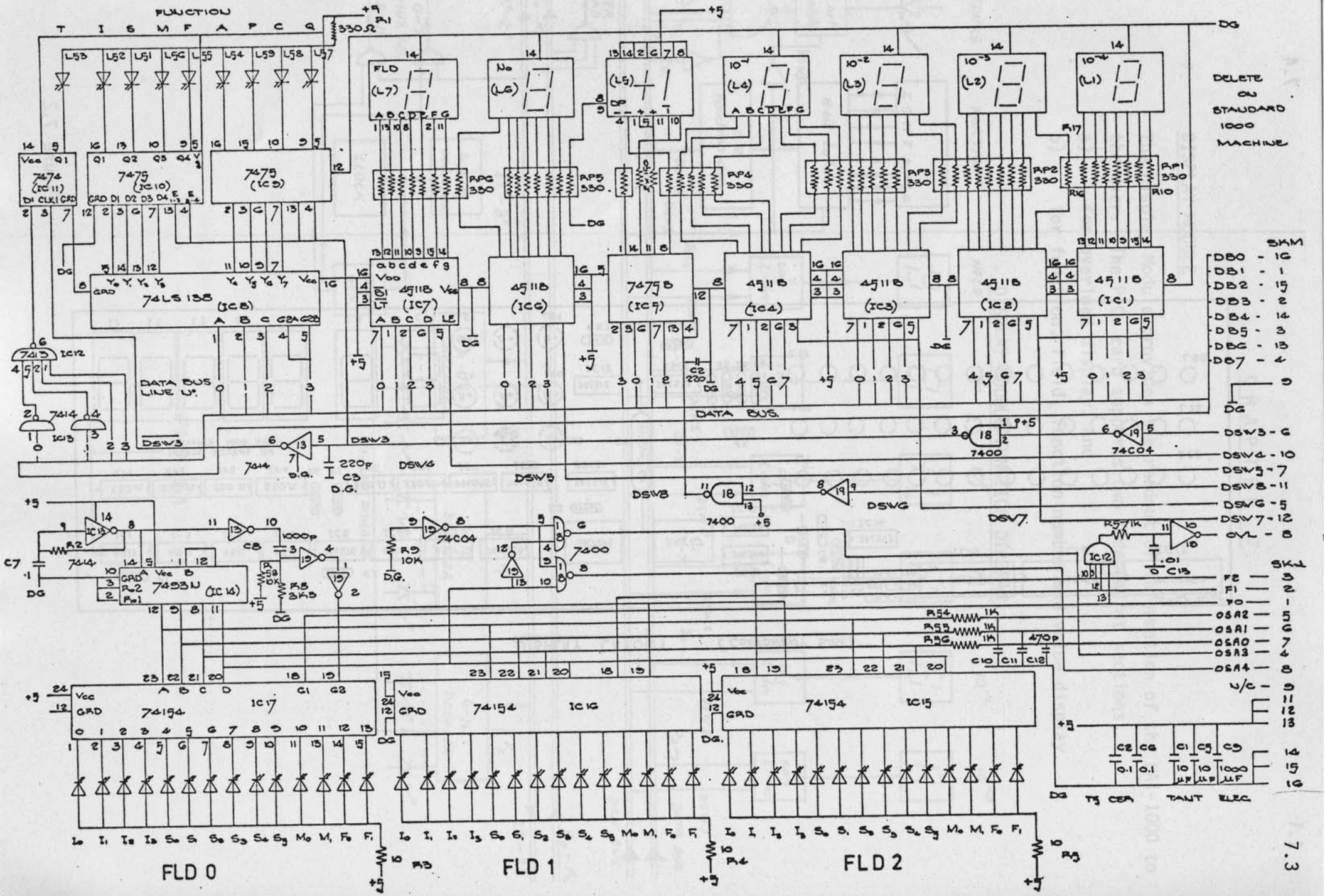
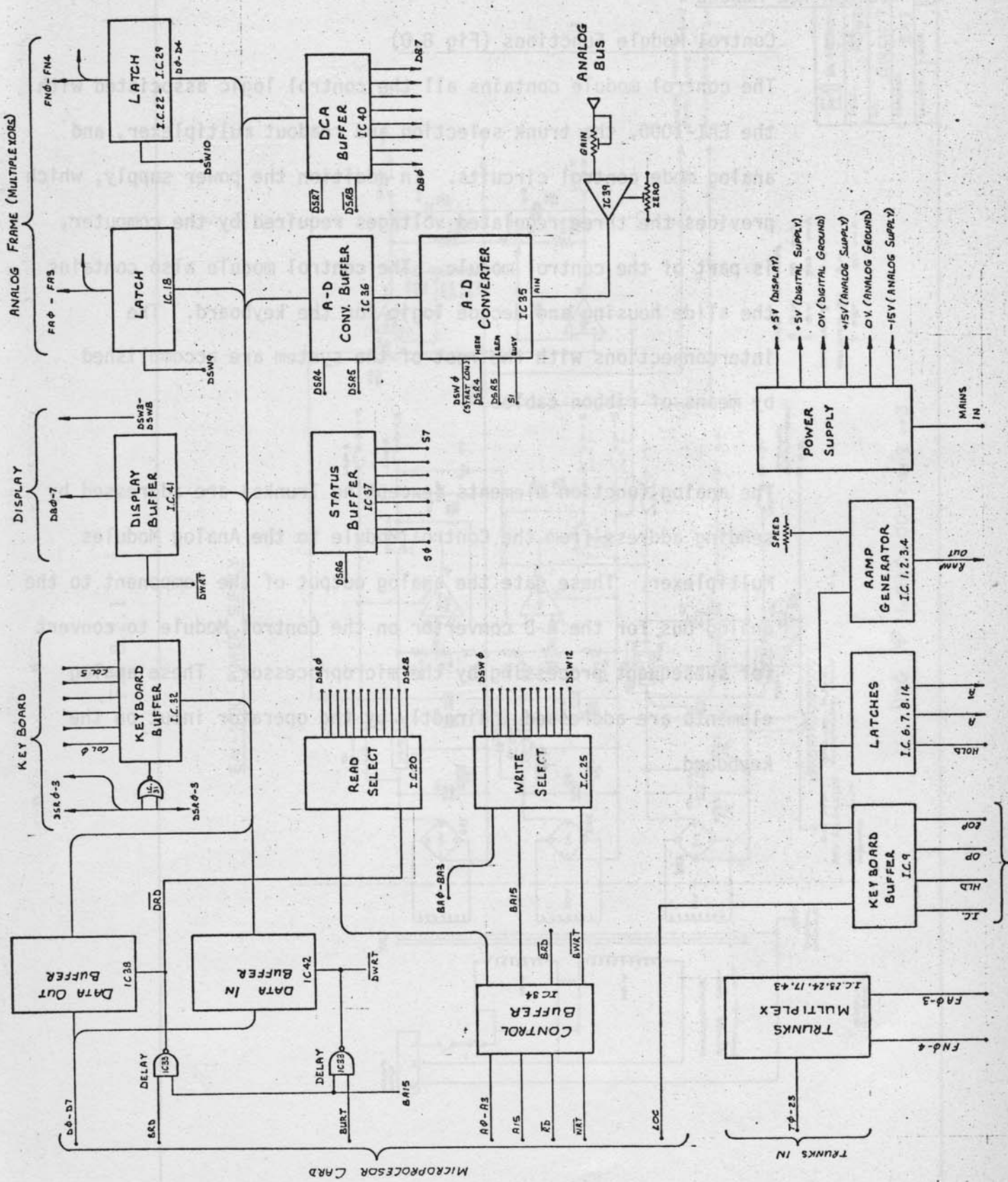

FUNCTION
T I S M F A P C Q
330Ω R1
+5
DG
DELETE ON STANDARD 1000 MACHINE
7474 (IC 11)
7475 (IC 10)
7475 (IC 9)
74LS138 (IC 8)
7413 IC12
7414 IC13
7400
74C04
7493N (IC 14)
74154 IC17
74154 IC16
74154 IC15
4511B (IC 6)
7475B (IC 7)
4511B (IC 4)
4511B (IC 3)
4511B (IC 2)
4511B (IC 1)
DATA BUS LINE U.
DATA BUS.
DSW3
DSW4
DSW5
DSW8
DSW6
DSW7
220p C3 D.G.
1000p C8
470p C10 C11 C12
.01 C13
1K R5
10K R9
3K3 R8
10K R58
1K R54 R55 R56
10 R3 R4 R5
SKM
DB0 - 16
DB1 - 1
DB2 - 15
DB3 - 2
DB4 - 14
DB5 - 3
DB6 - 13
DB7 - 4
DSW3 - 6
DSW4 - 10
DSW5 - 7
DSW8 - 11
DSW6 - 5
DSW7 - 12
OVL - 8
SKJ
F2 - 3
F1 - 2
F0 - 1
OSA2 - 5
OSA1 - 6
OSA0 - 7
OSA3 - 4
OSA4 - 8
U/C - 9
11
12
13
14
15
16
C2 0.1 C6 0.1 C1 10 µF C5 10 µF C9 1000 µF
TANTALUM ELEC.
FLD 0
FLD 1
FLD 2
7.3

Fig. 7.1B



CONTROL BOARD FIG 8.0

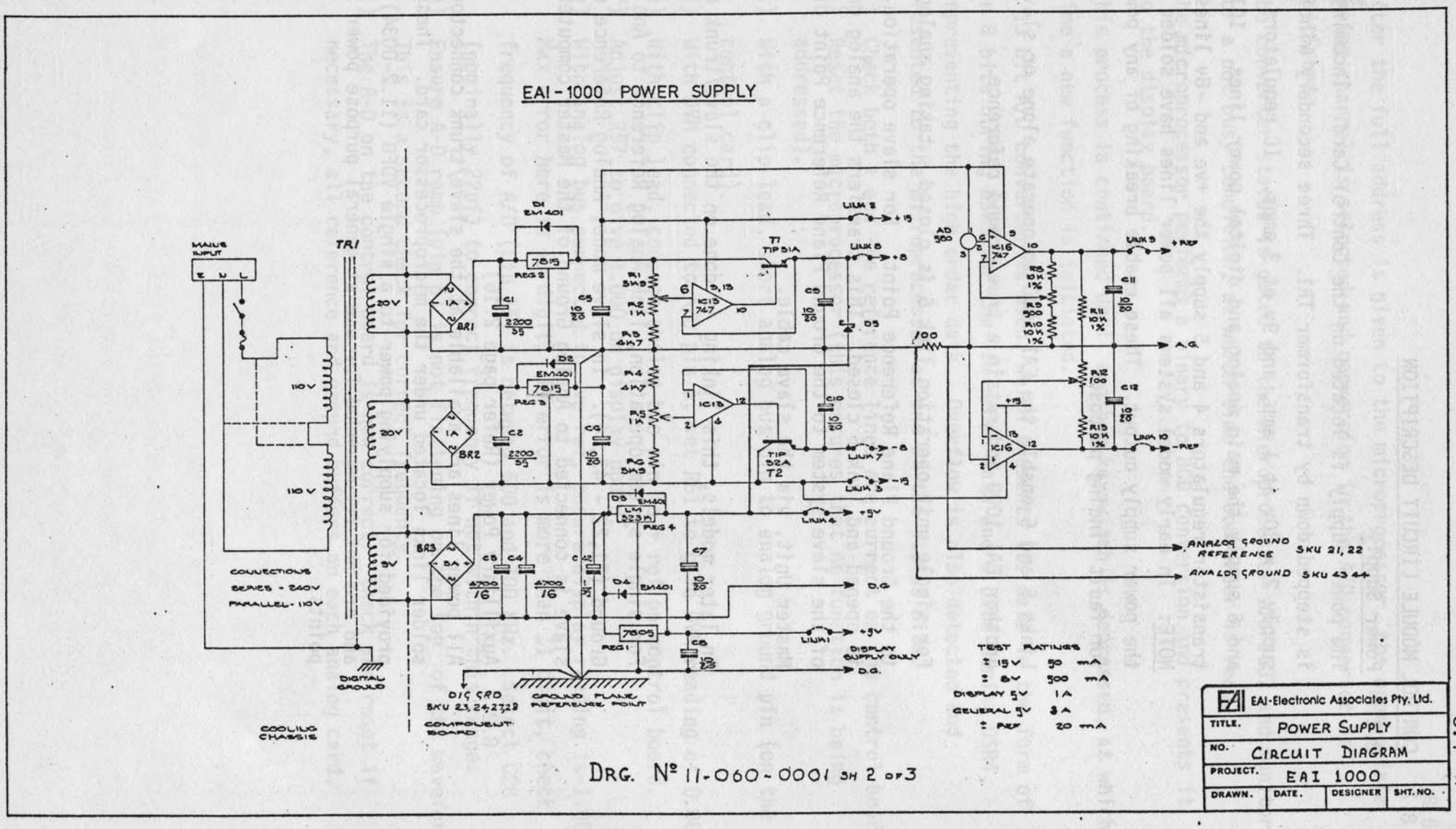
8.0 CONTROL MODULE

8.1 Control Module Functions (Fig 8.0)

The control module contains all the control logic associated with the EAI-1000, the trunk selection and readout multiplexer, and analog mode control circuits. In addition the power supply, which provides the three regulated voltages required by the computer, is part of the control module. The control module also contains the slide housing and decode logic for the keyboard. The interconnections with the rest of the system are accomplished by means of ribbon cables.

The analog function elements (excepting Trunks) are addressed by sending address from the Control Module to the Analog Modules Multiplexer. These gate the analog output of the component to the analog bus for the A-D convertor on the Control Module to convert for subsequent processing by the microprocessor. These analog elements are addressed indirectly by the operator input on the keyboard.

FIG 8.2.1



DRG. Nº 11-060-0001 SH 2 OF 3

EAI-Electronic Associates Pty. Ltd.			
TITLE. POWER SUPPLY			
NO. CIRCUIT DIAGRAM			
PROJECT. EAI 1000			
DRAWN.	DATE.	DESIGNER	SHT. NO.

8.2 CONTROL MODULE CIRCUIT DESCRIPTION

8.2.1 Power Supply

The power supply is located on the Control Card. Incoming mains is stepped down by transformer TR1. Three secondary windings supply 2 x 20v at 1 amp, and 9v at 3 amps. IC regulators 1,2,3 and 6 supply the main analog and digital power lines. IC13 feeding transistor regulators 4 and 5 supply the +ve and -8v lines.

NOTE: In early model systems all power lines have solder links at the power supply output. These enable breaking of any power line for fault finding purposes

Links 5 and 6 enable the EAI 1000 to operate alone or slaved to another EAI 1000 and retain a true ground reference.

For single unit operation link 6 is closed - taking analog ground to the Ground Plane Reference Point. For slave operation, link 6 is opened and link 5 closed. This transfers the analog ground of the slave system to the Ground Plane Reference Point of the Master Unit, via the slave cable.

In later models, this linking is done on the slave/trunk connection.

For single system operation, link Analog Reference to Analog Ground (21,22 - 43,44). In slave mode, Analog Reference of the slave is connected to Analog Ground of the Master computer.

8.2.2 Auxilliary Power (Refer page 2.16)

All power lines are available at the slave/trunk connector via solder links located under the microprocessor card. These are provided for supplying power to a single VDFG (11.2-0034) only and are not recommended for use as general purpose power supply points.

After the full address is given to the microprocessor, the appropriate analog channel is selected and conversion in the A/D converter is initiated.

The converter status is gated to the microprocessor via IC37 and monitored for a not busy condition, at which time the converter is read.

The microprocessor performs a binary to BCD conversion and presents it to the display board.

This process is continued until another keyswitch is depressed, at which time a new function is initiated.

A 13 bit A/D converter is used, which presents its data in the form of an 8 bits during DSR5 for the low order data and 5 bits during DSR4, representing the high order data. Overflow is also detected and presented to the microprocessor as one of the status bits.

a) Check both + and -ve reference lines are currect on the control board.
b) Reset the microprocessor (this ensures that no function is being addressed).
c) With a clip lead, short analog bus pin to analog ground pin (on the control card).
d) With DVM connected to A/D pin 5, set R61 to give DVM reading of 0.0000.
e) With clip lead, connect analog bus pin to + ref on control board.
f) Adjust R57 to give 1.000 on display board.
g) With analog bus connected to -ve ref, ensure display reading is-1.000. Max error here is +1 digit. If error is more than $\pm$1 digit, check frequency of A/D (pin 15) is between 500 and 700 KHz. Select C28 (nominally 22pf) to correct frequency if not within this range.
h) Ensure A-D ramp (pin 6) is not flattening on the top of the waveform. This is a second check for correct frequency.
i) The A-D on the control board is now correct. Check and reset if necessary, all reference and ground buffers on each analog card.

8.2.2 Control Board

The Control Board (Ref Fig 8.2.2) provides the logic required to drive the display, multiplex the keyboard, select analog channels and control the A/D converter.

Data and address bus signals are initially buffered by IC43, IC38 and IC34 respectively.

The $\overline{RD}$ and $\overline{WRT}$ from the microprocessor are delayed by IC33/6 and IC33/8 respectively and gated with A15 to provide settling time for the data bus and select logic for the tristate buffers IC42 and IC38.

IC25 is the decoder used to supply the write data strobes (DSWØ through DSW12) to enable the microprocessor to control the output peripherals (display, analog multiplexor).

IC20 decodes the read data strobes (DSRØ - DSR8) to input the data from the keyboard and A/D converter to the microprocessor.

The keyboard is scanned by firmware and is input via IC32 to the microprocessor data bus.

IC18, IC22 and IC29 latch the data bus to control the analog multiplexer.

IC41 buffers the data bus to the display board. IC36 buffers the data from the A/D converter IC35.

The microprocessor continuously scans the keyboard. When a switch is selected the firmware responds accordingly. When a function key is depressed then the firmware immediately displays the function and then returns to scan the keyboard.

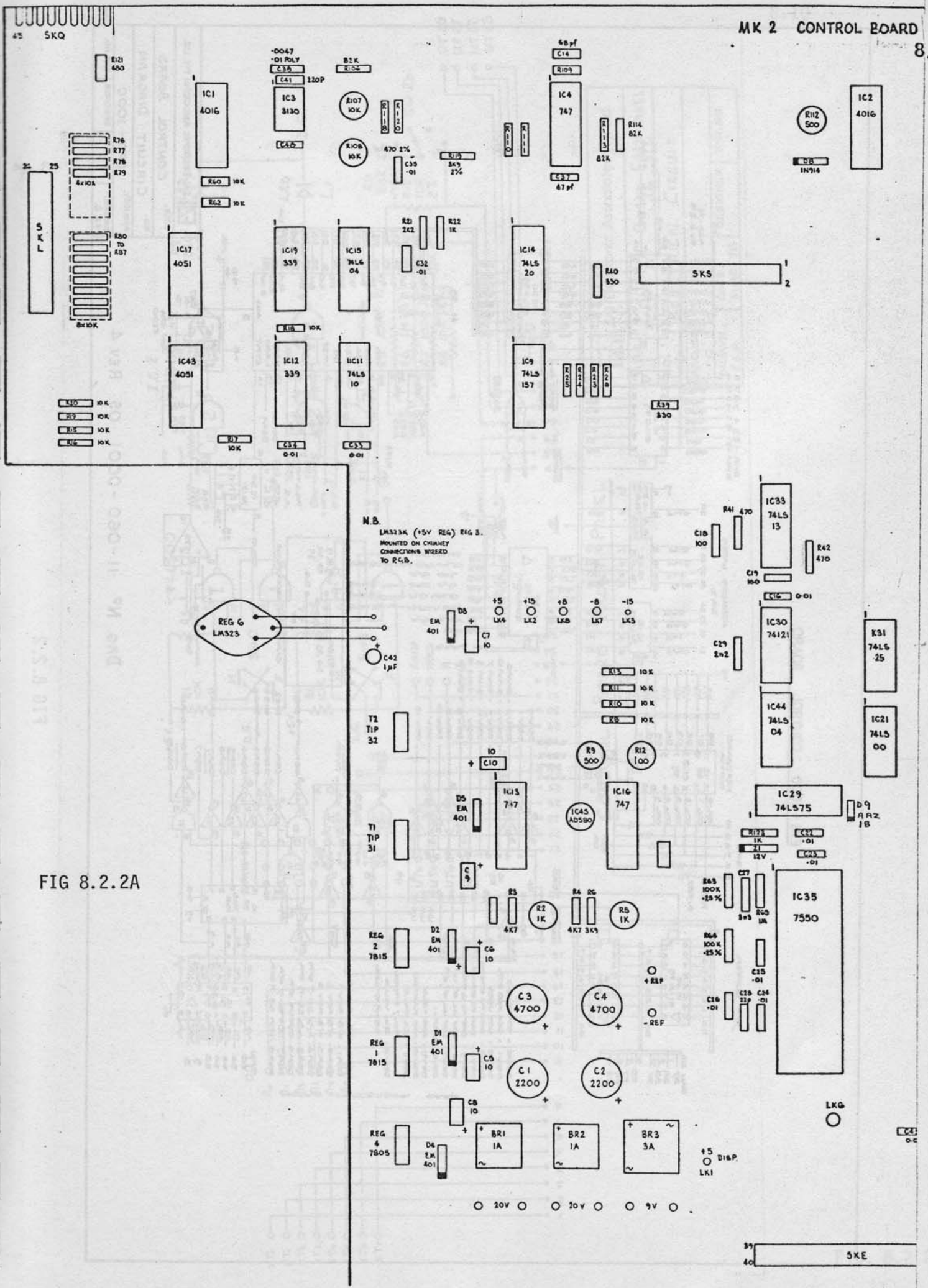

SKQ
SKS
SKE
IC1 4016
IC2 4016
IC3 3130
IC4 747
IC9 74LS 157
IC11 74LS 10
IC12 339
IC13 747
IC14 74LS 20
IC15 74LS 04
IC16 747
IC17 4051
IC19 339
IC29 74LS75
IC30 74121
IC33 74LS 13
IC35 7550
IC43 4051
IC44 74LS 04
IC45 AD580
K31 74LS 25
IC21 74LS 00
REG G LM323
REG 1 7815
REG 2 7815
REG 4 7805
BR1 1A
BR2 1A
BR3 3A
T1 TIP 31
T2 TIP 32
N.B.
LM323K (+5V REG) REG 3.
MOUNTED ON CHIMNEY
CONNECTIONS WIRED
TO PCB.
+5 LK4
+15 LK2
+8 LK8
-8 LK7
-15 LK5
+5 DISP. LK1
LKG
20V
20V
9V

FIG 8.2.2A

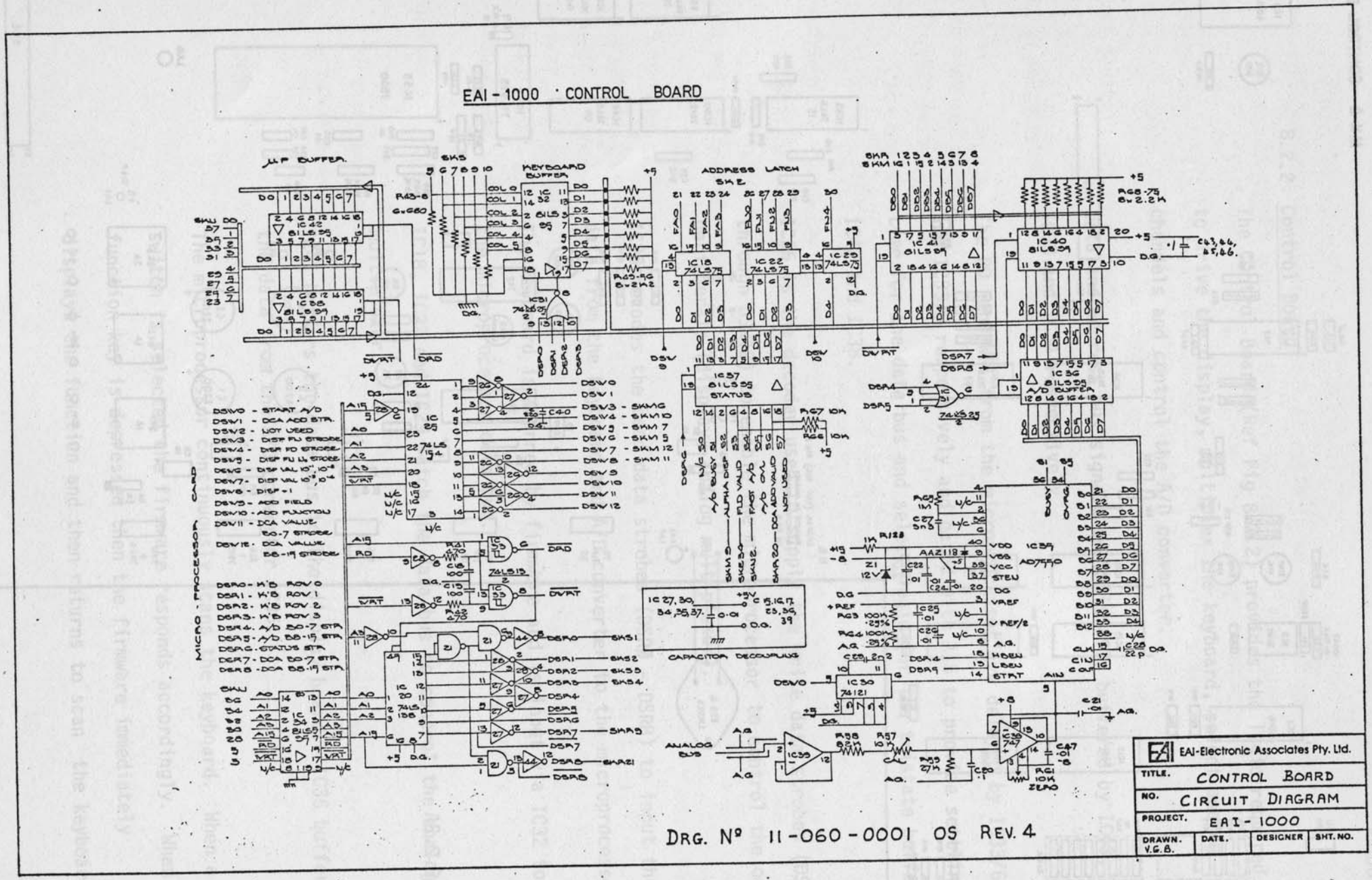

EAI - 1000 · CONTROL BOARD
MICRO - PROCESSOR CARD
KEYBOARD BUFFER
ADDRESS LATCH
A/D BUFFER
STATUS
CAPACITOR DECOUPLING
DRG. Nº 11-060-0001 05 REV. 4
EAI-Electronic Associates Pty. Ltd.
TITLE. CONTROL BOARD
NO. CIRCUIT DIAGRAM
PROJECT. EAI - 1000
DRAWN. V.G.B.
DATE.
DESIGNER
SHT. NO.

FIG 8.2.2

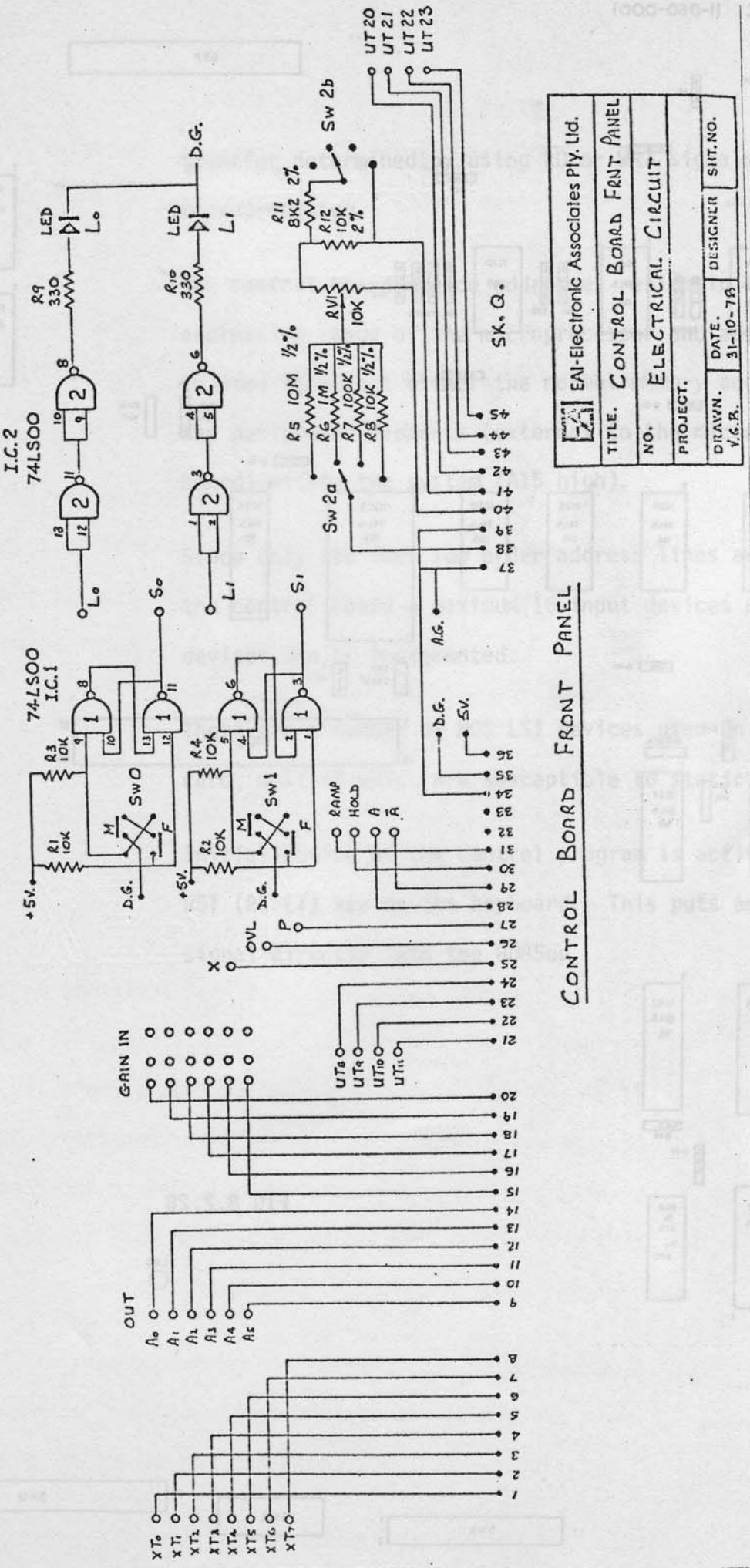

CONTROL BOARD FRONT PANEL
EAI-Electronic Associates Pty. Ltd.
TITLE. CONTROL BOARD FRNT PANEL
NO. ELECTRICAL CIRCUIT
PROJECT.
DRAWN. V.G.R.
DATE. 31-10-78
DESIGNER
SHT. NO.
I.C.2 74LS00
I.C.1 74LS00
LED
R9 330
R10 330
R11 8K2 2%
R12 10K 2%
RV1 10K
R5 10M ½%
R6 1M ½%
R7 100K ½%
R8 10K ½%
R1 10K
R2 10K
R3 10K
R4 10K
Sw 2a
Sw 2b
Sw0
Sw1
D.G.
A.G.
+5V.
SK. Q.
GAIN IN
OUT
RAMP
HOLD
OVL
UT20
UT21
UT22
UT23

Fig. 8.2.2 C

LAYOUT COMPONENT SIDE 11-060-0001

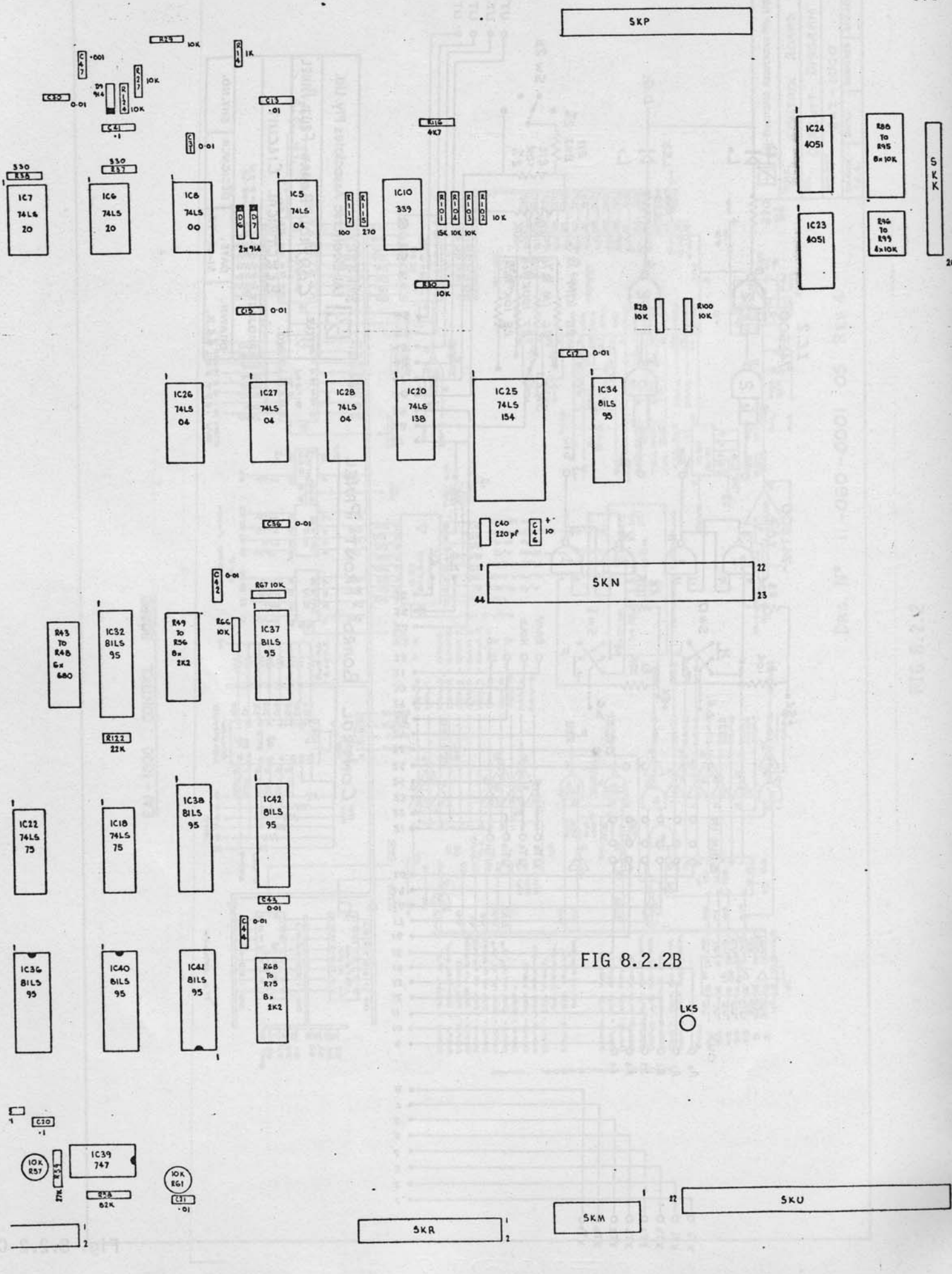


FIG 8.2.2B

transfer determined by using $\overline{RD}$ or $\overline{WRT}$ signals from the microprocessor.

The control board device addresses reside in the upper 32K addressing range of the microprocessor and address bit 15 (A15) is used to select either the normal memory access (A15 low) or the peripheral elements (external to the microprocessor board) within the system (A15 high).

Since only the four low order address lines are decoded on the control board a maximum 16 input devices and 16 output devices can be implemented.

There are a number of MOS LSI devices used on the microprocessor card, most of which are susceptible to static changes.

Initialization of the control program is activated by the RST (RESET) key on the keyboard. This puts an active low signal directly into the 8085up.

8.2.3 Microprocessor Card (Ref Fig 8.2.3)

The EAI-1000 system derives its overall control from the microprocessor card. The microprocessor is an Intel 8085 which incorporates a multiplexed Data address bus.

Two kilobytes of EPROM (IC3, IC6) contain the basic operating firmware and 256 bytes of RAM (IC7, IC8) is used by the firmware for the storage of data and variables

IC9 position is provided for future memory expansion on the microprocessor board. Further memory expansion is possible with the on board decoding for up to 7K bytes of EPROM (IC5) and 1.5K bytes of RAM (IC4) total. A daughter board is required to fully utilise this capacity.

An 8212 eight bit latch (IC2) sychronized by the ALE signal holds the low order eight bits of the address bus to allow sixteen address lines to be utilised through the 8095 instruction cycle.

Data and address bus buffering is not performed on the microprocessor card but all the data lines, FIVE address lines (A0, A1, A2, A3, A15) and control signals ($\overline{RD}$, $\overline{WRT}$) are present at the control board edge connector. These signals are buffered and further decoded on the control board to achieve device selection and data transfer to/ from the various devices within the computer.

Interchange of data between the microprocessor and the control board peripherals is through memory mapping techniques. The device address is decoded and the direction of data

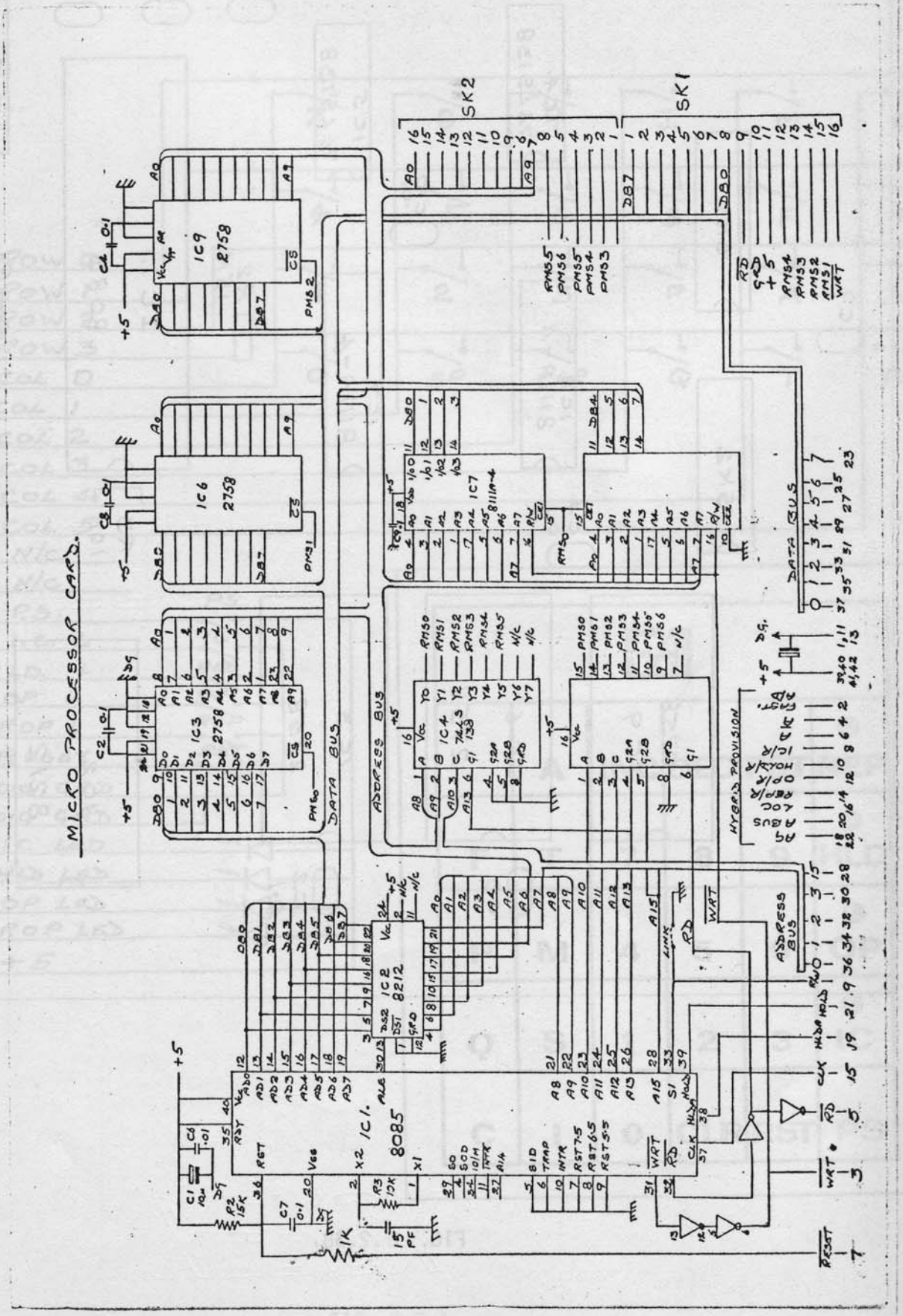

MICRO PROCESSOR CARD.
SK2
SK1
IC9 2758
IC6 2758
IC3 2758
IC7 8111-4
IC4 74LS 138
IC2 8212
IC1. 8085
DATA BUS
ADDRESS BUS
DATA BUS
HYBRID PROVISION
+5
RESET
WRT
RD

FIGURE 8.2.3

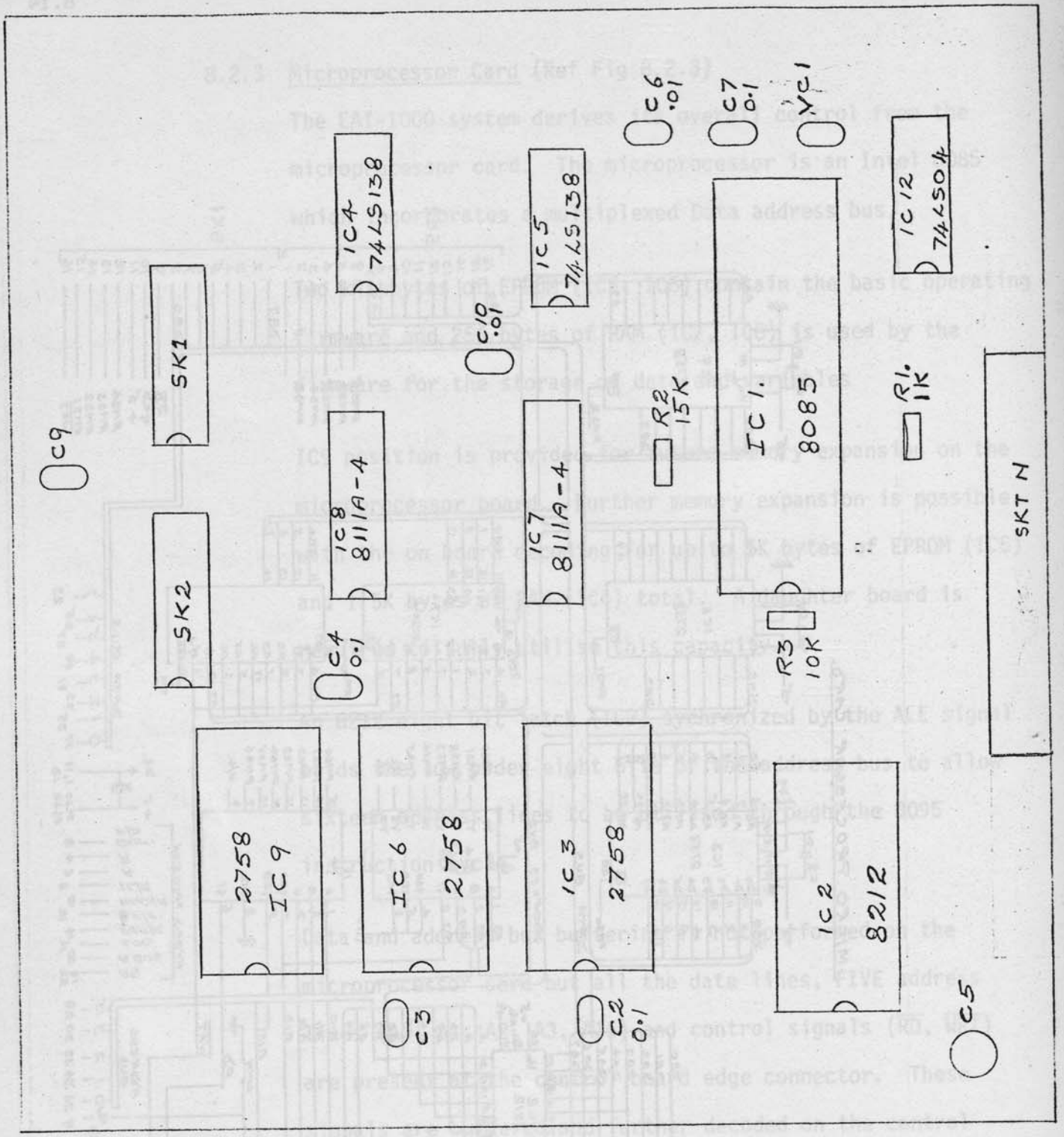

MICRO-PROCESSOR BOARD
C9
SK1
SK2
IC4 74LS138
IC8 8111A-4
C4 0.1
C10 0.01
IC5 74LS138
IC7 8111A-4
C6 .01
C7 0.1
VC1
R2 15K
IC 1. 8085
R1. 1K
IC 12 74LS04
SKT N
R3 10K
2758 IC 9
IC 6 2758
IC 3 2758
IC 2 8212
C3
C2 0.1
C5

FIG. 8.2.3B.

KEYBOARD

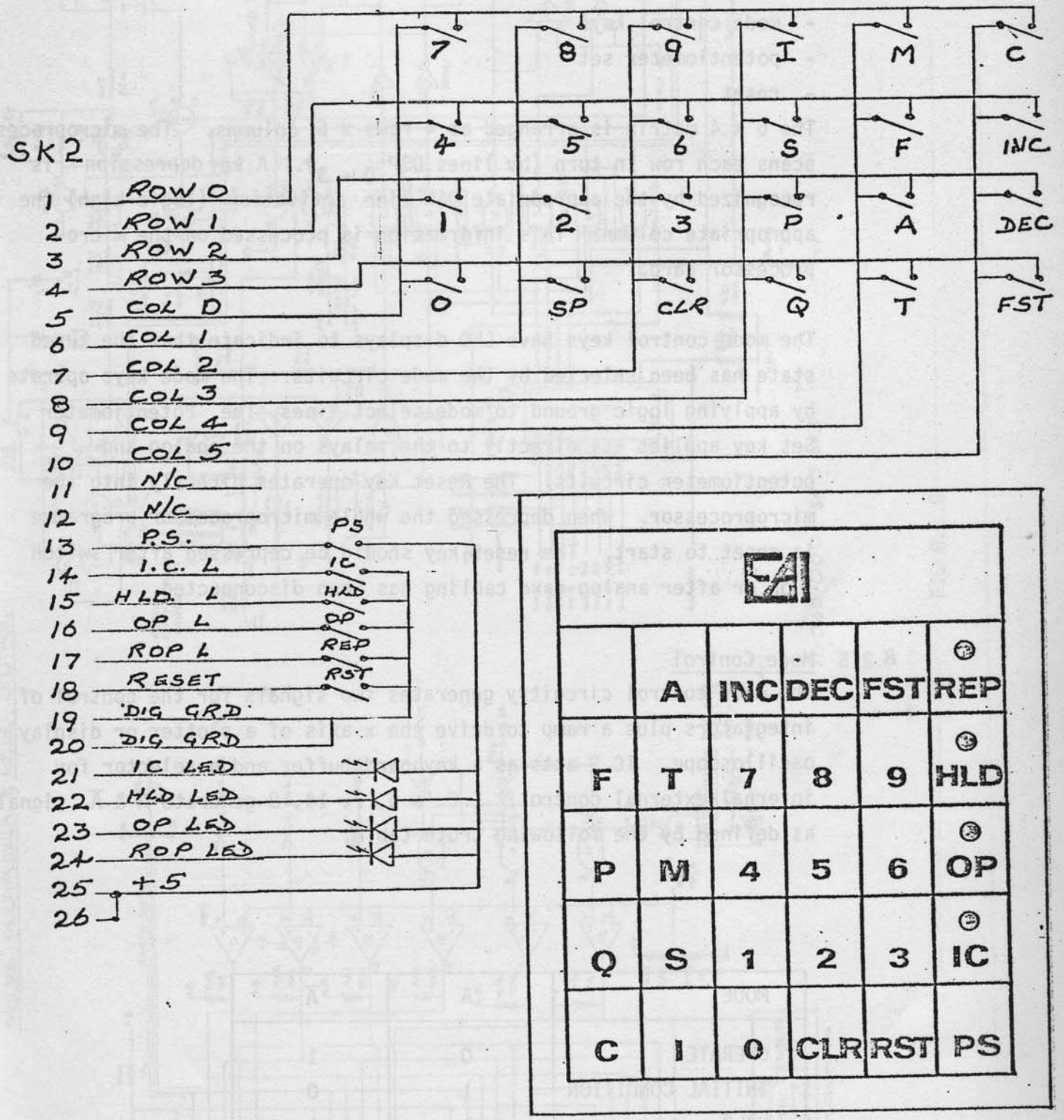


FIG. 8.2.4

8.2.4 Keyboard

Instructions for control of the computer are entered via the keyboard. Electrically the keys are organised into four groups

- a matrix in a 6 x 4 matrix
- mode control keys
- potentiometer set
- reset

The 6 x 4 matrix is arranged as 4 rows x 6 columns. The microprocessor scans each row in turn (by lines DSP $_{0-3}$). A key depression is recognized by the appropriate DSR line activating (logic high) the appropriate column. This information is processed on the microprocessor card.

The mode control keys have LED displays to indicate that the keyed state has been selected by the mode circuits. The mode keys operate by applying logic ground to mode select lines. The Potentiometer Set key applies +5v directly to the relays on the analog and potentiometer circuits. The Reset Key operates directly into the microprocessor. When depressed the whole microprocessor programme is reset to start. The reset key should be depressed after switch - on or after analog card cabling has been disconnected.

8.2.5 Mode Control

The mode control circuitry generates two signals for the control of integrators plus a ramp to drive the x axis of a plotter or display oscilloscope. IC 9 acts as a keyboard buffer and a selector for internal/external control. I.C.'s 6, 7, 14, 8 generate A & $\overline{A}$ signals as defined by the following truth table.

MODE	A	$\overline{A}$
OPERATE	0	1
INITIAL CONDITION	1	0
HOLD	1	1
REP-OP	Alternating	Alternating

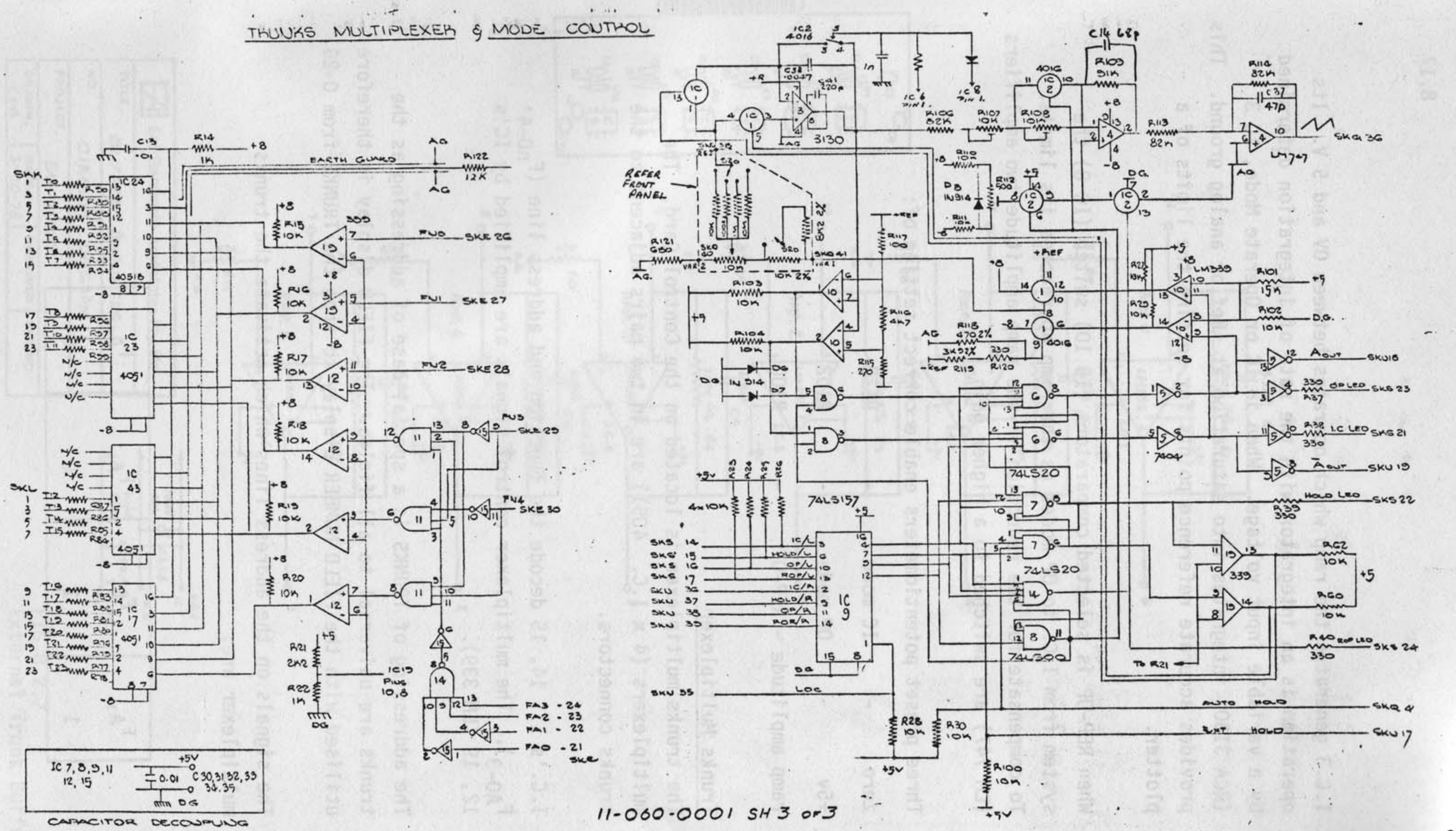

TRUNKS MULTIPLEXER & MODE CONTROL
EARTH GUARD
REFER FRONT PANEL
74LS157
74LS20
74LS00
LM339
LM747
3130
4016
4051
AUTO HOLD
EXT HOLD
CAPACITOR DECOUPLING
11-060-0001 SH 3 OF 3

FIG 8.2.6

I.C.3 generates the ramp which operates between OV and 5 V. Its operation is an integrator with the rate of integration determined by a variable input voltage. When in IC or Operate Mode, IC 3 (RCA 3130) integrates into saturation at +Ref or analog ground. This provides accurate reference points for setting the limits of a plotter.

When REP-OP is selected comparators (IC 10) switch (IC 8) the system from I.C. to OP modes as the ramp approaches its limits. To compensate for the reduction in the ramp amplitude two amplifiers (LM 747) are switched to a higher gain.

Three preset potentiometers enable correct setting of:

zero	-	IC mode	-	R112
+5v	-	OP mode	-	R102
ramp amplitude	-	REP-OP	-	R100

8.2.6 Trunks Multiplexer

The trunks multiplexer is located on the Control Card. The multiplexers (4 x I.C. 4051) are in two pairs adjacent to the trunks connectors.

I.C.'s 11, 14, 15 decode the function and address line (F_{nO-4}, F_{AO-3}). The multiplexer control signals are amplified by IC's 12, 19 (LM 339).

The addressing of TRUNKS is a special case of addressing as the trunks are universal to all fields. The FIELD display is therefore utilised with the FIELD NUMBER display to show the TRUNKS from 0-23.

The signals on the address lines which activate the trunks multiplexer are:

F_{A_3}	F_{A_2}	F_{A_1}	F_{A_0}
1	1	0	0

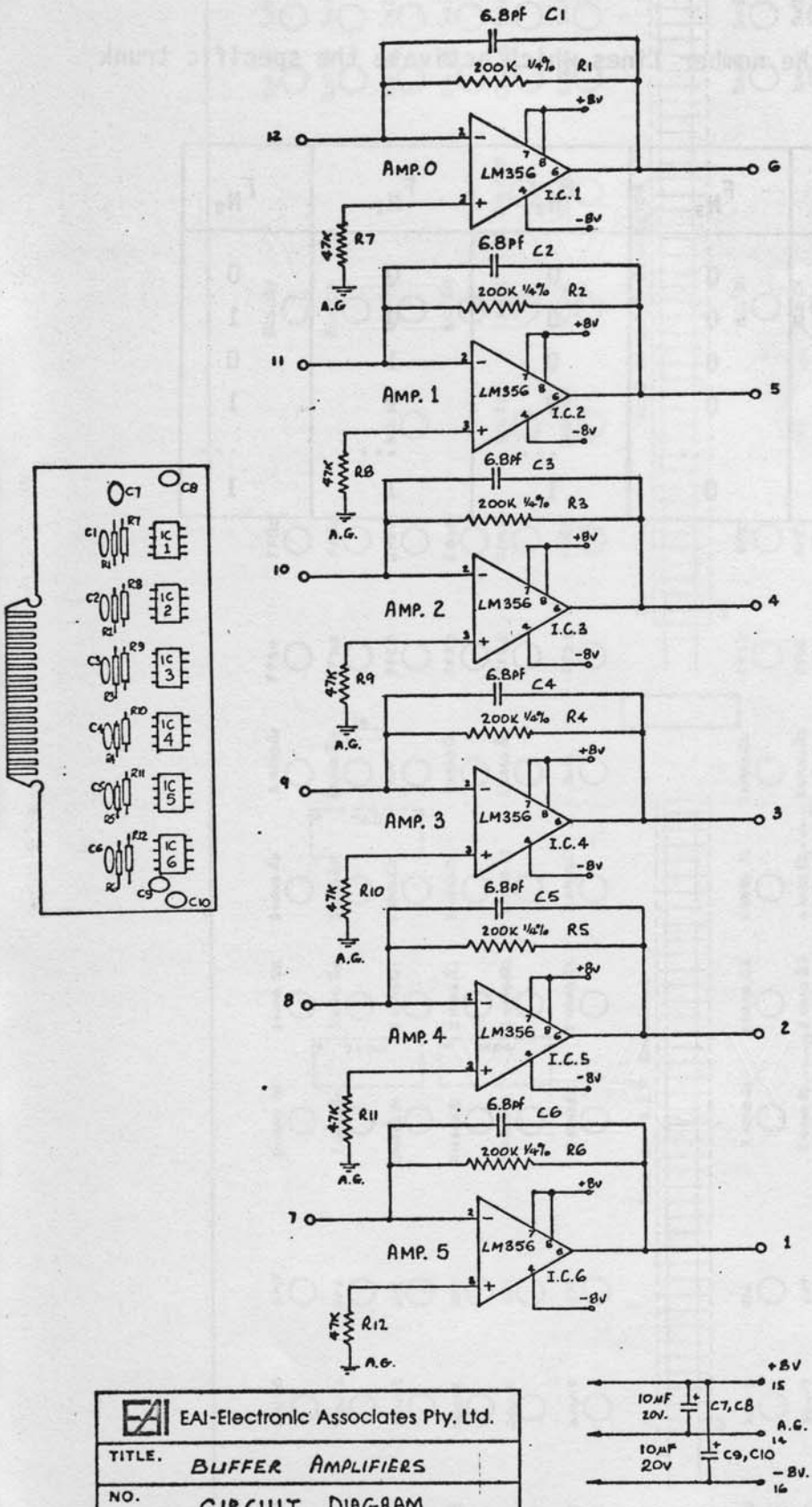


FIG 8.2.7
External Trunk Buffer (Option)

The signals on the number lines which activate the specific trunk selection are:

TRUNK	F_{N_4}	F_{N_3}	F_{N_2}	F_{N_1}	F_{N_0}
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
.....	...	...	...	...	...
23	1	0	1	1	1

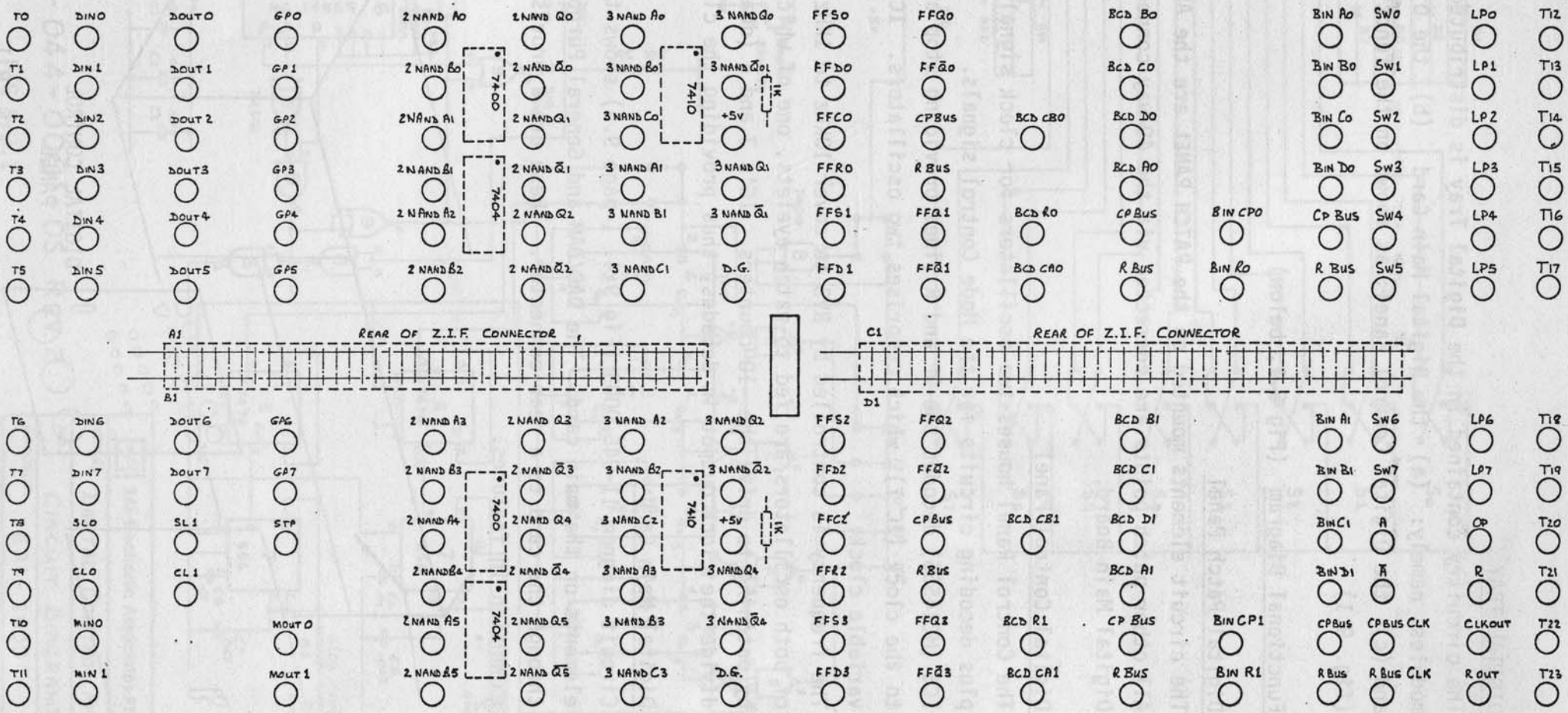

T0 DIN0 DOUT0 GP0 2 NAND A0 2 NAND Q0 3 NAND A0 3 NAND Q0 FFS0 FFQ0 BCD B0 BIN A0 SW0 LP0 T12
T1 DIN1 DOUT1 GP1 2 NAND B0 2 NAND Q0 3 NAND B0 3 NAND Q0 FFD0 FFQ0 BCD C0 BIN B0 SW1 LP1 T13
T2 DIN2 DOUT2 GP2 2NAND A1 2 NAND Q1 3 NAND C0 +5V FFC0 CPBUS BCD CB0 BCD D0 BIN C0 SW2 LP2 T14
T3 DIN3 DOUT3 GP3 2 NAND B1 2 NAND Q1 3 NAND A1 3 NAND Q1 FFR0 R BUS BCD A0 BIN D0 SW3 LP3 T15
T4 DIN4 DOUT4 GP4 2 NAND A2 2 NAND Q2 3 NAND B1 3 NAND Q1 FFS1 FFQ1 BCD R0 CP BUS BIN CP0 CP BUS SW4 LP4 T16
T5 DIN5 DOUT5 GP5 2 NAND B2 2 NAND Q2 3 NAND C1 D.G. FFD1 FFQ1 BCD CA0 R BUS BIN R0 R BUS SW5 LP5 T17
7400
7410
1K
7404
A1
REAR OF Z.I.F. CONNECTOR
B1
C1
REAR OF Z.I.F. CONNECTOR
D1
T6 DIN6 DOUT6 GP6 2 NAND A3 2 NAND Q3 3 NAND A2 3 NAND Q2 FFS2 FFQ2 BCD B1 BIN A1 SW6 LP6 T18
T7 DIN7 DOUT7 GP7 2 NAND B3 2 NAND Q3 3 NAND B2 3 NAND Q2 FFD2 FFQ2 BCD C1 BIN B1 SW7 LP7 T19
T8 SLO SL1 STP 2 NAND A4 2 NAND Q4 3 NAND C2 +5V FFC2 CPBUS BCD CB1 BCD D1 BIN C1 A OP T20
T9 CLO CL1 2 NAND B4 2 NAND Q4 3 NAND A3 3 NAND Q4 FFR2 R BUS BCD A1 BIN D1 Ā R T21
T10 MIN0 MOUT0 2 NAND A5 2 NAND Q5 3 NAND B3 3 NAND Q4 FFS3 FFQ2 BCD R1 CP BUS BIN CP1 CPBUS CPBUS CLK CLKOUT T22
T11 MIN1 MOUT1 2 NAND B5 2 NAND Q5 3 NAND C3 D.G. FFD3 FFQ3 BCD CA1 R BUS BIN R1 R BUS R BUS CLK ROUT T23
7400
7404

FIG 9.2.1

9.0 DIGITAL TRAY

The circuitry contained in the Digital Tray is distributed on the three modules, namely: (a) the Digital Main Card (b) the Digital Patch Pan and (c) the Digital Control Panel; as shown on the functional diagram (fig. 9.1)

9.1 Functional Diagram (Fig 9.1, below)

9.2 Digital Patch Panel

The circuit elements mounted on the PATCH PANEL are the AND/NAND gates. All other patch points are connected via the 40-way connectors to the Digital Main Board.

9.3 Digital Control Panel

The Control Panel houses two oscillators for clock signal generation plus decoding circuits for the Mode Control signals.
IC6 (MC14555) decodes the OP and R lines providing stop and run commands to the clock (IC 7), which comprises two oscillators. IC7B is the variable clock.
The frequency is controlled by RV3 to cover 10KHz to 1KHz. The outputs of both oscillators are fed to patch eyelets, one of which is selected by patching to drive the -10 counters. IC's 3 and 4 (dual decode counter divide the clock output in decades, thus providing the clock bus signals.

9.4 Digital Main Card

Circuit diagram 11-045.0003 (Fig 9.4. , page 9.5) shows the circuit elements on the main card. The DAC/DAM and General Purpose lines run through the card to a rear connector. These are a provision for future expansion in features.

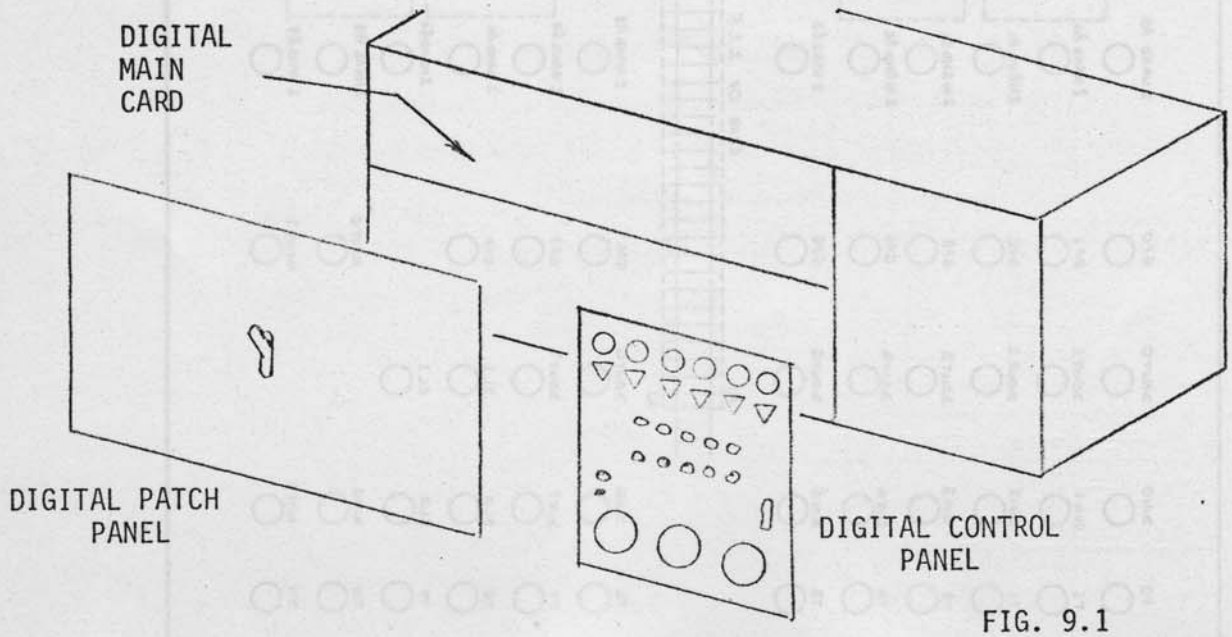
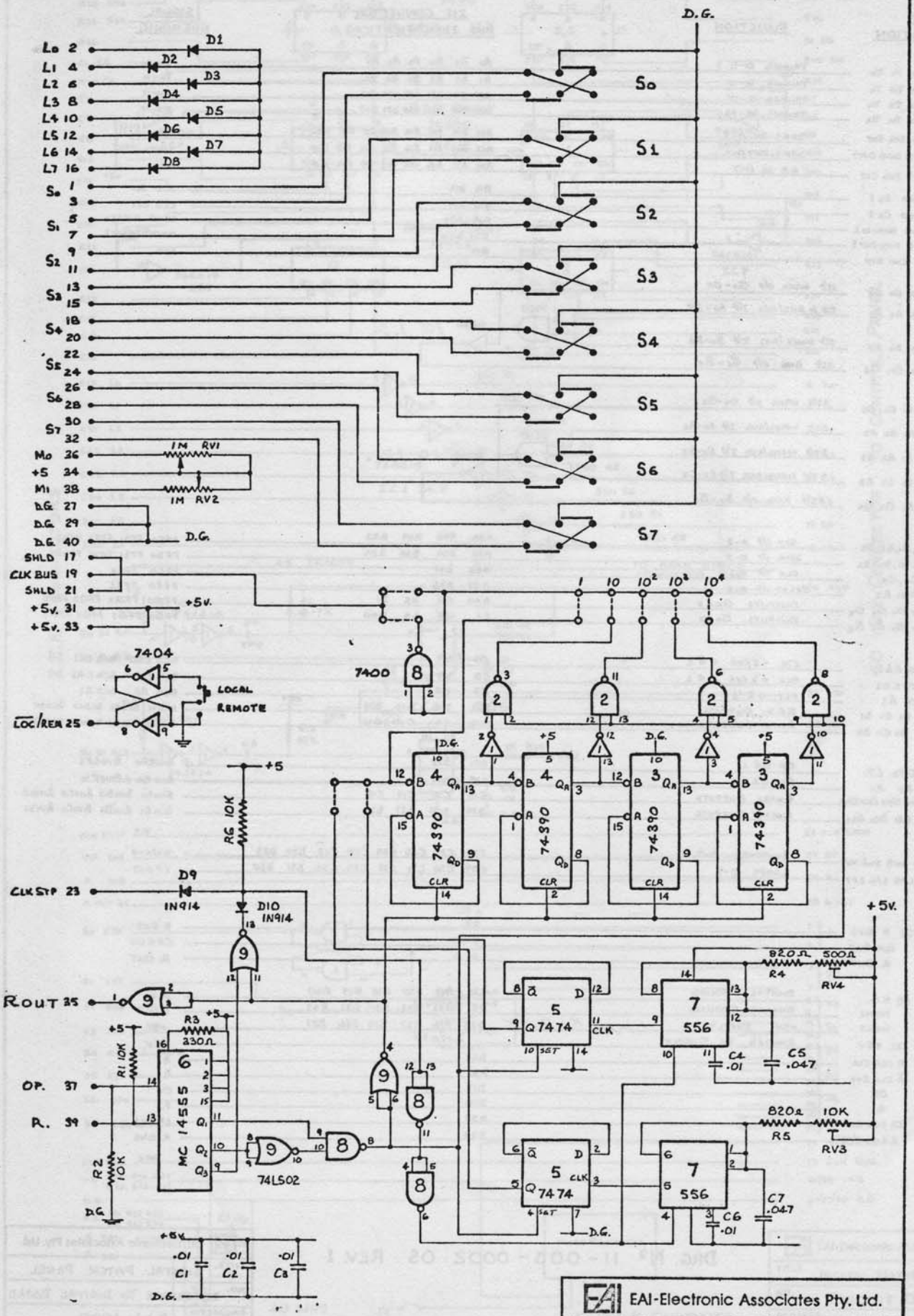


FIG. 9.1



EAI-Electronic Associates Pty. Ltd.

TITLE.	DIGITAL CONTROL PANEL
NO.	CIRCUIT DIAGRAMS
PROJECT.	EAI - 1000

DRG. Nº 11-044-0001-05 REV. 2

FIG 9.3.1

EYELET IDENTIFICATION	FUNCTION	ZIF CONNECTOR PIN IDENTIFICATION	SIGNAL NMEMONIC
To T1 T2 T3 T4 T5	TRUNKS 0-5	A6 A5 A4 A3 A2 A1	To-5
T6 T7 T8 T9 T10 T11	TRUNKS 6-11	B1 B2 B3 B4 B5 B6	T6-11
T12 T13 T14 T15 T16 T17	TRUNKS 12-17	C35 C36 C37 C38 C39 C40	T12-17
T18 T19 T20 T21 T22 T23	TRUNKS 18-23	D36 D36 D37 D38 D39 D40	T18-23
DINO IN1 IN2 IN3 IN4 IN5 IN6 IN7	DAMS IN 0-7	A22 A19 A16 A13 A10 A7 B8 B9	DINO-7
OUTO OUT1 OUT2 OUT3 OUT4 OUT5 OUT6 OUT7	DAMS OUT 0-7	A25 A20 A17 A14 A11 A8 B7 B10	DOUTO-7
INO IN1 IN2 IN3 IN4 IN5 IN6 IN7	G.P. IN 0-7	A24 A21 A18 A15 A12 A9 B12 B11	GP0-7
SLO SL1		B18 B14	SLO SL1
CLO CL1		B16 B17	CLO CL1
MONO IN0 MONO IN1		B19 B22	MINO MIN1
MONO OUT0 MONO OUT1		B21 B24	MOUTO MOUT1
CLK STP		B15	STP
Ao Q A1 Q2 A3 Q4	2I/P NAND O/P Qo-Q5		
Bo A1 A2 B3 A4 A5	2I/P NAND/AND I/P Ao-A5	7400	
Bo B1 B2 B3 B4 B5	2I/P NAND/AND I/P Bo-B5	7404 IC 1.2.	
$\bar{Q}_0$ $\bar{Q}_1$ $\bar{Q}_2$ $\bar{Q}_3$ $\bar{Q}_4$ $\bar{Q}_5$	2I/P AND O/P $\bar{Q}_0$-$\bar{Q}_5$	IC 3,4	
Qo Q1 Q2 Q3	3I/P NAND O/P Qo-Q2		
Ao A1 A2 A3	3I/P NAND/AND I/P Ao-A2	7410	
Bo B1 B2 B3	3I/P NAND/AND I/P Bo-B3	7404 IC 1,2.	
Co C1 C2 C3	3I/P NAND/AND I/P Co-C3	IC 5,6	
$\bar{Q}_0$ $\bar{Q}_1$ $\bar{Q}_2$ $\bar{Q}_3$	3I/P AND O/P $\bar{Q}_0$-$\bar{Q}_3$		
D/FLIP FLOPS So,S1,S2,S3	SET I/P 0-3	A34 A38 B39 B35	FFSo FFS1 FFS2 FFS3
D/FLIP FLOPS Do.D1.D2.D3	DATA I/P 0-3	A35 A39 B38 B34	FFDo FFD1 FFD2 FFD3
D/FLIP FLOPS Co, C2	CLK I/P 0,2	A36 B37	FFCO FFC2
D/FLIP FLOPS Ro. R2	RESET I/P 0.2	A37 B36	FFRo FFR2
D/FLIP FLOPS Qo Q1 Q2 Q3	OUTPUTS Qo-3	A40 C4 D5 D1	FFQo FFQ1 FFQ2 FFQ3
D/FLIP FLOPS $\bar{Q}_0$ $\bar{Q}_1$ $\bar{Q}_2$ $\bar{Q}_3$	OUTPUTS $\bar{Q}_0$-3	C1 C5 D4 B40	FF$\bar{Q}$o FF$\bar{Q}$1 FF$\bar{Q}$2 FF$\bar{Q}$3
B.C.D.CTR. CB0, CB1	CLK. ÷ECTR 0 & 1	C6 D9	BCD CBO BCD CB1
B.C.D.CTR. CA0, CA1	CLK ÷2 CTR 0 & 1	C8 D7	BCD CAO BCD CA1
B.C.D.CTR. RO. R1	RST 0 & 1	C7 D8	BCD RO BCD R1
B.C.D.CTR. A1 B1 C1 D1	B.C.D. OUTPUTS	D12 D15 D14 D13	BCDA1 BCDB1 BCDC1 BCDD1
B.C.D.CTR. Ao Bo Co Do	B.C.D. OUTPUTS	C12 C9 C10 C11	BCDAO BCDBO BCDCO BCDDO
BINARY CTR. CPo CP1	CK 0 & 1	C21 D22	BINCPo BINCP1
BINARY CTR. Ro R1	RST 0 & 1	C19 D23	BIN Ro BIN R1
BINARY CTR. QAO QBO QCO QDO	BINARY OUTPUTS	C15 C16 C17 C18	BINAO BINBO BINCO BINDO
BINARY CTR. QA1 QB1 QC1 QD1	BINARY OUTPUTS	D29 D28 D27 D26	BINA1 BINB1 BINC1 BIND1
SWO SW1 SW2 SW3 SW4 SW5 SW6 SW7	SWITCHES 0-7	C28 C27 C26 C25 C24 C23 D34 D33	SWo-7
LPO LP1 LP2 LP3 LP4 LP5 LP6 LP7	LAMPS 0-7	C29 C30 C31 C32 C33 C34 D21 D20	LPo-7
(2) R BUS		D6	R BUS
CLK OUT		D30	CP BUS
R OUT		D 6	R OUT
(2) D.G.	DIGITAL GROUND	A28 A29 A30 B28 B29 B30	D.G.
NONE	ANALOG GROUND	A31 A32 A33 B31 B32 B33	A.G.
NONE	+5V SUPPLY	R1,2. 1K A25 A26 A27 B25 B26 B27	+5V.
(2) +5V	LIMITED 5V. SUPPLY		+5V.
A CLK CTR		D32	A
$\bar{A}$ CLK CTR		D31	$\bar{A}$
OP.		D19	OP
R.		D18	R
CP BUS CLK		D25	CP BUS
R BUS CLK		D24	R BUS

DRG. Nº 11-005-0002 OS REV. 1

EAI-Electronic Associates Pty. Ltd.			
TITLE. DIGITAL PATCH PANEL			
NO. INTERFACE TO DIGITAL BOARD			
PROJECT. E.A.I. 1000			
DRAWN. V.B.B.	DATE. 20-2-79	DESIGNER	SHT. NO.

FIG 9.2.2

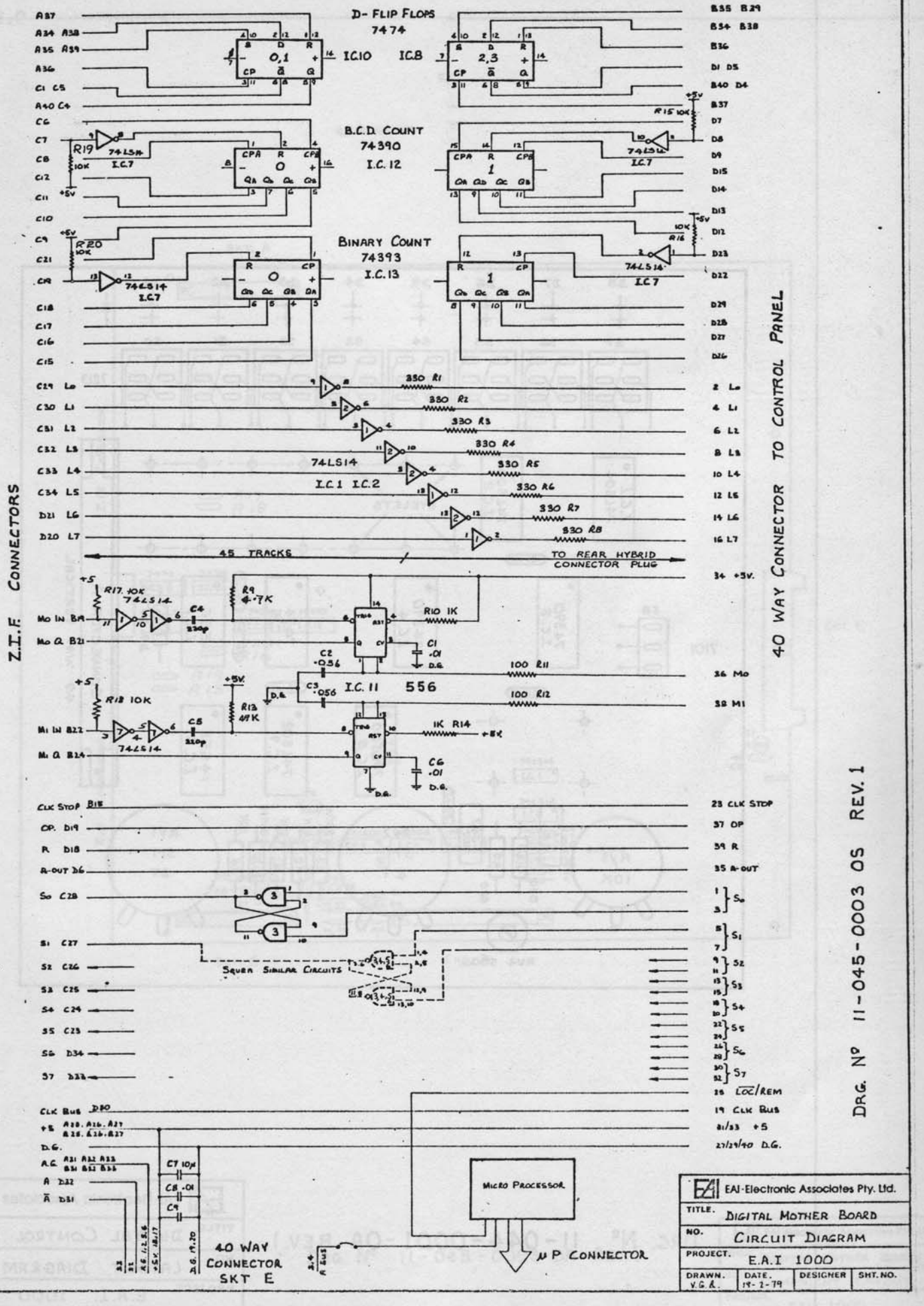
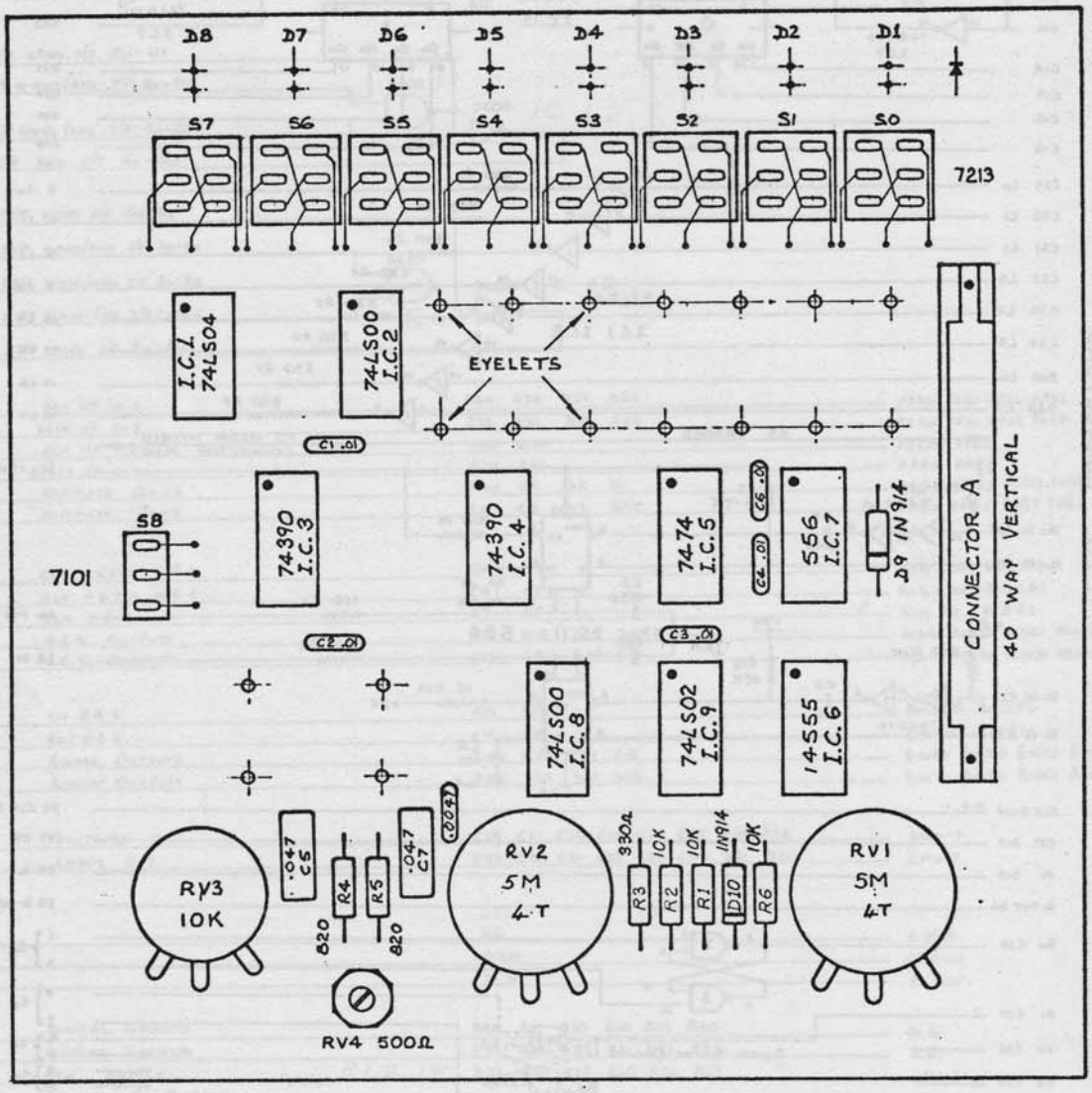

D- FLIP FLOPS
7474
IC.10
IC.8
B.C.D. COUNT
74390
I.C. 12
BINARY COUNT
74393
I.C. 13
74LS14
I.C.1 I.C.2
330 R1
330 R2
330 R3
330 R4
330 R5
330 R6
330 R7
330 R8
45 TRACKS
TO REAR HYBRID CONNECTOR PLUG
Z.I.F. CONNECTORS
40 WAY CONNECTOR TO CONTROL PANEL
R17 10K
R9 4.7K
R10 1K
R18 10K
R13 4.7K
R14 1K
100 R11
100 R12
C1 .01
C2 .056
C3 .056
I.C. 11 556
C4 330p
C5 330p
C6 .01
SQUEN SIMILAR CIRCUITS
CLK STOP
CP.
R
A-OUT
CLK BUS
D.G.
A.C.
C7 10M
C8 .01
C9
MICRO PROCESSOR
40 WAY CONNECTOR SKT E
µP CONNECTOR
DRG. Nº 11-045-0003 OS REV. 1
EAI-Electronic Associates Pty. Ltd.
TITLE. DIGITAL MOTHER BOARD
NO. CIRCUIT DIAGRAM
PROJECT. E.A.I 1000
DRAWN. V.G.A.
DATE. 19-2-79
DESIGNER
SHT. NO.

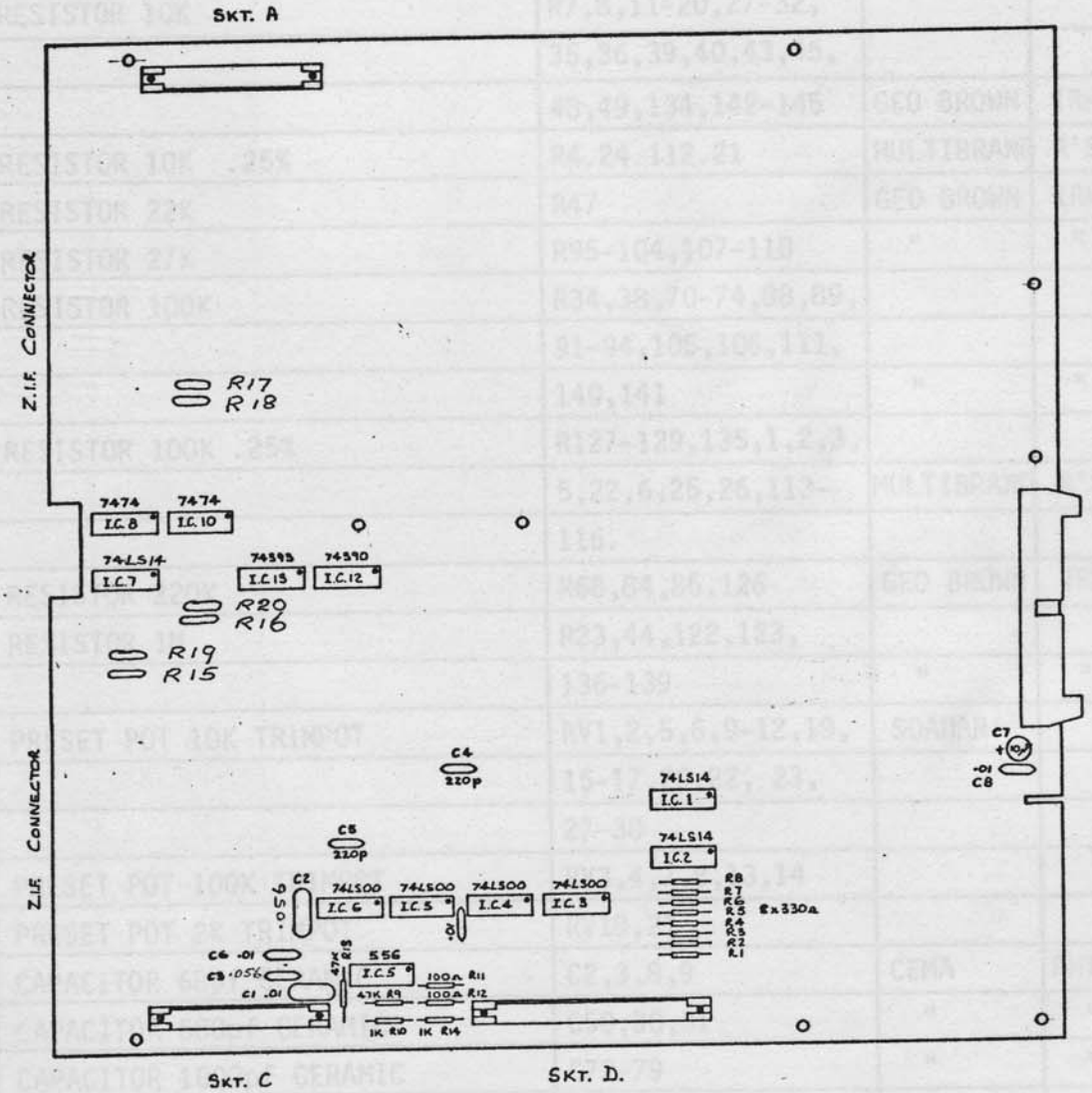
FIG 9.4.1



DRG. Nº 11-044-0001-0A REV.1

FIG 9.3.2

EAI-Electronic Associates Pty.			
TITLE. DIGITAL CONTROL PAN			
NO. LAYOUT DIAGRAM			
PROJECT. E.A.I. 1000			
DRAWN. V.G.B.	DATE. 26-2-79	DESIGNER	SHT



DRG. Nº 11-045-0003 0A REV. 1

EAI-Electronic Associates Pty. Ltd.			
TITLE. DIGITAL MOTHER BOARD			
NO. – COMPONENT LAYOUT			
PROJECT. EAI · 1000			
DRAWN. VEZ	DATE. 19-2-79	DESIGNER	SHT. NO.

FIG 9.4.2

EAI-ELECTRONIC ASSOCIATES PTY. LIMITED

PARTS LIST
ANALOG CARD
11-45-0001

ITEM	DESCRIPTION	DWG. REF.	SOURCE	MAKE	SUPPLI MFG RE
32	RESISTOR 10K	R7,8,11-20,27-32,			
		35,36,39,40,43,45,			
		48,49,134,142-145	GEO BROWN	IRH	
33	RESISTOR 10K .25%	R4.24.112.21	MULTIBRAND	R'STEIN	10K25%
34	RESISTOR 22K	R47	GEO BROWN	IRH	CR25
35	RESISTOR 27K	R95-104,107-110	"	"	
36	RESISTOR 100K	R34,38,70-74,88,89,			
		91-94,105,106,111,			
		140,141	"	"	
37	RESISTOR 100K .25%	R127-129,135,1,2,3,			
		5,22,6,25,26,113-	MULTIBRAND	R'STEIN	100K
		116.			
38	RESISTOR 220K	R68,84,85,126	GEO BROWN	IRH	CR.25
39	RESISTOR 1M	R23,44,122,123,			
		136-139	"	"	
40	PRESET POT 10K TRIMPOT	RV1,2,5,6,9-12,19,	SOANAR		
		15-17,20,22, 23,			
		27-30			VTP-1
41	PRESET POT 100K TRIMPOT	RV3,4,7,8,13,14			VTP 1
42	PRESET POT 2K TRIMPOT	RV18,21			VTP-2
43	CAPACITOR 68pf CERAMIC	C2,3,8,9	CEMA	PHILIPS	632-1
44	CAPACITOR 680pf CERAMIC	C50,30,31	"	"	630-0
45	CAPACITOR 1000pf CERAMIC	C72-79	"	"	630-0
46	CAPACITOR 2700pf 100V +10% POLY	C43-46	SOANAR		
47	CAPACITOR 4700pf 100V +10% POLY	C19,22	"		
48	CAPACITOR .01uf CERAMIC	C1,11,16,17,24,28,			
		29,33,34,36,38,39,			
		49,52,53,55,56,			
		64-68,80,81	CEMA	.01ufCER	629-0
49	CAPACITOR .0105uf ±2% P/S	C4-7	ALLIED CAP	TCS	.0105
50	CAIACPTOR .1mf CERAMIC	C10,25,40,60,71,			
		18,51,82-87			
51	CAPACITOR 1.05mf ±2% POLY/STYR	C41,42,47,48	"	"	1.05
52	CAPACITOR TANT 10mf 20V	C20,24,26,35,32	"	"	

EAI-ELECTRONIC ASSOCIATES PTY. LIMITED

PARTS LIST

ANALOG CARD

11-45-0001

ITEM	DESCRIPTION	DWG. REF.	SOURCE	MAKE	SUPPLIE MFG REF
1	IC LM311	IC28,29,47,50,	ICS	NS	LM311N
2	IC LM339	IC7,8,22,36,38,41	"	"	LM339N
3	IC LM741	IC24,25,26	"	"	LM741N
4	IC LM747	IC1,2,12,13	"	"	LM747N
5	IC CA3140T	IC3,4,10,11	AMTRON	"	CA3140A
6	IC LF356	IC14 - 21	ICS	"	LF356N
7	IC 4016	IC51	"	"	CD4016E
8	IC4051	IC34,35,37,39,42,43	"	"	CD4051E
9	IC 4066	IC5,6	TOTAL	MOTOROLA	MC1406
10	IC 74LS00	IC9,49	ICS	NS	DM74LS
11	IC 74LS04	IC27,44	"	"	DM74LS
12	IC 74LS10	IC40	"	"	DM74LS
13.	IC74LS20	IC45	"	"	DM74LS
14	IC 74LS74	IC30	"	"	DM74LS
15	IC 7486	IC46	"	"	DM7486
16	IC TL191	IC23	"	TEXAS	TL191C
17	IC AD534J	IC31,32	PARAMETERS	AD	AD534J
18	TRANSISTOR 2N3646 (P/N 3646)	TR4	ICS	RIFA	
19	TRANSISTOR FET2N4393	TR1,2	"	"	
20	TRANSISTOR FET 2N4340	TR(5,6), (7,8)	"	" (MATCHED PA	
21	TRANSISTOR TIP31	TR3	"	"	
22	DIODE IN914	D1	"	TEXAS	IN914
23	RELAY 4 POLE C/O	RL1	MULTIBRAND	DAVALL	26/4c
24	RESISTOR 180 ohm	R42	GEO BROWN	IRH	CR25
25	RESISTOR 470 ohm	R46	"	"	
26	RESISTOR 820 ohm	R11,20	"	"	
27	RESISTOR 1Kohm	R9,10,52-59,77,90, 117,118	"	"	
28	RESISTOR 1K2	R41	"	"	
29	RESISTOR 2K2	R33,37,60-67,80-83, 86,87,124,125	"	"	
30	RESISTOR 3K9	R50,51	"	"	
31	RESISTOR 5K6	R75,76	"	"	

EAI-ELECTRONIC ASSOCIATES PTY. LIMITED

PARTS LIST

POTENTIOMETER PANEL

11-42-0001

ITEM	DESCRIPTION	DWG. REF.	SOURCE	MAKE	SUPPLIE MFG REF
1	PC CARD	042-0100			
2	LEGEND PANEL	11-042-0001L	PH'TRONICS		
3	IC TL083	IC1-5	ICS	TEXAS	TL083AC
4	TRANSISTOR TIP31	TR1	"		
5	POTENTIOMETER 10K CERMET	VR11-20		SOANAR	VTP 10K
6	POTENTIOMETER 10K 4T	VR1-10	MORGANITE	MORGANITE	19M121
7	RELAY 6P c/o	RL1	M'BRAND	DAVALL	466cc-5
8	RELAY 4P c/O	RL2	"	"	244cc-1
9	DIODE IN914	D1	ICS	TEXAS	IN 91
10	CAPACITOR 0.1 CER	C1-5	"	"	
11	LED - HIGH EFFICIENCY	L1	AT	HP	5082-4(
12	16 PIN DIL SKT	SKT P.Q.	XENITEC		ICN163
13	RESISTOR 10K	R2	RIFA	IRH	GLP
14	RESISTOR 2K2	R1	"	"	
15	RESISTOR 8K2				
16	CAPACITOR 68pf				

EAI-ELECTRONIC ASSOCIATES PTY. LIMITED

PARTS LIST
ANALOG CARD
11-45-0001

ITEM	DESCRIPTION	DWG. REF.	SOURCE	MAKE	SUPPLI MFG RI
53	CAPACITOR TANT 10mf 35V	C27	ICS		
54	16 WAY DIL SOCKET	F.G.H.J.	XENITEC		ICN163
55	26 WAY PLUG	K,L	AMPEC	HIROSE	3E26P2
56	40 WAY PLUG, RIGHT ANGLE	E	"	"	3E40P2
57	DIGI SWITCH	DIP SW	XENITEC		GF008
58	RESISTOR 2K7 5%	R69,78	GEO BROWN	IRH	CR25
59	TRANSISTOR SKT 3 WAY		TOTAL		8059-
60	TRANSISTOR SKT 6 WAY		"		805-1

EAI-ELECTRONIC ASSOCIATES PTY. LIMITED

PARTS LIST
CONTROL CARD
11-02-0012

ITEM	DESCRIPTION	DWG. REF.	SOURCE	MAKE	SUPPLIE MFG REF
1	PC BOARD	11-060-0001			
2	IC LM339	IC10,12,19	ICS	NS	LM339N
3	IC UT747	IC4,13,16,39	"	"	LM747C
4	IC 3130	IC3			
5	IC 4016	IC1,2	ICS	NS	CD4016
6	IC4051	IC17,23,24,43	"	"	CD4051
7	IC 74LS00	IC8,21	"	"	DM74LS
8	IC 741S04	IC5,15,26,27,28,44.	"	"	DM74LS
9	IC 74LS10	IC11	"	"	DM74LS
10	IC 74LS13	IC33	"	"	DM74LS
11	IC 74LS20	IC6,7,14	"	"	DM74LS
12	IC 7425	IC31	"	"	DM7425
13	IC 74LS75	IC18,22,29	"	"	DM74LS
14	IC 74LS121	IC30	AJF	"	74121
15	IC 74LS138	IC20	ICS	"	DM74LS
16	IC 74LS154	IC25	"	"	DM74LS1
17	IC 81LS95	IC32,34,36-38,40-42	"	"	DM81LS
18	IC MP7550BD	IC35	AMPEC	MPS	MP7550
19	IC 74LS157	IC9	ICS	NS	DM74LS
20	IC AD580	IC45	PARAMETERS	AD	
21	RESISTOR - 100 ohm	R117	RIFA	IRH	GLP
22	RESISTOR - 270 ohm	R115	"	"	"
23	RESISTOR - 330 ohm	R37-40, 120	"	"	"
24	RESISTOR - 470 ohm	R41,42,118	"	"	"
25	RESISTOR - 680 ohm	R43-48,121	"	"	"
26	RESISTOR 1K ohm	R14,22,123	"	"	"
27	RESISTOR 2K2	R21,49-56, 68-75	"	"	"
28	RESISTOR 3K9	R1,6	"	"	"
29	RESISTOR 3K9 2%	R119	"	"	"
30	RESISTOR 4K7	R3,4	"	"	"
31	RESISTOR 10K	R15-20, 23-30, 60,			
		62, 66, 67, 76-100,			
		102-104, 110,111	"	"	"

EAI-ELECTRONIC ASSOCIATES PTY. LIMITED

PARTS LIST

PATCH PANEL ANALOG

11-005-0001

ITEM	DESCRIPTION	DWG. REF.	SOURCE	MAKE	SUPP MFG
1	PC CARD				
2	LEGEND PANEL		PH'TRONICS		
3	ZIF CONNECTOR WITH 6" RELEASE BAR	Z1,2	WLB	AMP	1-5
4	POTENTIOMETER 10K 10T	RV1,2	IRH	CTS	
5	RESISTOR 1K5%	R59	RIFA	IRH	GL
6	RESISTOR 1M ¼W ¼%	R1-3, 8-10, 16-18,			
		21-23,26-28,33-35,			
		40-42,45-47,50	M'BRAND	R'STEIN	1/8
7	RESISTOR 10K ¼W ¼%	R6,7,14,15,31,32,			
		38,39	"	"	1/8
8	RESISTOR 100K ¼W ¼%	R4,5,12,13,19,20,			
		24,25,29,30,36,37,			
		43,44,48,49,53,54,			
		58	"	"	1/8
9	IC 7400	IC1	ICS	NS	DM7
10	CAPACITOR 10uf TAG TANT		"		

EAI-ELECTRONIC ASSOCIATES PTY. LIMITED

PARTS LIST

CONTROL FRONT PANEL

11-020-0001

ITEM	DESCRIPTION	DWG. REF.	SOURCE	MAKE	SUPPLIE MFG REF
1	LED HIGH EFFICIENCY	LO,1	AMTRON	HP	5082-40
2	TOGGLE SWITCH 7213	SWO,1	C & K	C & K	7213
3	IC 74LSOO	IC1,2	ICS	NS	DM74LSO
4	RESISTOR 330 ohm	R9,10	RIFA	IRH	GLP
5	RESISTOR 8K2 2%	R11	"	"	RG¼
6	RESISTOR 10K 2%	R12	"	"	"
7	RESISTOR 10K .25%	R8	M'BRAND	R'STEIN	
8	RESISTOR 100K .25%	R7	"	"	
9	RESISTOR 1M 0.25%	R6	"	"	
10	RESISTOR 10M 2%	R5	RIFA		
11	ROTARY SWITCH	SW2	MSP	MSP	
12	POTENTIOMETER 10K 1T	RV1	IRH	CTS	BL55913
13	RESISTOR 10K	R1-4	RIFA	IRH	GLP

EAI-ELECTRONIC ASSOCIATES PTY. LIMITED

PARTS LIST

CONTROL CARD

11-02-0012

ITEM	DESCRIPTION	DWG. REF.	SOURCE	MAKE	SUPPLIE MFG REF
32	RESISTOR 10K 0.25%	R8,10,11,13	M'BRAND	R'STEIN	1/8w .2
33	RESISTOR 15K	R101	RIFA	IRH	GLP
34	RESISTOR 22K	R122	"	"	"
35	RESISTOR 82K	R58,106,114,133	"	"	"
36	RESISTOR 91K	R109	RIFA	ICS	
37	RESISTOR - 100K 0.25%	R63,64	M'BRAND	R'STEIN	
38	RESISTOR 27K	R59	RIFA	IRH	GLP
39	RESISTOR 1M	R65	"	"	"
40	TRIMPOT 500 ohm	R 12,112	ICS		VTP-5
41	TRIMPOT 1K	R 2,5,9	"		VTP-1
42	TRIMPOT 10K	R 57,61,107,108	"		VTP10
43	CAPACITOR 68pf CERAMIC	C14	ELCOMA	PHILIPS	
44	CAPACITOR 22pf CERAMIC	C12,28	"	"	632-1
45	CAPACITOR 47pf CERAMIC	C37	"	"	632-1
46	CAPACITOR 100pf CERAMIC	C18,19	"	"	632-1
47	CAPACITOR 220pf CERAMIC	C40,41	"	"	630-(
48	CAPACITOR 2n2 POLY	C29	SOANAR		100v±
49	CAPACITOR 4n7 POLY	C38	"		"
50	CAPACITOR 3n3 POLY	C27	"		
51	CAPACITOR 0.01uf CERAMIC	C13,15-17, 21-26, 30-36,47,49	ELCOMA		629-
52	CAPACITOR 0.1uf CERAMIC	C20,43-46	ICS		
53	CAPACITOR 10uf TAG TANT	C5-12, 42	"		
54	CAPACITOR 2200uf ELECTROLYTIC	C1,2	AMTRON		
55	CAPACITOR 4700uf "	C3,4	"		
56	DIODE EM402	D1-5	ICS		IN4
57	DIODE IN914	D6-8	"	TEXAS	IN9
58	RECTIFIER SB2	BR1,2	SOANAR		SB2
59	RECTIFIER PW01	BR3	IN'ELEC		PW(
60	ZENER DIODE - 12V	Z1	ICS		BZX
61	DIODE	D1		PHILIPS	AA

EAI-ELECTRONIC ASSOCIATES PTY. LIMITED

PARTS LIST

MICROPROCESSOR CARD

11-045-0002

ITEM	DESCRIPTION	DWG. REF.	SOURCE	MAKE	SUPPLIER MFG REF
1	P.C. BOARD	11-045-0002	P'TRONICS		
2	IC 2758	IC3,6	AJF	INTEL	B2758
3	IC 74LS04	IC12	ICS	NS	DM74LS04
4	IC 8085	IC1	AJF	INTEL	P8085A
5	IC 8111A-4	IC7,8	"	"	P211A-4
6	IC 8212	IC2	"	"	P8212
7	IC 74LS138	IC4,5	ICS	NS	DM74LS13
8	RESISTOR 1K	R1	RIFA	IRH	GLP
9	RESISTOR 10K	R3	"	"	"
10	RESISTOR 15K	R2	"	"	"
11	CAPACITOR 33pf CERAMIC	C1	ELCOMA	PHILIPS	632-1022
12	CAPACITOR 0.01uf CERAMIC	C2,3,4,6,7,8,9	"	"	629-0310
13	CAPACITOR 10uf TAG TANT	C5	ICS	TANTALEX	

EAI-ELECTRONIC ASSOCIATES PTY. LIMITED

PARTS LIST

DISPLAY PANEL

11-026-0001

ITEM	DESCRIPTION	DWG. REF.	SOURCE	MAKE	SUPPLI MFG RE
		26-0001 R1	PRINTRONICS		5726B
1	PC CARD	IC2-4,6,7	ICS	NS	CD451
2	IC 4511	IC18	"	"	DM74L
3	IC 74LS00	IC19	"	"	MM74C0
4	IC 74C04	IC12	"	"	DM74LS
5	IC 74LS13	IC 13	"	"	SN74LS
6	IC 74LS14	IC11	"	"	DM74LS
7	IC 74LS74	IC5,9,10	"	"	DM74LS
8	IC 74LS75	IC14	"	"	DM74LS
9	IC 74LS93	IC8	"	"	DM74LS
10	IC74LS138	IC 15-17	"	"	DM74L
11	IC74LS154	L2-46,7	AMTRON	HP	5082-
12	LED - SEVEN SEGMENT	L8-58	AMTRON	"	HLMP1
13	LED - HIGH EFFICIENCY	L5	AMTRON	HP	5082-
14	LED - OVERFLOW	R3-5	RIFA	IRH	GLP
15	RESISTOR 10 ohm	R6,7	"	"	"
16	RESISTOR 150 ohm	R1,2,17,53	"	"	"
17	RESISTOR 330 ohm	C3,14	ELCOMA	PHILIPS	630-
18	CAPACITOR 220pf CERAMIC	C8	"	"	630-
19	CAPACITOR 1000pf CERAMIC	C13	ELCOMA	PHILIPS	629-
20	CAPACITOR 0.01uf CERAMIC	C2,6	ICS		
21	CAPACITOR 0.1uf CERAMIC	C1,5	"		
22	CAPACITOR 10uf TAG TANT	C10-12	ELCOMA	PHILIPS	630-
23	CAPACITOR 470pf CERAMIC	SK M, SK J.	XENITEC		ICN
24	SOCKET 16 WAY DIL	C9	AJF	WIMMA	
25	CAPACITOR 1000uf 6V ELECT	R54 - 57	RIFA	IRH	GL
26	RESISTOR 1K	R8	"	"	"
27	RESISTOR 3K3	R58	"	"	"
28	RESISTOR 10K		GEO BROWN		905
29	STAND OFF TO18				

EAI-ELECTRONIC ASSOCIATES PTY. LIMITED

PARTS LIST

DIGITAL PANEL MAIN BOARD

11-045-0003

ITEM	DESCRIPTION	DWG. REF.	SOURCE	MAKE	SUPPLIER MFG REF.
1	P.C. BOARD	11-045-0003	E.WILSON		
2	40 STR CONNECTOR		AMPEC	HIROSE	3E40P2.54
3	40 WAY RT ANGLE CONNECTOR		"	"	3E40P2.54
4	26 WAY STR CONNECTOR		"	"	3E26P2.54
5	IC 74LS74	IC 8,10	ICS	NS	DM74LS74N
6	IC 7439ON	IC12	"	TEXAS	SN39ON
7	IC 74393N	IC13	"	"	SN393N
8	IC 74LSOON	IC3-6	"	NS	DM74LSOON
9	IC556N	IC11	"	"	LM556N
10	IC 74LS14N	IC1,2,7	TOTAL	MOTOROLA	SN74LS14N
11	CAPACITOR .01 CERAMIC	C1,6,8,9	ELCOMA	PHILIPS	629-03103
12	CAPACITOR 220pf CERAMIC	C4,5	"	"	630-03221
13	CAPACITOR 10uf 35V TANT	C7	ICS		
14	CAPACITOR .056	C2,3			
15	RESISTOR 330 ohms	R1-8	RIFA	IRH	GLP
16	RESISTOR 1K ohm	R10,14	"	"	"
17	RESISTOR 47K ohm (4K7)	R9,13	"	"	"
18	RESISTOR 100 ohm	R11,12	"	"	"
19	RESISTOR 10K 5%	R15-20			

EAI-ELECTRONIC ASSOCIATES PTY. LIMITED

PARTS LIST

DIGITAL PANEL - CONTROL BOARD

11-044-0001

ITEM	DESCRIPTION	DWG. REF.	SOURCE	MAKE	SUPPLIE MFG REF
1	PC BOARD	11-044-0001	E.WILSON	E.WILSON	
2	40 WAY STR CONNECTOR		AMPEX	HIROSE	3E26P2.
3	TOGGLE SWITCH	S0-7	C & K	C & K	7213
4	TOGGLE SWITCH	S8	"	"	7101
5	POTENTIOMETER 5M LIN.	RV1,2	IRH	CTS	
6	POTENTIOMETER 1T 10K LIN.	RV3	"	"	BL5591
7	TRIMPOT 500 ohms	RV4	ICS	SOANAR	VTP500
8	IC 556	IC 7			
9	IC 7439ON	IC3,4	ICS	TEXAS	SN7439
10	IC 74LS00N	IC8,2	"	NS	DM74LS
11	IC 74LS02N	IC9	"	"	
12	IC 74LS74N	IC5	"	"	DM74LS
13	IC 74LS04N	IC1	"	"	DM74LS
14	IC 14555B CMOS	IC6		SSS	SCL14
15	CAPACITOR .01 CERAMIC	C1-4,6	ELCOMA	PHILIPS	629-0
16	CAPACITOR .047 POLY #10%	C5,7	SOANAR		
17	RESISTOR 820 ohms	R5	RIFA	IRH	GLP
18	RESISTOR 330 ohms	R3	"	"	"
19	RESISTOR 10K	R1,2,6	"	"	"
20	RESISTOR 1K2	R4	"	"	"
21	DIODE IN 914	D9,10	ICS	TEXAS	IN9
22	LED - RED		HP	HP	HLMP

EAI-ELECTRONIC ASSOCIATES PTY. LIMITED

PARTS LIST
DIGITAL PANEL - PATCH PANEL
11-05-0002

ITEM	DESCRIPTION	DWG. REF.	SOURCE	MAKE	SUPPLIER MFG REF.
1	P.C. BOARD	11-005-0002	E.WILSON	E.WILSON	
2	LEGEND PANEL		Ph'TRONICS		
3	EYELETS 2mm		R.H.J'SON	EYELETS	1132
4	ZIF CONNECTOR W/6" RELEASE BAR		AMP		1-530801-
5	RESISTOR 1K	R1,2	RIFA	IRH	
6	IC 7404N	IC1,2			
7	IC 7400N	IC3,4	ICS	TEXAS	DM7400N
8	IC 7410N	IC5,6	"	NS	DM7401N