HITACHI Analog·Hybrid Computer 220/240

—— Operator's Manual for Digital Logics. ——

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CONTENTS

Operator's Manual for Digital Logics

1. Introduction

The purpose of this manual is to describe operations, programs and fundamental applications of the digital logics of Hitachi analog computers. The digital logics are intended to add higher logical techniques to the operation of general analog components. Information of only marginal interest to the programmer, such as specifications, maintenance terms of analog components, is omitted.

This manual places emphasis on the following:

(1) Elements

What kinds and how many elements are there?
Where are they located? What do they do?
In what ways can they be used? How are they patched?

(2) Composite elements

Combination of elements. Control, decision and memorization accomplished by such element combinations. What kinds of control logics are available? How are they applied?

(3) Application

Solution of fundamental problems, and some exercises. Examples of practical applications. Application to boundary and extreme value problems.

Items (2) and (3) also include the logical use of analog components.

2. Logic Elements

All logic elements and control terminals use high voltage (logic ONE) and low voltage (logic ZERO) for both input and output signals. Logic ONE is nominally +6.0 V DC but may go as high as +24V DC. The performance will not be adversely affected by voltage increase. The nominal value of low voltage is 0 V, but its level change is allowable within a range of approximately ±1V. In some cases the input and output voltages become about -2 and 3 V, respectively. This does not have any adverse effect on performance either. However, it is recommendable for the programmer to remember that the voltage levels of logic elements are always +6 and 0 V.

With a Hitachi analog computer, regardless of its control system being the EMC type, the integrator and operation mode can be controlled directly from digital logic elements without using any voltage level converter. Also, digital logic elements are directly controllable by the use of the logic signals generated in the analog patch section.

RUN, STOP, CLEAR and MANUAL CLOCK of all the digital logic elements are controlled on the logic control panel (CT-264). Under these four modes, the logic element operates as follows:

RUN: Element operates in accordance with input signal.
Output signal of the standard clock is emitted.

STOP: Operation stops. Output signal will not change even when input signal is varied.
Output of the standard clock goes off.

CLEAR: All output levels are reset to the initial condition.
Output signal of the standard clock is 0.
Element will operate if input signal if changed.

CLOCK: Push this button, then generated one pulse output for manual checking to programs and RING COUNTER.

Gates are always in the operative condition with no regard to these four modes.

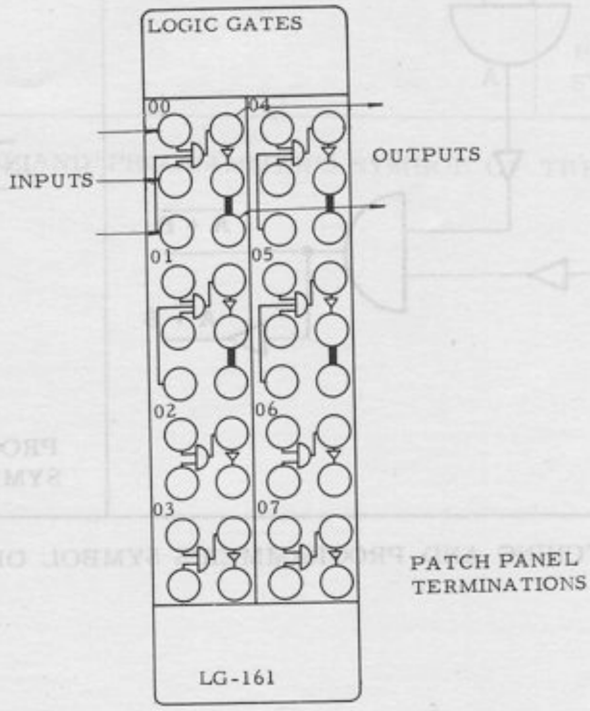
2.1 AND and NAND gates

The patch hole marking of patch unit LG-161 having AND and NAND gates is shown in Fig. 2.1. One LG-161 unit includes four 3-input gates and four 2-input gates. Each gate has one inverter at its output. The output of this inverter is the NAND gate output. Outputs of AND and NAND gates for various logic input signals are listed in Table 2.1.

Input		AND	NAND
1	1	1	0
1	0	0	1
1	open	1	0
0	1	0	1
open	1	1	0
0	0	0	1
open	open	1	0

Table 2.1

The "open" in Table 2.1 signifies that the input terminal is not used. This open input terminal normally operates as logic ONE. Therefore, it is unnecessary to terminate the remaining input to logic ONE when only two inputs of a 3-input AND gate are used.



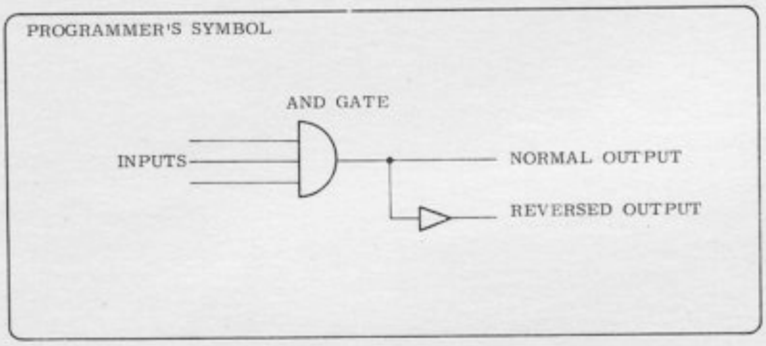


Fig. 2.1 PATCH PANEL TERMINATIONS AND PROGRAMMER'S SYMBOL OF THE AND GATE

2.2 OR and NOR gates

The output of OR gate is logic ONE when at least one of the OR gate inputs is logic ONE. NOR is equivalent to the reversed OR. No OR or NOR gates are incorporated in the digital logic patch panel; however, an OR gate can be formed by patching utilizing the AND gate mentioned in Item 2.1. OR operations can be obtained by reversing all the 0's and 1's in Table 2.1 in respect of the relationship between input and AND gate output. For this reason, the OR gate can be formed by reversing the signals of all inputs and outputs of the AND gate through inverters.

The actual patch panel is designed to be able to connect most logic signals as normal and reversed signals. When the OR signal of certain two signals is desired, all that is needed is to supply an AND gate with the reversed signals of these signals and to extract the output from the inverter attached to that gate. Fig. 2.2 shows the patching for ORing the output signals A and B of two AND gates.

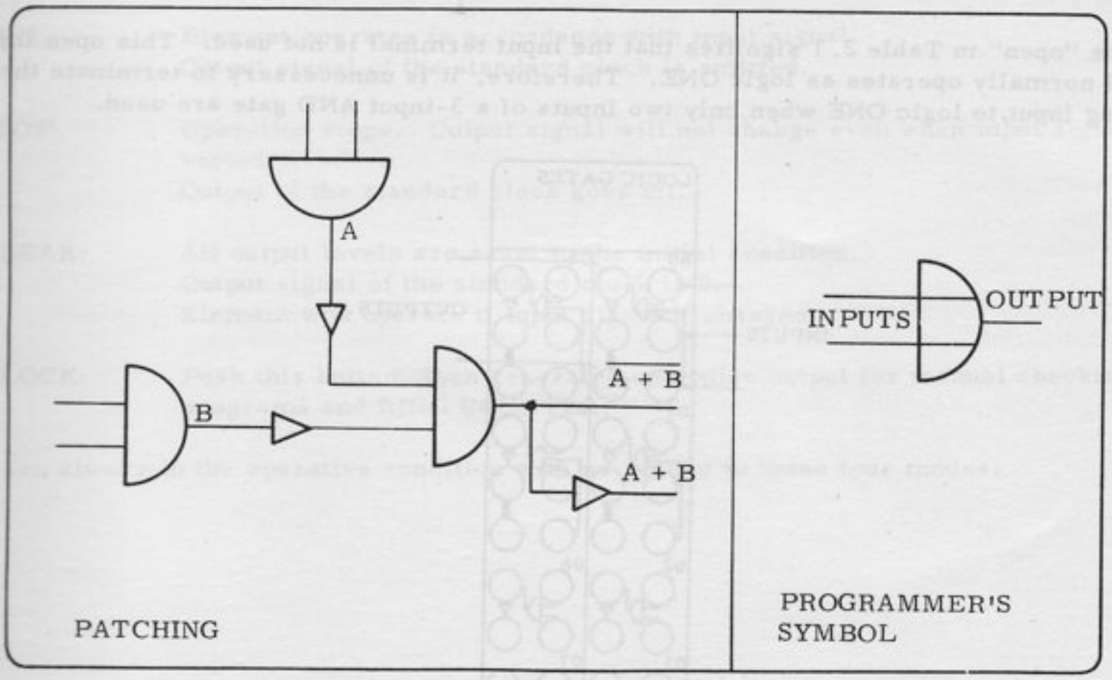


Fig. 2.2 PATCHING AND PROGRAMMER'S SYMBOL OF THE OR GATE

2.3 Inverter

Most logic elements are provided with an inverter directly coupled with their output, and very few programs require independent inverters. However, since the standard clock (CL-161), main control mode logic output (MC-161) do not have inverted outputs, an AND gate is used when their reversed output is needed. An AND gate can be operated identically to an inverter by using only one input of the AND gate and obtaining signal from the reversed output of that gate. That is, the input and output of the AND gate are identical with each other since the open terminal of AND gate is the same as logic ONE. The input therefore becomes the reversed signal by the inverter placed in the succeeding stage.

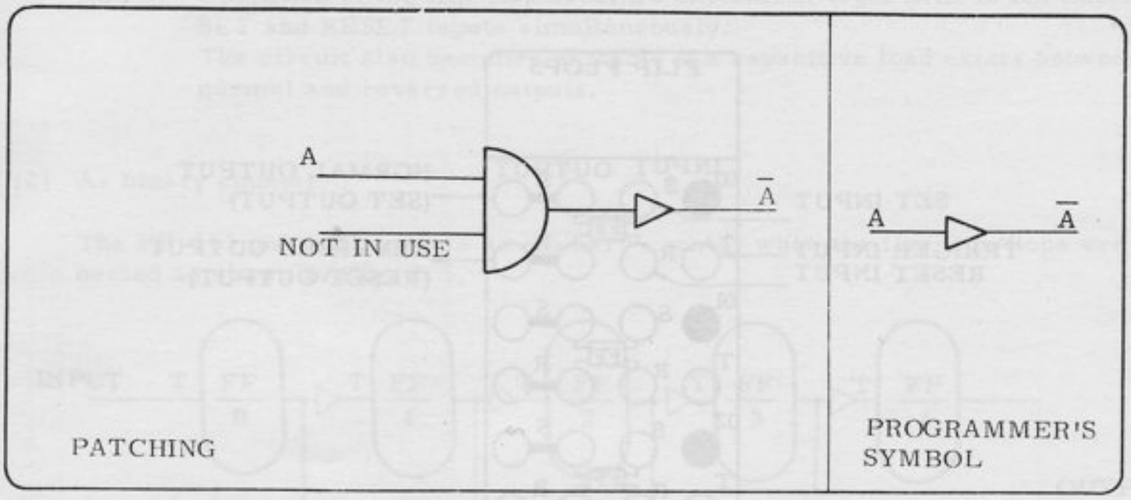


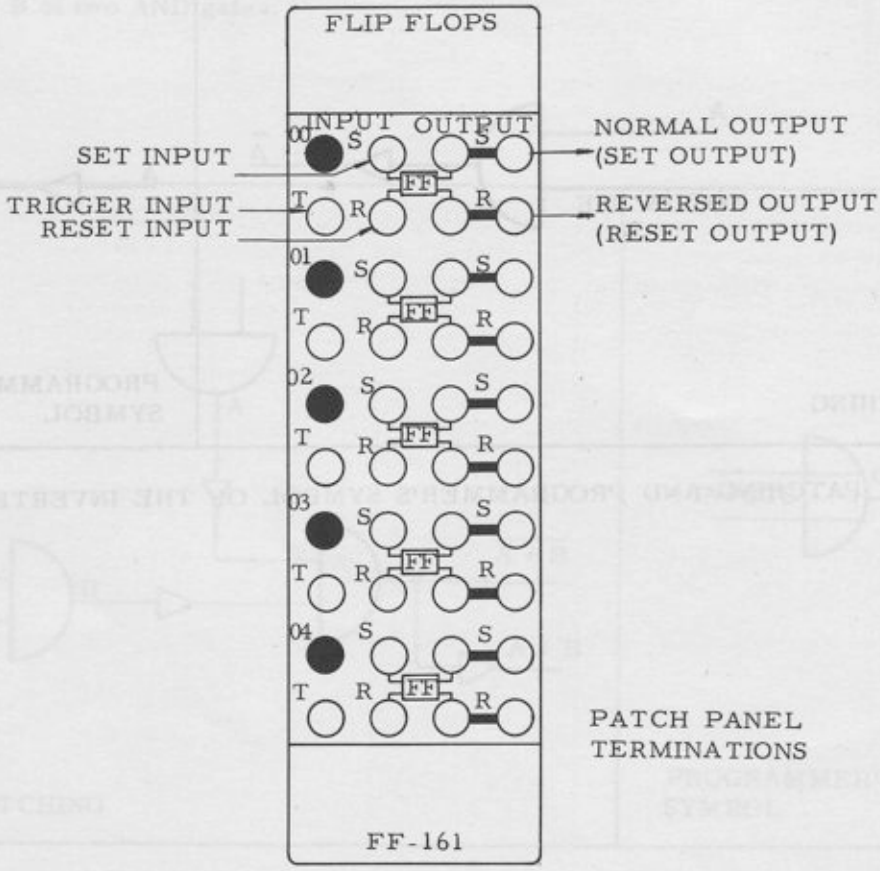
Fig. 2.3 PATCHING AND PROGRAMMER'S SYMBOL OF THE INVERTER

2.4 Flip-flops

(1) As independent flip-flops

The patch hole marking of flip-flop patch unit FF-161 is shown in Fig. 2.4. Each FF-161 unit has five flip-flops.

Each flip-flop is individually provided with SET, RESET and TRIGGER inputs, and NORMAL and REVERSED outputs. All flip-flops let their normal output be logic ZERO and their reversed output be logic ONE when the CLEAR button is pressed on the logic control panel.



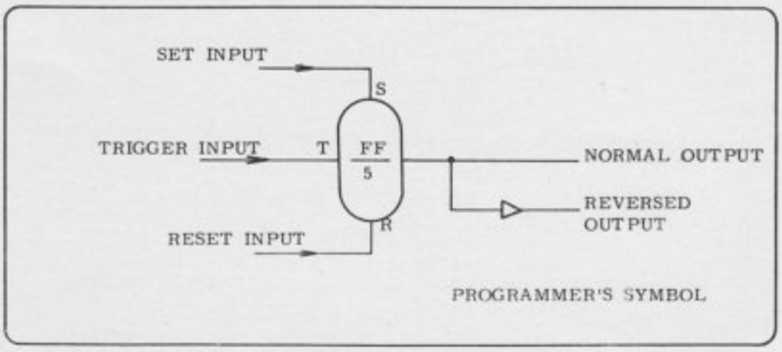


Fig. 2.4 PATCH PANEL TERMINATIONS AND PROGRAMMER'S SYMBOL OF THE FLIP FLOP

When logic ONE is fed into the SET input of a flip-flop, its normal output becomes logic ONE. When the logic ONE at the SET input is gone and changed to logic ZERO, the above condition remains intact until logic ONE is supplied to the RESET input. Also, the output will not change at all regardless of how many times logic ONE is resupplied to the SET input if the normal output is logic ONE. The same performance is applicable when the SET and RESET inputs are exchanged for each other. When logic ONE and logic ZERO are alternately fed into the TRIGGER input, the output logics of normal and reversed outputs alternate with each other every time logic ONE enters the input. Therefore, logic pulse of half the frequency are obtained from the normal output when logic pulses of the desired frequency are fed into the TRIGGER input.

NOTE: Operation of the flip-flop becomes unstable if logic ONE is fed into the SET and RESET inputs simultaneously.
The circuit also becomes unstable if a capacitive load exists between the normal and reversed outputs.

(2) As binary counter

The FF-161 unit will operate as a binary counter when the five flip-flops are connected as shown in Fig. 2.5.

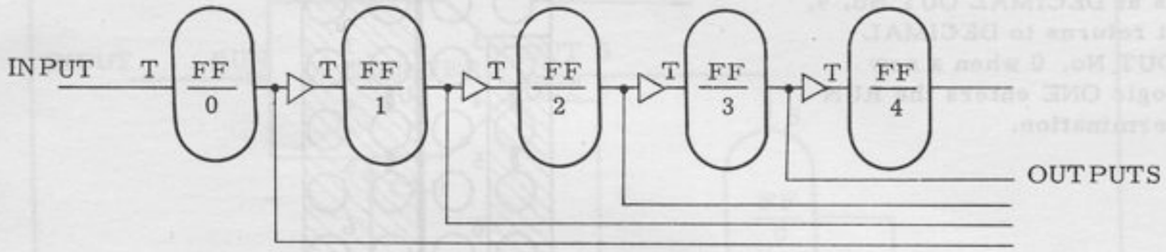


Fig. 2.5 PATCHING OF THE BINARY COUNTER

(3) As shift register

A 5-bit shift register can be formed by combining five flip-flops. However, a ring counter (RC-161) is incorporated in the logic patch-panel as a separate unit, and can simply be utilized as a shift register. The decimal counter (CU-161) can also be used as a shift register. It is therefore practically unnecessary to compose a shift resister by combining flip-flops.
When necessary, however, a shift register can be produced by patching as shown in Fig. 2.6.

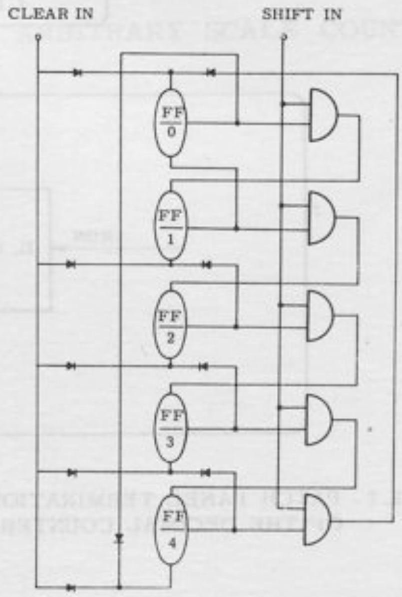


Fig. 2.6 PATCHING SCHEMATIC OF THE SHIFT RESISTOR

2.5 Decimal counter

The patch hole marking of decimal counter patch unit CU-161 is shown in Fig. 2.7. One patch unit CU-161 contains two decimal counters.

One decimal counter has two inputs (RUN and CLEAR), one CARRY OUT, and ten outputs (DECIMAL OUT). One of the ten DECIMAL OUTs is always logic ONE, and the remaining nine DECIMAL OUTs are logic ZERO. When logic ONE is fed into CLR (abbreviation of CLEAR), only DECIMAL OUT No. 0 of the ten DECIMAL OUTs turns to logic ONE and the other DECIMAL OUTs No. 1 through No. 9 become logic ZERO. This condition remains so as long as the CLR termination keeps logic ONE.

The logic ONE at DECIMAL OUT No. 0 moves to a higher-number DECIMAL OUT one by one every time a logic ONE enters the RUN termination while the RUN termination is supplied with nothing or with logic ZERO. If the logic ONE is at DECIMAL OUT No. 9, it returns to DECIMAL OUT No. 0 when a new logic ONE enters the RUN termination.

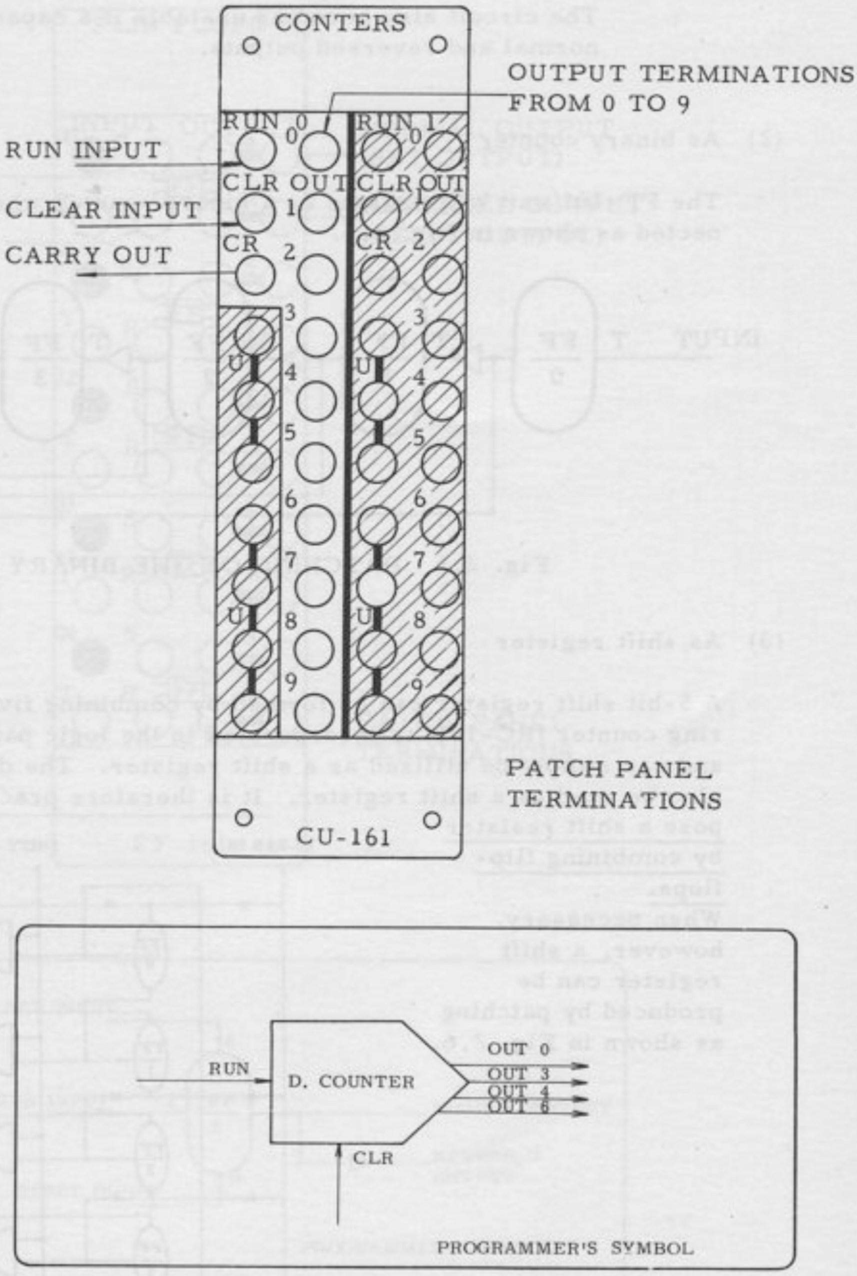


Fig. 2.7 PATCH PANEL TERMINATIONS AND PROGRAMMER'S SYMBOL OF THE DECIMAL COUNTER

When the logic ONE returns from DECIMAL OUT No. 9 to DECIMAL OUT No. 0, the CR (abbreviation of CARRY) termination issues an inpulse. Provided that the CR termination is terminated at the RUN termination of the second decimal counter, these two counters can be as a two-digit decimal counter.

The output of counter for each digit can be monitored on the digital logic control panel.

As arbitrary scale counter:

The decimal counter can be used as a quinary counter by patching as shown in Fig. 2.8. In the quinary counter, the output logic ONE circulates from DECIMAL OUT No. 0 through DECIMAL OUT No. 4 in a ring. The CR termination is not used for this counter, and DECIMAL OUT No. 5 termination serves as CR termination. Therefore, a two-digit quinary counter can be formed by producing two of the above quinary counter and patching the DECIMAL OUT No. 5 termination of one quinary counter to the RUN termination of the quinary counter.

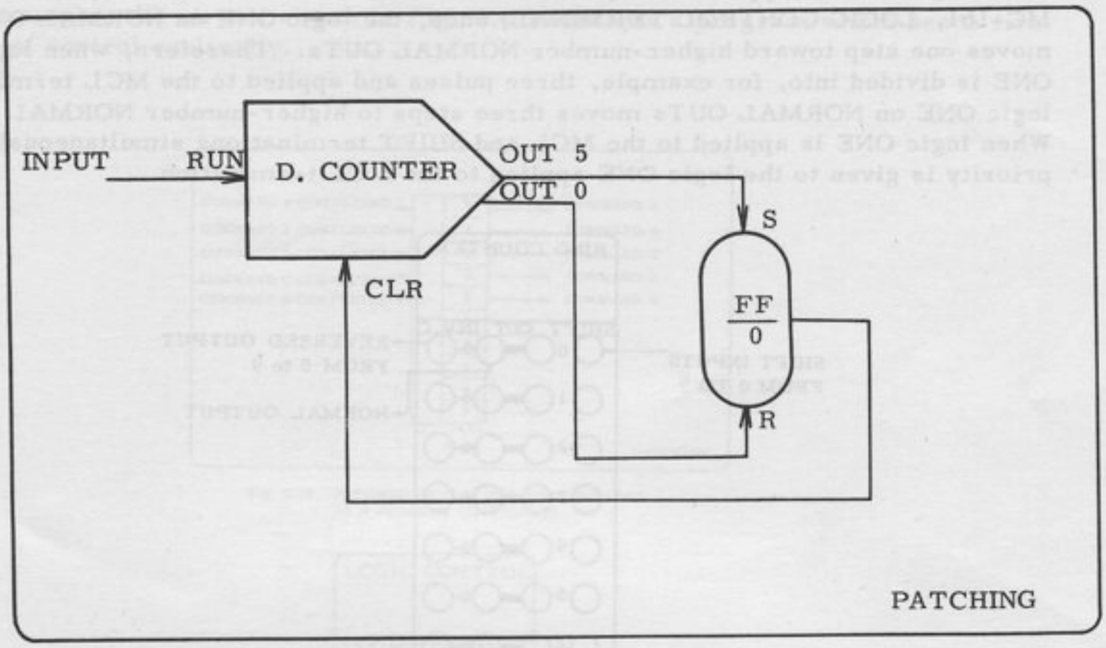


Fig. 2.8 PATCHING FOR ARBITRARY SCALE COUNTING

2.6 Ring counter

(1) Function

Patch hole marking of ring counter patch unit RC-161 is shown in Fig. 2.9. The ring counter consists of ten individual SHIFT inputs. Ten NORMAL OUTs; and ten REVERSED OUTs. This logic module is also manually controllable by using pushbutton CLOCK located on the logic control panel.
One of the ten NORMAL OUTs is always logic ONE, and all the remaining nine NORMAL OUTs are logic ZERO.
When logic ONE is applied to one of the ten SHIFT INPUTs, the corresponding NORMAL OUT turns to logic ONE and the other nine NORMAL OUTs become logic ZERO. This condition remains so until another shift input enters one of the SHIFT INPUTs, even after the former shift input becomes logic ZERO.
When pushbutton CLEAR on the logic control panel is pushed, NORMAL OUT No. 0 becomes logic ONE, and the other NORMAL OUTs are logic ZERO. If other than SHIFT INPUT No. 0 is logic ONE simultaneously, the corresponding NORMAL OUT remains logic ONE.
When logic ONE is applied to the MCL termination (on the MODE CONTROL PANEL MC-161, LOGIC CONTROL TERMINAL) once, the logic ONE on NORMAL OUTs moves one step toward higher-number NORMAL OUTs. Therefore, when logic ONE is divided into, for example, three pulses and applied to the MCL termination, logic ONE on NORMAL OUTs moves three steps to higher-number NORMAL OUTs. When logic ONE is applied to the MCL and SHIFT terminations simultaneously, priority is given to the logic ONE applied to the MCL termination.

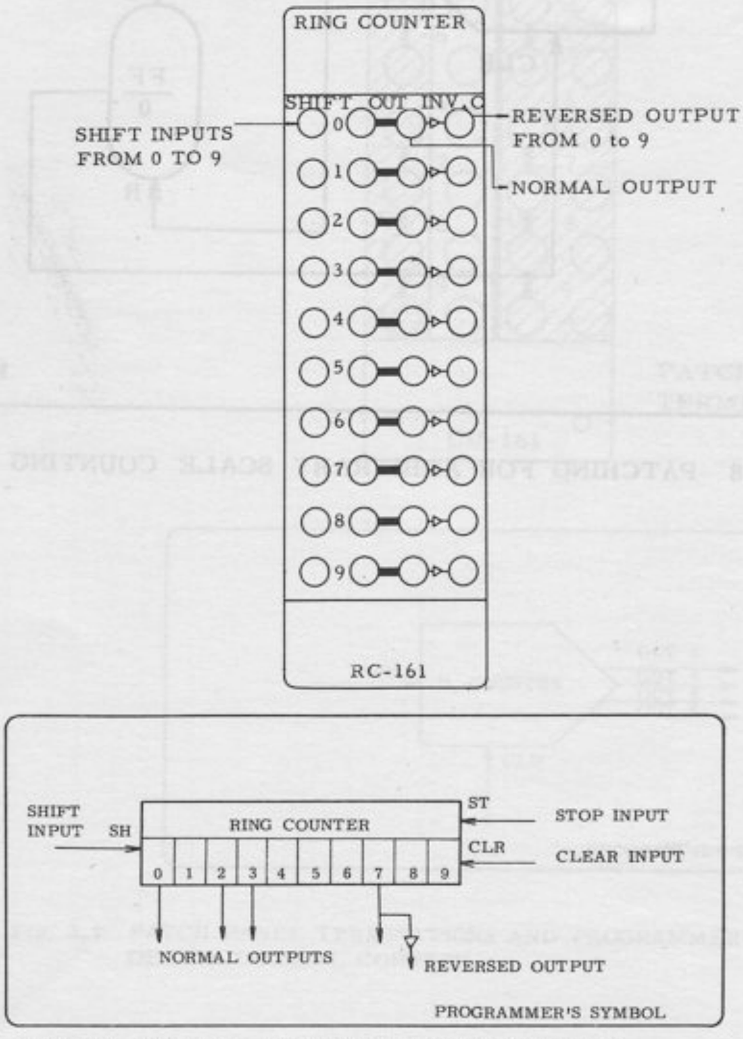


Fig. 2.9 PATCH PANEL TERMINATIONS AND PROGRAMMER'S SYMBOL OF THE RING COUNTER

All operation of the ring counter stops when push the STOP pushbutton on the logic control panel. This condition remains so until push the CLEAR pushbutton on the logic control panel. When push the CLOCK pushbutton on the logic control panel once by once, then logic ONE on NORMAL OUTs moves one step toward higher-number NORMAL OUTs. (But MCL terminal must be open.) It is undesirable, when using the ring counter in an ordinary manner, to simultaneously apply many logic ONEs to the input terminations because the program becomes complex. It is recommendable to use the ring counter to a degree that either one of the inputs is logic ONE at all times or none of them is logic ONE once in a while.

(2) As program controller

The ring counter is utilized as the circuit for controlling a program which requires cyclic mode control. The ring counter is designed to supply its output from ten separate terminations; however, it does not necessarily mean that the counter is solely used for the programs requiring ten kinds of control per cycle. Because the ring counter can be employed, similarly to the decimal counter, by using only desired steps and unusing the other steps.
For example, the circuit shown in Fig. 2.10 controls a program which needs five kinds of control cyclically.

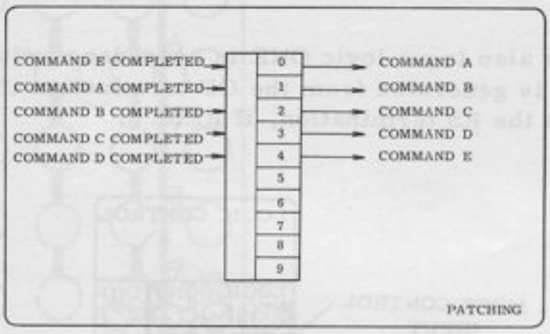


Fig. 2.10 PATCHING OF THE RING COUNTER USED AS A PROGRAM CONTROLLER

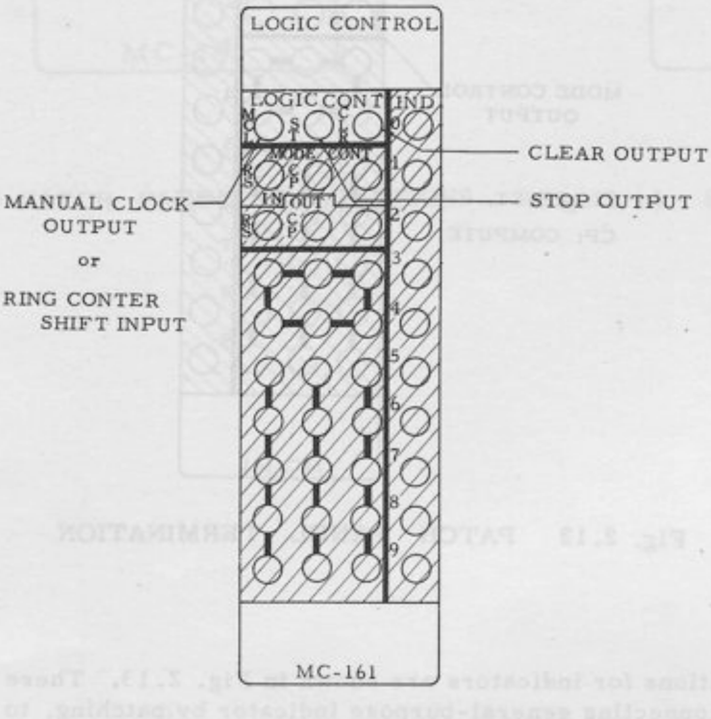


Fig. 2.11 PATCH PANEL TERMINATIONS

2.7 Logic Control

(1) Mode control of digital logic

The output terminations provided for mode control of the overall digital logic modules are shown in Fig. 2.11
They are STOP and CLEAR logic output terminations and MANUAL CLOCK output or RING COUNTER SHIFT input terminations.

The MCL termination is one pulse output when the digital logic mode is CLOCK or RING COUNTER SHIFT input signal; the STOP termination is logic ONE when the mode is STOP; and the CLR termination is logic ONE when the mode is CLEAR.

(2) Mode control of analog module

The input and output terminations utilized for effecting the mode control of analog module from the digital logic patch panel are shown in Fig. 2.12.
Input terminations are RS (RESET) and CP (COMPUTE), and output terminations are RS and CP, totaling four terminations.
The analog computer console mode becomes RESET when logic ONE enters the RS input termination, and the mode turns to COMPUTE when logic ONE enters the CP input termination.

Output terminations also issue logic ONE in accordance with the console mode. That is, logic ONE is generated from the CP termination if the console mode is COMPUTE; from the RS termination, if RESET.

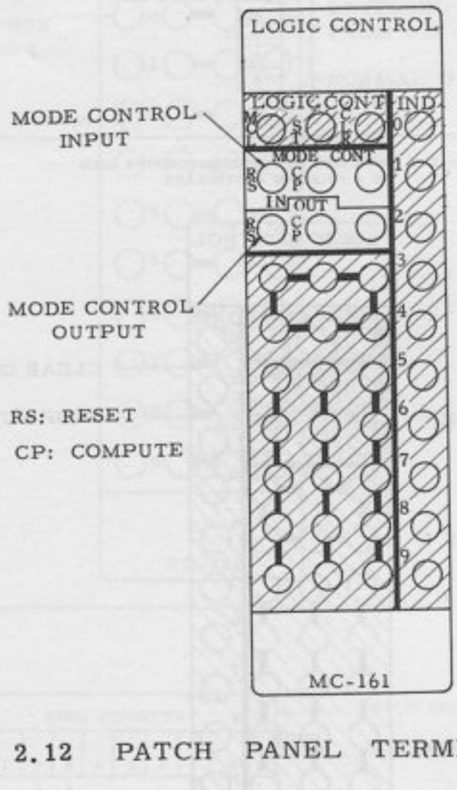
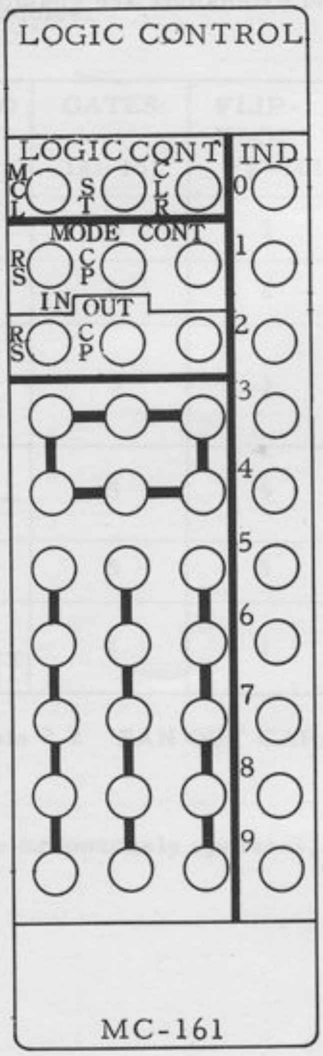


Fig. 2.12 PATCH PANEL TERMINATION

(3) Indicator

Patch terminations for indicators are shown in Fig. 2.13. These terminations are used for connecting general-purpose indicator by patching, to confirm the operation of modules (for example, FLIP FLOP, AND gate) which do not have an indicator.

When logical ONE enters one of the terminations, the indicator lamp corresponding to the termination number lights on the control panel.



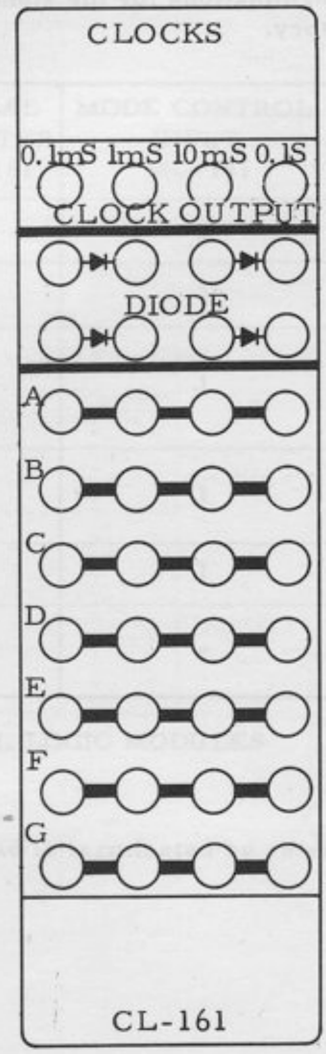


Fig. 2.13 PATCH PANEL TERMINATIONS

Fig. 2.14 PATCH PANEL TERMINATIONS

2.8 Clock

The patch hole marking of clock patch unit CL-161 is shown in Fig. 2.14. This unit consists of a standard clock, diodes and extension terminations.

Terminations for the standard clock, diodes and extensions are considered to be self-explanatory.

2.9 Fan-out capacity of digital logic modules

Inputs and outputs of digital logic modules can be mutually terminated between the modules. However, the load of an output is limited since each output has a specific fan-out capacity. The number of loads to be terminated differs depending on the type of load. Table 2.2 shows the maximum number of loads allowable according to the combination of input and output of various modules.

FROM \ TO	GATES LG-161	FLIP-FLOP FF-161	RING COUNTER RC-161	DICIMAL COUNTER CU-161	MODE CONTROL INPUT MC-161
LG-161	5	5	1	2	1
FF-161	2	2	1	2	1
RC-161 NORMAL OUT	3	3	1	2	1
RC-161 REVSD OUT	5	5	1	2	1
CU-161	5	5	1	2	1
CU-161 CARRY OUT	1	1	-	1	-

Table 2.2 FAN OUT CAPABILITY OF DIGITAL LOGIC MODULES

When a logic module erroneously operates, check if exessive load is terminated by referring to the table.

3. Control Circuits Using Logic Modules

This section deals with example logic components composed of integrator, comparator, and the digital logic modules described in Section 2. This section also explains functions and fundamental applied circuits of such components. For detailed explanation of the patching regarding the analog components quoted in this section, refer to the operation manual separately issued.

3.1 Track/store

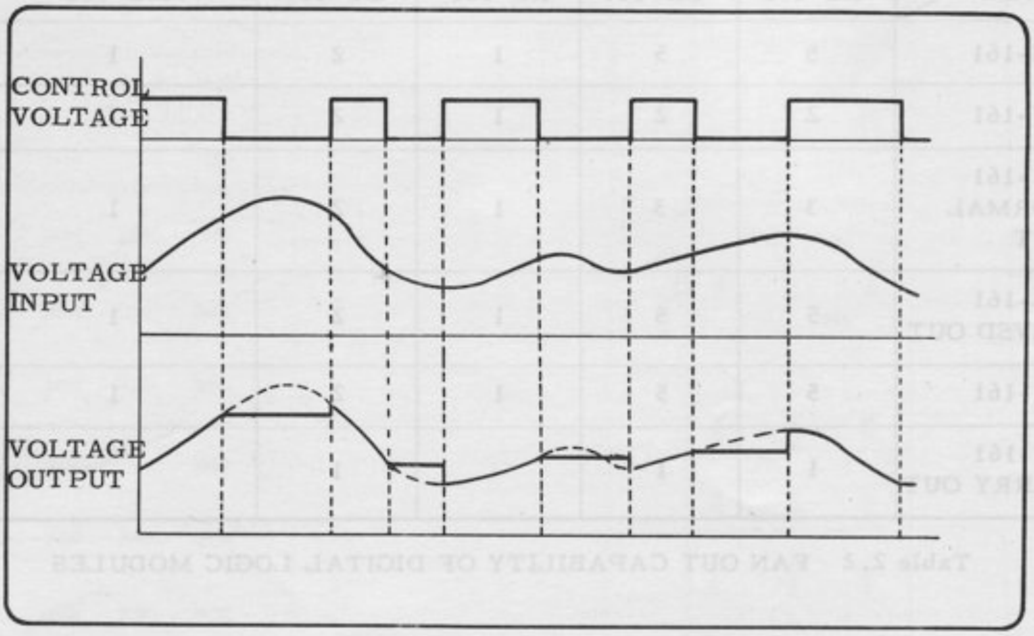


Fig. 3.1 INPUT AND OUTPUT OF TRACK/STORE UNIT

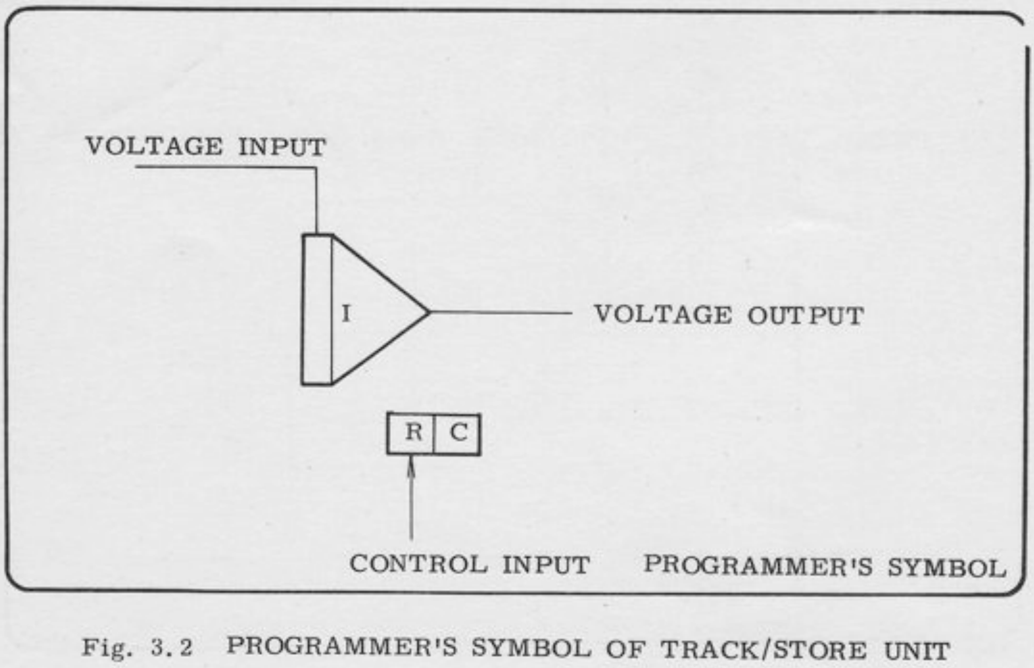


Fig. 3.2 PROGRAMMER'S SYMBOL OF TRACK/STORE UNIT

3.2 Sample/hold

A sample/hold unit can be formed by terminating two track/store units in series. The block diagram is shown in Fig. 3.3. Input and output voltages of each component of the unit are shown in Fig. 3.4. The voltage output No. 1 actually is a negative value; however, the negative sign is omitted for easy understanding. The transfer delay network, which will be described later, is an applied circuit of this sample/hold unit.

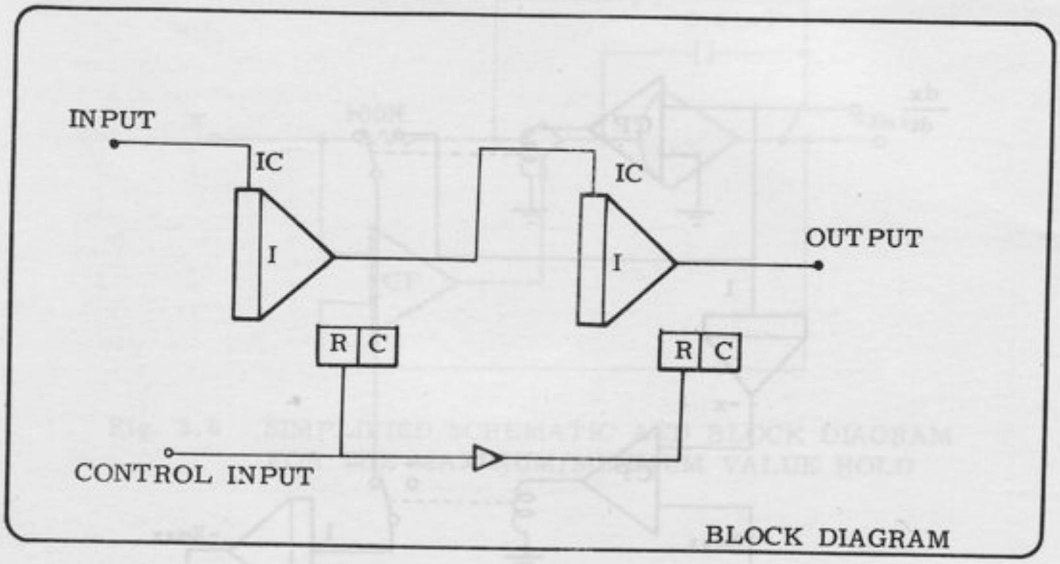


Fig. 3.3 BLOCK DIAGRAM OF SAMPLE/HOLD UNIT

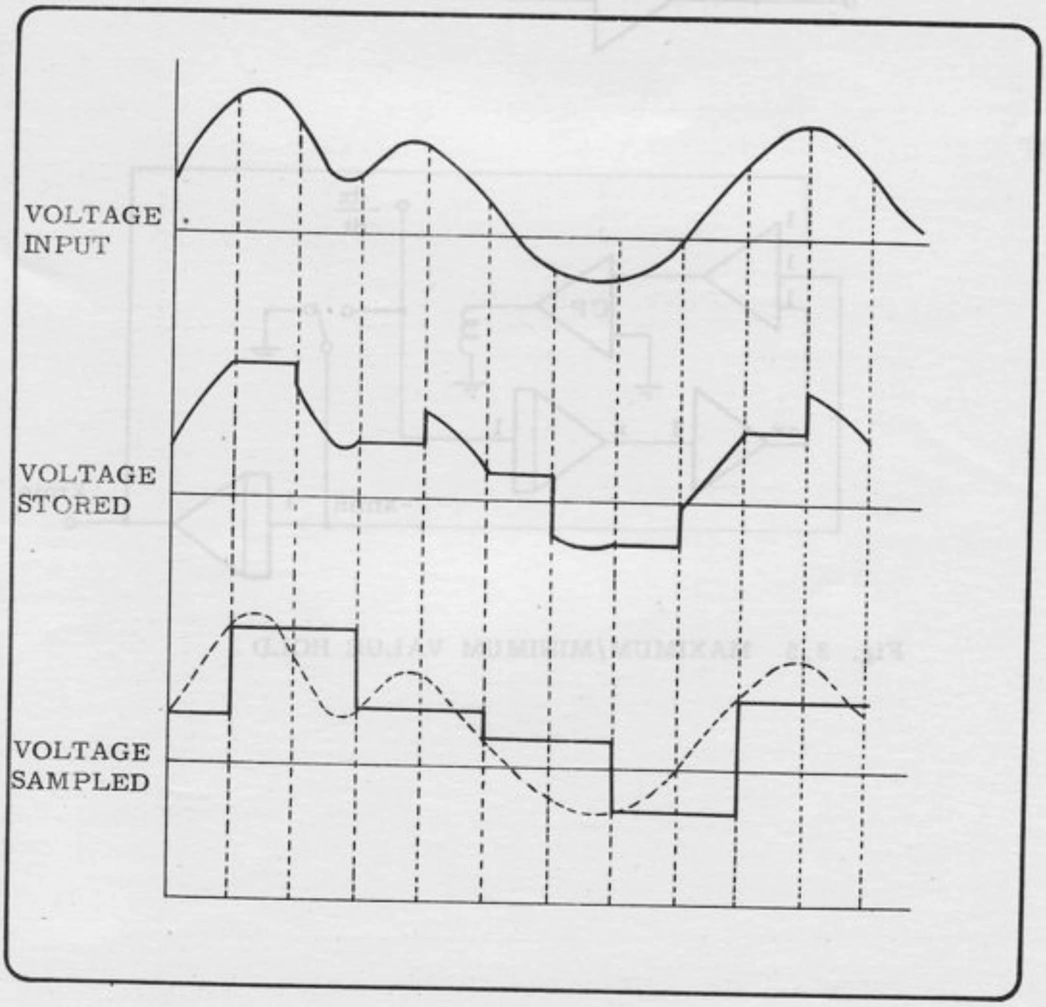


Fig. 3.4 INPUT AND OUTPUT OF SAMPLE/HOLD UNIT

3.3 Max. /min. value hold

The logic circuit for storing the maximum or minimum value of a function is often needed. Fig. 3.5 shows two examples of maximum value hold composed by combining relay type comparators, integrators and adders. They can be used as minimum value hold by merely inverting the sign of $\frac{dx}{dt}$.

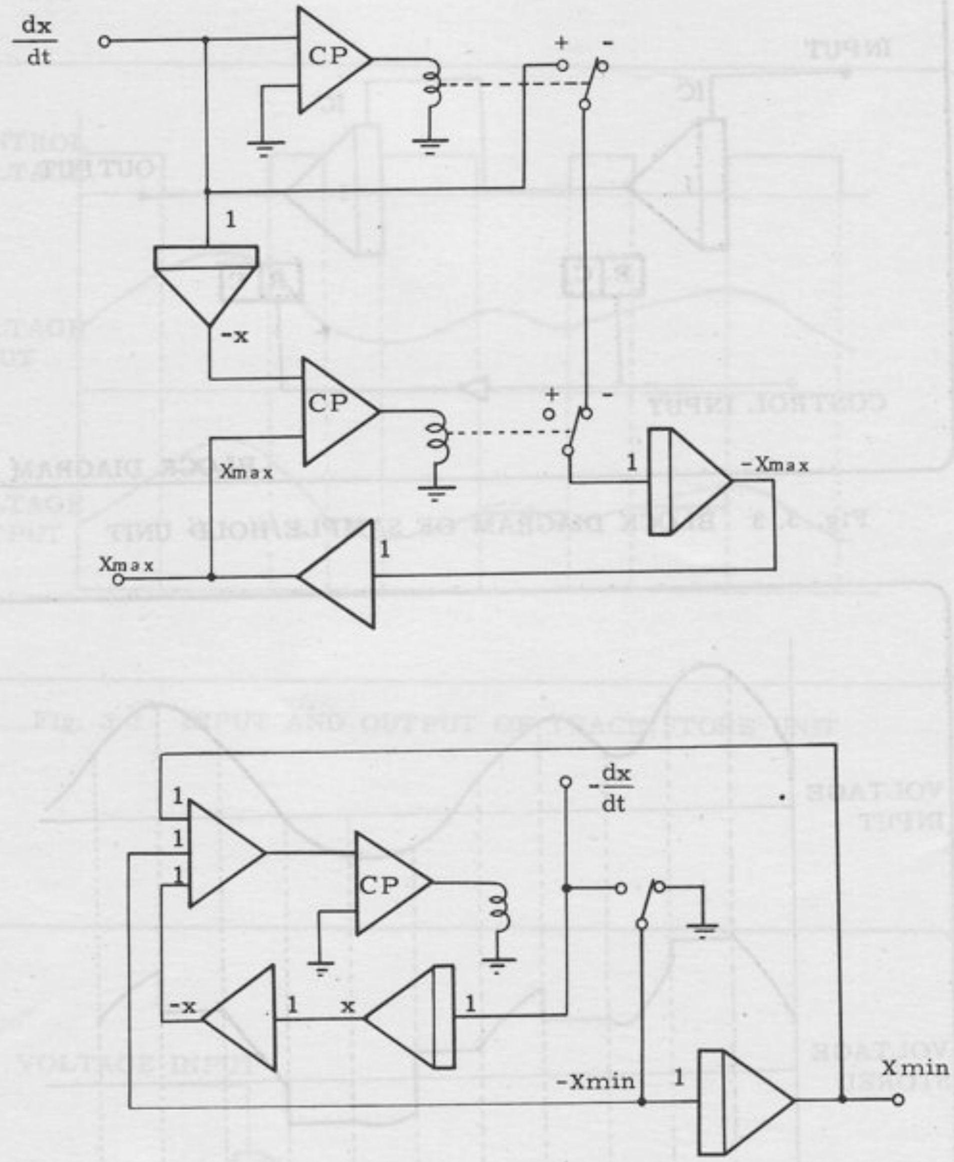


Fig. 3.5 MAXIMUM/MINIMUM VALUE HOLD

The above circuit uses relays. When a higher speed computation is required, the digital logic module is usable for the complete control by the EMC system. Fig. 3.6 shows an example of the circuit.

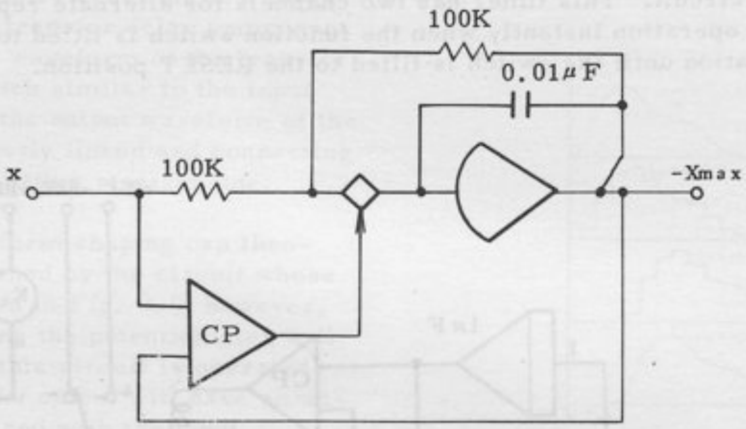


Fig. 3.6 SIMPLIFIED SCHEMATIC AND BLOCK DIAGRAM FOR THE MAXIMUM/MINIMUM VALUE HOLD

3.4 Analog timer

It is seldom required to form an analog timer by patching because in many cases a standard timer is provided. If an analog timer is needed, however, it can be composed by patching. Fig. 3.7 shows an example of the circuit and the relationship between the input and output of the circuit. This timer has two channels for alternate repetitive computation. The timer starts operation instantly when the function switch is titled to the START position. It continues operation until the switch is tilted to the RESET position.

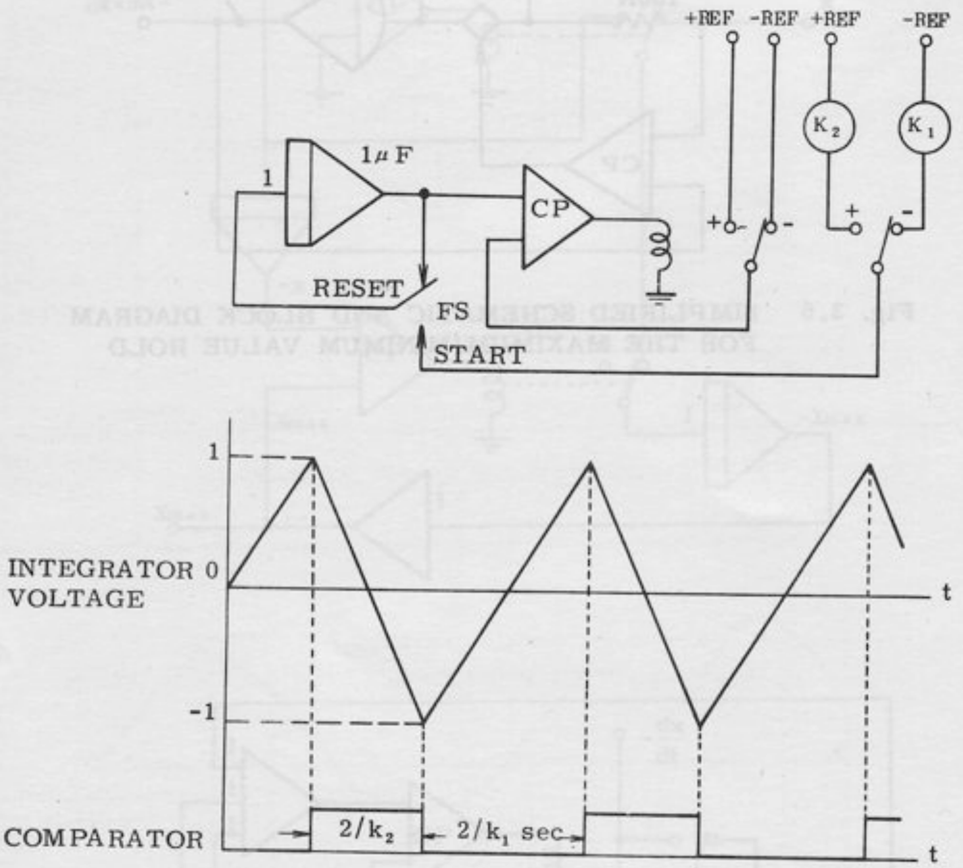


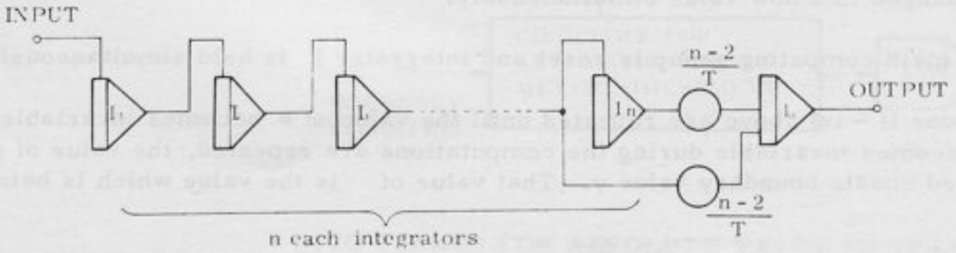
Fig. 3.7 ANALOG TIMER

3.5 Transfer delay

A transfer delay component can be formed by directly linking many track/store units. However, the track/store units merely directly linked give an output waveform in the form of a staircase, sometimes resulting in a large error and making the transfer delay component unusable. The output waveform of the transfer delay will be made much similar to the input waveform by shaping the output waveform of the track/store units directly linked and connecting each sampled voltage with a straight line.

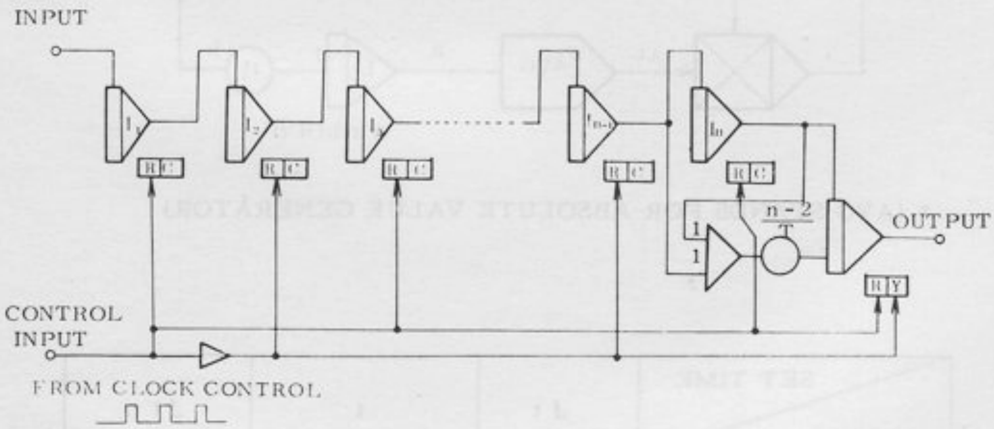
The above waveform shaping can theoretically be accomplished by the circuit whose block diagram is shown in Fig. 3.9; however, a slight error in setting the potentiometer will be accumulated when this circuit is operated for a long time, and the output will have an unnecessary bias compared with the input.

Fig. 3.8 TRANSFER DELAY



INTEGRATORS. I_{2i} HAVE TO BE IN COMPUTE (OR IN HOLD) WHILE INTEGRATORS, I_{2i+1} ARE IN RESET, AND VICE VERSA SUCH MODES ARE PERIODICALLY INTERCHANGED EACH OTHER.

Fig. 3.9 PRINCIPLE OF THE TRANSFER DELAY



THE PULSE WIDTH OF LOGIC ONE MUST BE AS SMALL AS POSSIBLE IN COMPARISON WITH THE WIDTH OF LOGIC ZERO. HOWEVER, IF THEY ARE TOO SMALL, INTEGRATORS CANNOT HAVE ENOUGH TIME FOR TRACKING.

Fig. 3.10 TRANSFER DELAY

3.6 Guide to boundary value problem

The block diagram of a typical circuit for determining the initial value or parameter so that the given equation meets a specific boundary condition will be introduced here. The main computing group shown in Fig. 3.11 denotes the block diagram for solving the given equation. That is, the unknown which should be included in the given equation will be supplied from outside the main computing group.

Integrator I_1 integrates the difference between y and the boundary value t of y, and changes the value of α. Potentiometer P_1 is provided for adjusting the speed of changing the value of α ; the smaller this value, the slower the convergence speed of α, and when the value is too great, the value of α oscillates, and sometimes does not converge. This computation proceeds as listed below:

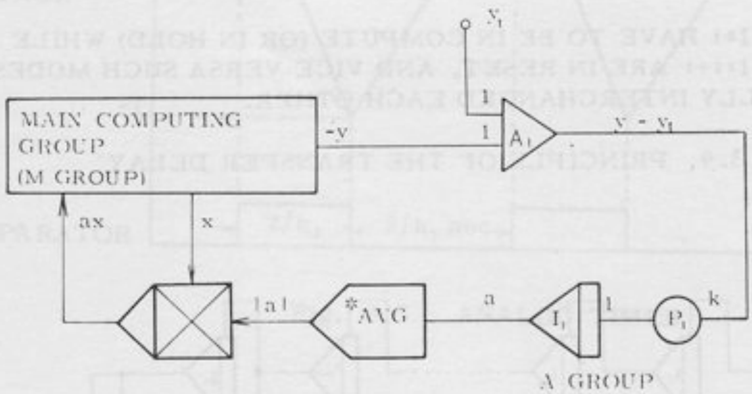
i) Using an arbitrary α value, the main computing group conducts computation to solve the given equation.

ii) The main computing group is held after compute time t has elapsed.

iii) The value of y after compute time t is compared with boundary value t, the difference is integrated for a certain period by integrator I_1, and the value of is changed to a new value simultaneously.

iv) The main computing group is reset and integrator I is held simultaneously.

Computations i) ~ iv) above are repeated until the value of α becomes invariable. If the value of α becomes invariable during the computations are repeated, the value of y after time t has elapsed equals boundary value y. That value of is the value which is being sought.

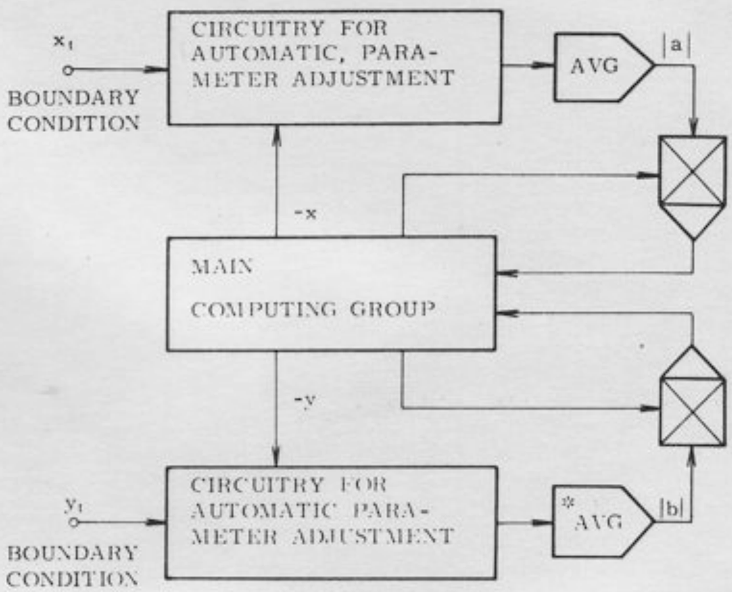


* (AVG STANDS FOR ABSOLUTE VALUE GENERATOR)

SET TIME / GROUP	Δt	t	Δt
WHEN M GROUP IS:	RESET	COMPUTE	HOLD
A GROUP is:	HOLD	HOLD	COMPUTE

Fig. 3.11 REFERENCE NETWORK FOR BOUNDARY VALUE PROBLEM WHICH INCLUDES AN UNKNOWN PARAMETER "a"

Two of the above-mentioned parameter tracking circuit are added to the main computing group for solving an equation having two unknown parameters and two boundary values. These two tracking circuits are not provided with any correlation and let to compute entirely independently. Therefore, it sometimes takes a longer time to obtain the converged value of two parameters, compared with the steepest descent method, to be described later, by which the aimed value is obtained fastest and effectively.



* (AVG STANDS FOR ABSOLUTE VALUE GENERATOR)

Fig. 3.12 LOGICAL CIRCUITRY FOR ANALYSIS OF BOUNDARY VALUE PROBLEM WITH TWO UNKNOWN PARAMETERS "a" AND "b"